# Novel Small-Dimension poly-Si TFTs with Improved Driving Current and Suppressed Short Channel Effects

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## Abstract

A novel small-dimension poly-Si TFT with ultrathin channel (300 Å) and W-raised source/drain is proposed. The kink effect is effectively suppressed due to the reduced channel thickness. Tungsten film selectively grown on the source/drain region greatly improves the sheet resistance as well as increases the drain current. Furthermore, the W film is selectively deposited under low temperature (300 ºC). The process is simple and compatible with conventional low-temperature poly-Si (LTPS) process. Characteristics of devices with different channel thicknesses and dimensions are also studied, revealing that new devices with ultrathin channel are free from the floating body effect.

## 1. Introduction

In recent years, poly-Si TFTs have drawn a strong attention for the applications to peripheral circuits in active matrix liquid-crystal displays (AMLCD) and to three-dimensional integration in advanced silicon MOSFET process. To achieve higher speeds and circuit densities, it is necessary to scale down the device dimension. However, similar to partially-depleted SOI devices, small-dimension poly-Si TFTs suffer from severe kink effects due to the presence of floating body. Holes generated by avalanche multiplication effect accumulate in body and thus raise the body potential, accordingly turning on the parasitic BJT [1]. To eliminate the floating body effect, it is desirable to decrease the drain electric filed and to minimize the body neutral region. Devices with thin channel and thick drain region are reported to effectively suppress the kink effect [2, 3, 4, 5]. However, previous structures are complex and the fabrication processes are not compatible with conventional AMLCD process, limiting their applications seriously.

In this paper, a novel W-raised source/drain poly-Si TFT (W-TFT) with ultrathin channel was proposed. Thick source/drain region was fabricated by selective deposition of W film on exposed poly-Si area. The deposition temperature is only 300 ºC and no other annealing process is needed. Due to the self-limiting property of the selectively W growth, the Si consumption is less than 200 Å. Therefore, the contact resistance can be kept low since the 300 Å channel film is not fully consumed.

## 2. Device Fabrication

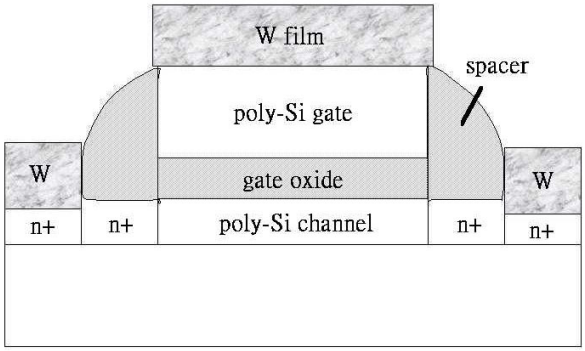


Figure 1. The schematic cross section of the new W-TFT

The schematic cross section of the new W-TFT is shown in Fig. 1. Fabrication processes of the new W-TFT are as follows: A 30-nm-thick amorphous silicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 ºC. Devices with 50-nm-thick channel are also fabricated for comparison. After active region patterning, a 60-nm-thick TEOS oxide was deposited by LPCVD, followed by 950 ºC 20 sec rapid thermal annealing (RTA) to densify oxide. Then a 300-nm-thick a-Si layer was deposited by LPCVD to serve as the gate electrode. The a-Si layer was recrystallized by solid phase crystallization (SPC) at 600 ºC for 24 hr. The poly-Si gate was then defined by reactive ion etching (RIE). After removing oxide on the source/drain region by HF dip, the device was implanted by phosphorus at a dose of 5E15 $cm^{-2}$. Afterwards, a 200-nm spacer was formed around the gate electrode by depositing TEOS oxide layer and subsequently etching back. Gate and source/drain regions were activated by RTA at 750 ºC for 20 sec. Since the poly-Si gate and source/drain regions were exposed without oxide capping, W film can be selectively deposited onto these areas.

The selective W-CVD system is ERA-1000 of ULVAC co.. Selective deposition was carried out by

$SiH_4$ reduction reaction ($WF_6/SiH_4$=20/6) at 300 ºC. Conventional oxide-spacer devices without W films were also fabricated as control samples. They use 500-nm-thick Al films sintered at 400 ºC for 30 min as metal pads.

To improve device performance, $NH_3$ plasma generated by plasma enhanced CVD (PECVD) at 300 ºC for 1 hr is used to reduce trap density and to enhance interface quality. It is found that W film around source/drain will block $NH_3$ molecules from entering channel region. Therefore, plasma treatment is applied to W-TFTs before W deposition. Passivated dangling bonds are stable during W deposition since the process temperature is 300 ºC, the same as the plasma temperature.

## 3. Results and Discussions

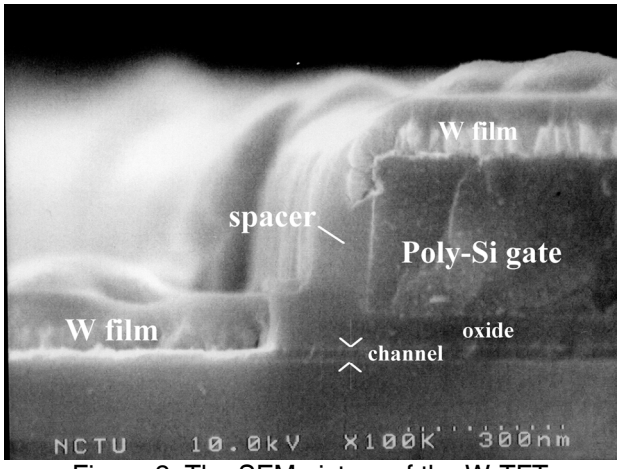


Figure 2. The SEM picture of the W-TFT

Fig. 2 shows the SEM picture of the W-TFT. The thickness of W film is about 120 nm. It is observed that the W film is divided into two layers, the lower one acts as the seed layer that has smaller grain size than the upper layer. Poly-Si source/drain regions are consumed with W, but the consumption is limited to 10-20 nm.

$I_D$-$V_D$ characteristics of W-TFTs and conventional TFTs are compared in Fig. 3. It is obvious that W-TFTs have larger ON current than the conventional ones, especially under large gate voltages. When $V_G$ increases every 3 volts, drain-current spacing of conventional TFTs is almost the same while that of W-TFTs increases gradually. In addition, at low $V_D$, drain currents of W-TFTs saturate more rapidly than those of conventional ones. This reveals that large source/drain resistance dominates characteristics of conventional TFTs when channel thickness scaled down. W-TFTs, on the contrary, successfully resolve this problem and have improved output characteristics.

Except improved ON current, W-TFTs also have good $I_D$-$V_G$ characteristics compatible with conventional ones as shown in Fig. 4. Typical parameters are listed and compared in Table 1. Excellent subthreshold swing denotes good interface quality. Acceptable leakage current validate the practical application of W-TFTs. However, it is worthy to note that plasma passivation before W deposition is essential to achieve good device performances. Fig. 5 compares the $I_D$-$V_G$ characteristics of W-TFTs with plasma treatment of (a) 1 hr before W deposition, and (b) 1 hr after W deposition. Obviously case (a) has smaller $V_{TH}$ and improved subthreshold swing than case (b). This represents that only passivation prior to W depostion is effective to reduce oxide/channel interface states.

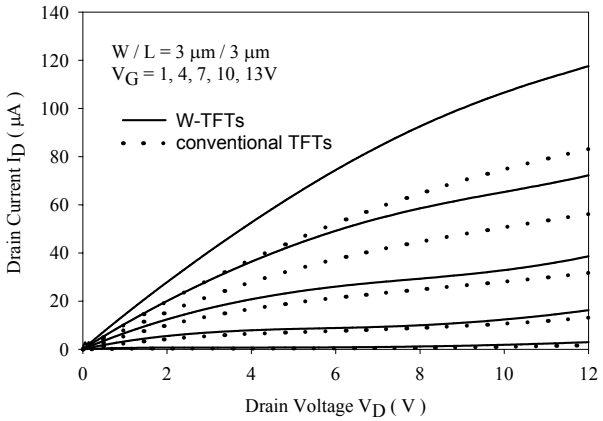


Figure 3. The $I_D$-$V_D$ characteristics of small-dimension W-TFTs and conventional TFTs

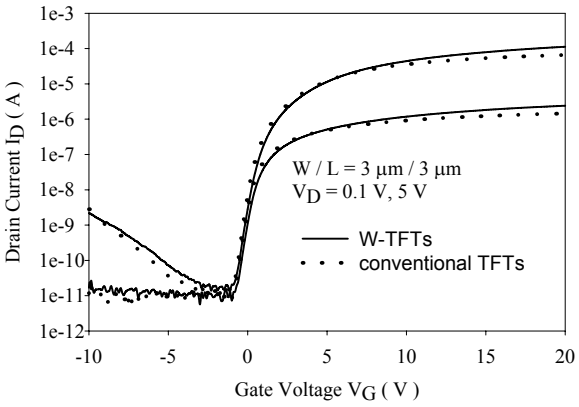


Figure 4. The $I_D$-$V_G$ characteristics of small-dimension W-TFTs and conventional TFTs

Table 1. Typical Parameters of W-TFTs and conventional TFTs ( W/L = 3μm/3μm )

| | W-TFTs | Conventional TFTs |
|---|---|---|
| Vth ( V ) at $V_D$ = 5V | 0.8 | 0.6 |
| S.S.(V/decade) at $V_D$=0.1V | 0.47 | 0.67 |
| On/Off ratio at $V_D$ = 5V | $8\times10^6$ | $2.4\times10^6$ |

W-TFTs with LDD implantation (phosphorous, 1E14 $cm^{-2}$) of different channel thicknesses are also fabricated. Fig. 6 depicts $I_D$-$V_D$ characteristics of LDD W-TFTs with different channel thickness. Devices with 50-nm-thick channel have more profound kink effects than those with 30-nm-thick channel, verifying previous discussions about suppressing floating body effect by reduced channel thickness.

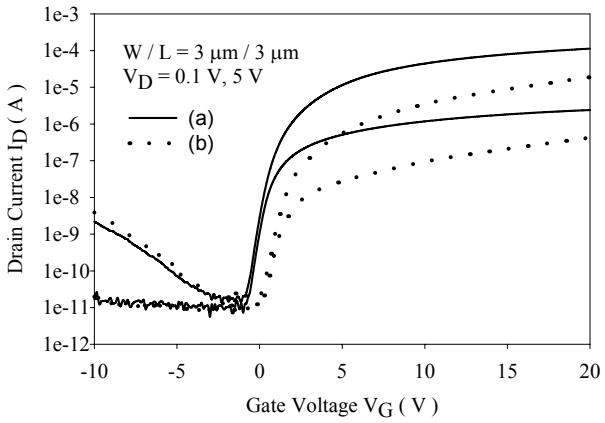


Figure 5. The $I_D$-$V_G$ characteristics of W-TFTs with (a) plasma treatment before W deposition and (b) plasma treatment after W deposition

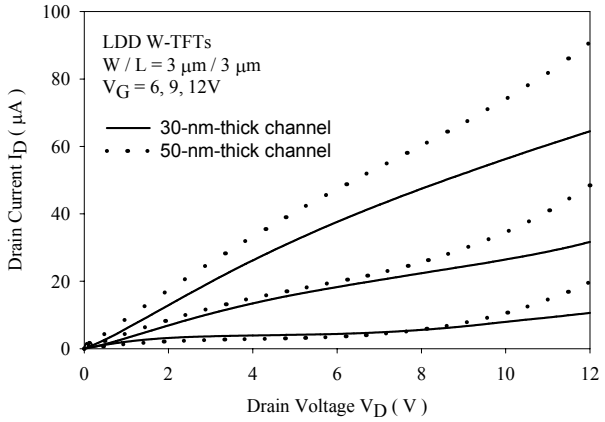


Figure 6. The $I_D$-$V_D$ characteristics of LDD W-TFTs with different channel thickness

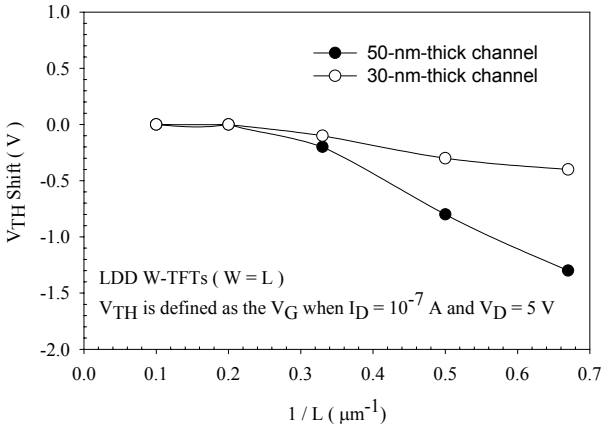


Figure 7. The relation between threshold voltage and the reverse of channel length 1/L for LDD W-TFTs with different channel thickness

The threshold voltages ( $V_{TH}$ ) roll off caused by short channel effects are also studied for LDD W-TFTs with different dimensions. Fig. 7 shows the relations between $V_{TH}$ shift and the reverse of channel length ( 1/L ). It is well known that linear relation between $V_{TH}$ shift and 1/L implies that the short channel effects are dominated by charge-sharing model. This explains the behaviours of devices with 30-nm-thick channel in Fig.7. Devices with 50-nm-thick channel, however, have curved relation that indicates the occurrence of avalanche multiplication and accordingly the floating body effect [6].

## 4. Conclusions

In this paper, we describe the characteristics of novel small dimension W-TFTs with ultrathin channel. The new devices have successfully decreased the source/drain resistance and improved the turn-on current while compared to conventional oxide-spacer counterparts. It is also verified that W-TFTs with ultrathin channel effectively suppress the short channel effects as dimension scaling down. To passivate oxide/channel interface states of W-TFTs, plasma treatment prior to W deposition is essential to improve device characteristics.

## 5. References

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