

Variable-Gain Inversion Layer Emitter Phototransistor in CMOS Technology

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Abstract

The vertical bipolar phototransistor in CMOS technology employing the inversion emitter concept has been analysed by simulation and experiment. It is found that the inversion emitter substantially increases current gain, particularly at low current levels, which yields to a high output photo-currents. In addition, current gain and photo-current magnitude can be controlled by the external gate voltage which has potential for number novel applications.

1. Introduction

A Vertical Bipolar Photo Transistors (VBPT) implemented, for example, in several CMOS image sensors usually suffer from poor photo-current gain [1]. It stems from the low emitter efficiency of shallow metal-contacted VBPT emitters (source/drain diffusions) and high base recombination because of the large extrinsic base area (N- or P-well). In this paper, we describe a novel pnp VBPT structure featuring high gain of the extremely low photocurrents with optional voltage controlled gain.

2. Device structure and simulation

Fig.1 shows the cross-section of pnp VBPT structure generated by process simulation of 0.5 μm N-well CMOS technology using TCAD software ISE¹. Note that the entire extrinsic base surface area is covered by MOS gate self aligned to the P+ emitter and N+ base contact diffusion. Also, gate-to-emitter area ratio is very high (5/0.25) as in standard phototransistors. The PMOS threshold voltage V_{th} of -0.7V is achieved in simulation by usual counter doping Nwell with BF2 ions. The VBPT in Fig.1 can operate in normal mode for $V_g < V_{th}$, or in the inversion emitter mode for $V_g > V_{th}$. Namely, it has been already shown that under the forward biasing of the inversion layer/substrate pn junction, the injection of

minority carriers from the inversion channel occurs [2],[3].

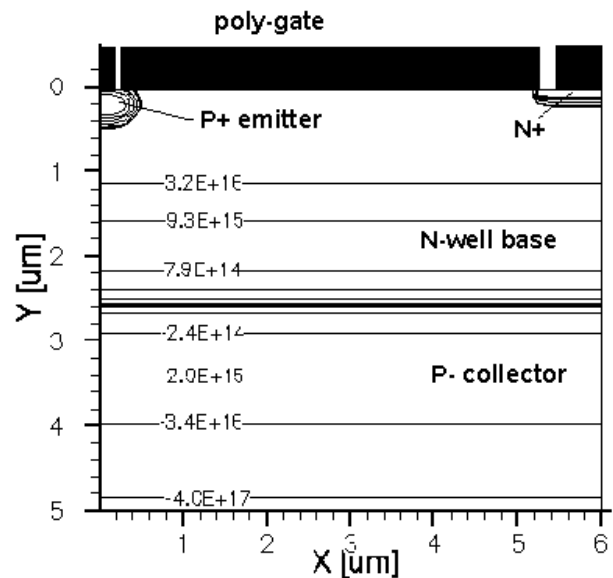


Figure 1 .Cross-section of the pnp VBPT structure generated by 2D process simulation.

In order to confirm this effect, we have simulated a hole distributions in N-well of VBPT for $V_{be}=0.7\text{V}$ and $V_g=0\text{V}$, -1V and -1.5V. The resulting distributions are shown in Fig.2. They clearly indicate the inversion layer injection for negative V_g . In addition, results in Fig.2 show that more holes are injected for more negative V_g , indicating that injection efficiency and current gain increases with decreasing V_g . The inversion emitter improves the overall β of VBPT for two reasons: first, the inversion emitter efficiency is inherently higher than shallow diffused emitter [4] and, second, the presence of MOS inversion layer decreases the total base current by eliminating minority carrier surface recombination in the channel area [3]. The net effect is a substantial improvement of β at low current levels in spite of the large VBPT area.

¹ The authors are grateful to Swiss Cooperation Office in Belgrade for supporting this research by donating commercial TCAD software ISE.

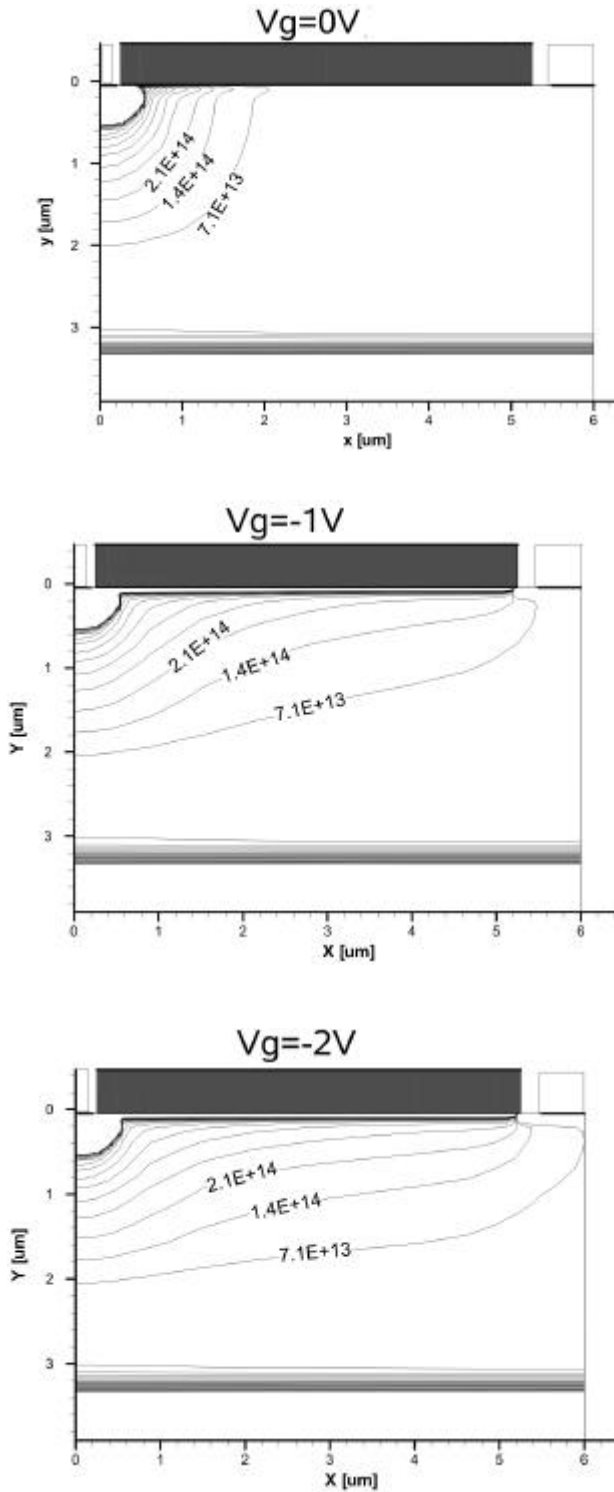


Figure 2. 2D Simulation of hole distribution in N-well base for various V_g with $V_{be}=0.7V$ and $V_{cb}=0V$.

Using the optical beam simulation option of ISE, we have also analysed the photocurrent generation in VBPT. Fig.3 shows simulated open-base photocurrents I_{ph} versus V_g dependences for two monochromatic beam wavelengths $\lambda=0.8\mu m$ and $\lambda=0.5\mu m$ using the same relative beam flux intensities (1:0.4:0.2) in both cases. In

simulation, the emitter contact was biased with $+1.2V$ while the collector contact was grounded. Fig.3 shows the order of magnitude increase of I_{ph} for both wavelengths when VBPT operates in the inversion emitter mode owing to higher β .

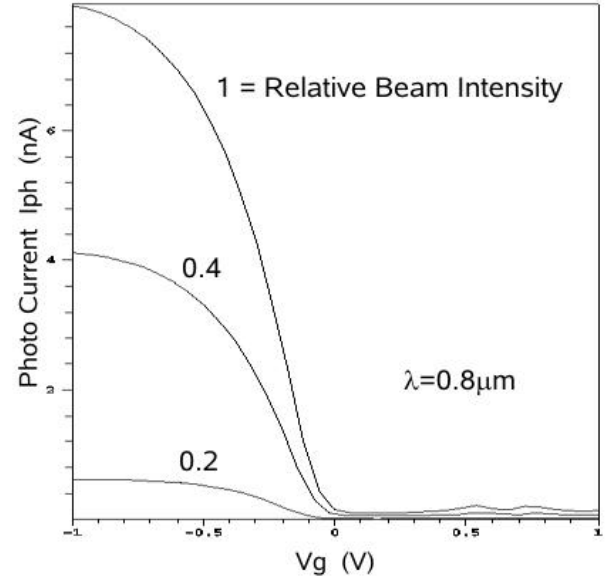


Figure 3. Simulated VBPT photo-current I_{ph} versus V_g for different monochromatic beam intensities.

3. Experimental results

In order to verify simulated results, an array of pnp VBPTs has been realized in three-metal single-poly $0.5\mu m$ N-well CMOS through MOSIS (USA). The photomicrograph of several VBPTs is shown in Fig.4, where one may see a large ($6\mu m \times 36\mu m$) rectangle poly-gate with minimal P+ diffused emitter in the middle.

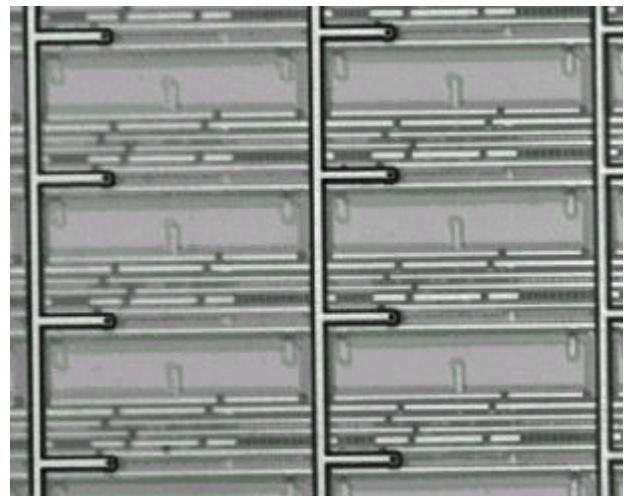


Figure 4. Microphotograph of six VBPTs on the chip.

The P+/N+ implantation mask mirrors at the poly-gate active area which was the only lay-out design role violation. Fig.5 shows the measured $\beta(I_c)$ characteristics extracted from Gummel plot.

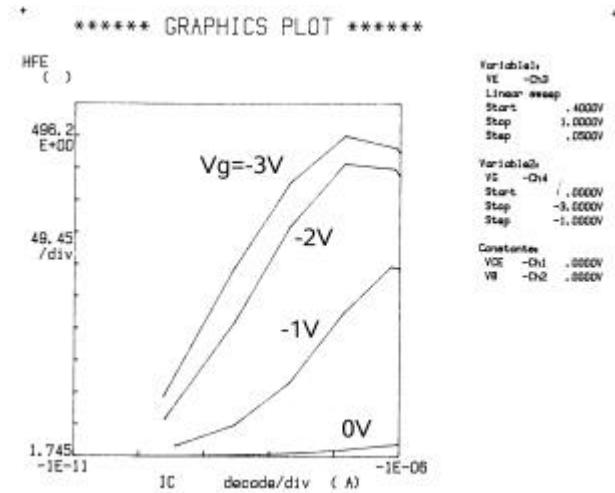


Figure 5. Graphics plot of measured VBPT current gain versus $\log(I_c)$ for various V_g .

Note the order of magnitude increase of β in the low current level region (around 0.1nA) for $V_g = -3V$, indicating the high efficiency of the inversion emitter. Finally, Fig.6 shows the measured photocurrent I_{ph} versus V_g dependences for various light intensities. During the measurements, an open package with mounted chip faced a with board illuminated by constant diffused light. Kodak Wratten neutral gelatine filters were used to vary the light intensity. The resulting behaviour of the experimental and simulated $I_{ph}(V_g)$ curves from Fig.3 and Fig.5 agrees well.

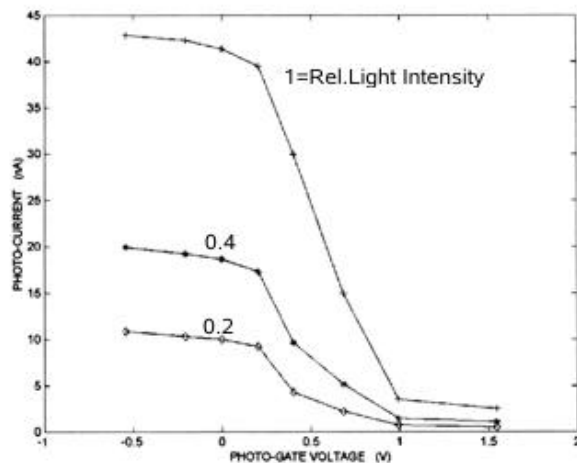


Figure 6. Experimental photo-current versus photo-gate voltage for different light intensities.

4. Conclusions

A novel inversion emitter bipolar phototransistor structure in CMOS technology has been investigated. Results from 2D process and device simulation has indicated high current gain owing to a high injection efficiency of the inversion emitter. This is also confirmed by measuring the experimental pnp inversion emitter phototransistor realized in 0.5um CMOS process. Due to the large variation of current gain with gate voltage, this photo-transistor device has potential as electronic shutter in image chips with appropriate photo-current thresholding. Similarly, it can becomes an efficient light beam selector if it's gain control is synchronized with specific beam appearing frequency.

5. References

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