An Ultra-Thin Polycrystalline-Silicon Thin-Film Transistor with SiGe Raised Source/Drain

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Abstract

An ultra-thin poly-Si thin film transistor (poly-Si TFT) with SiGe raised Source/Drain (SiGe RSD) was fabricated. The raised source and drain regions were selectively grown by ultra-high vacuum chemical vapor deposition (UHVCVD) at 550℃. The resultant transistor has an ultra-thin channel region with thickness of 20 nm and a self-aligned thick S/D region, which leads to better performance. With this structure, the turn-on current in the I-V characteristics increases dramatically and the drain breakdown voltage is increased as well, compared with conventional thin-channel poly-Si TFTs.

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are attractive for many applications, such as the switching devices as well as peripheral driving circuits in the active matrix liquid crystal display (AMLCD) [1], [2]. In order to integrate peripheral driving circuits on the same glass substrate, both a large current drive and a high drain breakdown voltage are necessary for poly-Si TFT device characteristics. There were papers indicating that thinning the active channel film is beneficial for obtaining a higher current drive [3-5]. However, the use of thin active channel layer inevitably results in poor source/drain contact and large parasitic series resistance. In addition, the short-channel poly-Si TFTs also suffer from a low drain breakdown voltage, which cannot meet the driving requirement for the thin active channel devices. An ideal TFT device structure should therefore consist of a thin active channel region, while maintaining a thick source/drain region. The thick source/drain region has the advantage of not only reduction of the lateral electric field near drain side, thus maintaining the drain breakdown voltage [6], [7], but also reduction of the source/drain series resistance. However, previous methods [6-7] used to fabricate such structures with thin active channel and thick source/drain region require one or more additional masks, and are not self-aligned in nature, when compared to the conventional TFTs.

In this experiment, a novel TFT with self-aligned SiGe raised source/drain structure is proposed. The new device characterizes a thin active channel region and a thick SiGe source/drain region. The raised source/drain region is self-aligned to poly-gate and no additional mask is needed in comparison with conventional TFTs. Comparison of experimental I_d-V_g characteristics, on/off current ratio, and breakdown voltage for the proposed novel structure and conventional thin-layer TFTs are reported.

2. Experimental

The key fabrication steps of the proposed SiGe raised Source/Drain device are shown in Figure 1. Silicon wafers coated with a 500nm thermal oxide were used as the starting substrates. A 20nm undoped ultra-thin amorphous-Si (a-Si) layer was deposited by low-pressure CVD (LPCVD) at 550°C. The deposited a-Si

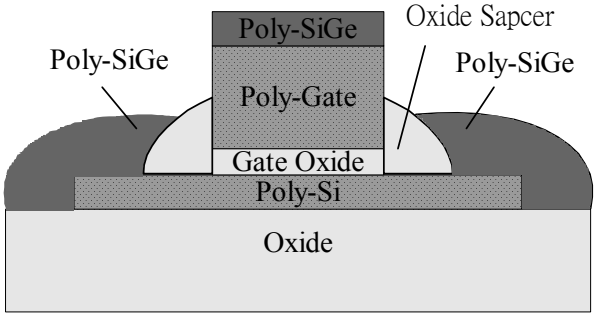

Figure 1. Key process steps with cross-sectional schematic for SiGe raised S/D poly-Si TFTs.

layer was then recrystallized for 24 h in nitrogen ambient at 600°C. After patterning and plasma etching to form the active device island, a 50 nm gate oxide was deposited by plasma-enhanced CVD (PECVD) at 300°C. This was followed by the deposition and patterning of a 300 nm poly-Si gate layer. A 300 nm TEOS oxide was then deposited by PECVD, and anisotropically etched by reactive ion etching (RIE) to form a sidewall spacer abutting the poly-Si gate. The remaining TEOS oxide above the source and drain regions was removed in diluted HF to ensure the exposure of the S/D poly-Si region. Afterwards, some wafers were loaded into a UHVCVD system to selectively grow an undoped SiGe layer on the exposed source, drain and gate regions at

550°C. The growth of SiGe on source, drain and gate regions was inherently self-aligned. The thickness of the SiGe was about 100 nm. Figure 2 shows a cross-sectional TEM photo of the fabricated structure. Next, the gate electrode and source/drain regions were implanted by phosphorus ions at a dosage of $5\times10^{15}cm^{-2}$, and an energy of 55 keV. For comparison, wafers with conventional TFTs were also processed on the same run by deliberately skipping the growth of SiGe and using a phosphorus implant energy of 15keV instead. All wafers were then subjected to a RTA anneal at 850°C for 20 seconds for dopant activation. The measured resistivities were 2×10^{-3} Ω-cm and 4.6 Ω-cm for SiGe raised S/D and conventional TFTs, respectively, indicating that a significant reduction in S/D resistance was indeed obtained by using a thicker S/D film. Next, a 300 nm-thick oxide was formed as the cap layer by PECVD. Finally, contact hole definition and Al metallization were performed, followed by a 400°C sintering in nitrogen ambient for 30 minutes.

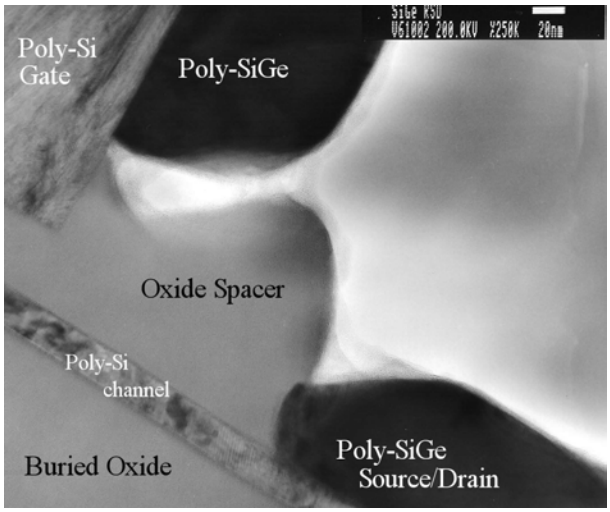

Figure 2. Cross-sectional transmission electron microphotograph (TEM) of a fabricated SiGe raised S/D TFT. The thickness of the SiGe on source/drain region is approximately 100 nm.

3. Results and Discussion

Figure 3 shows the comparison of typical I_d-V_g characteristics for the conventional and the proposed SiGe raised S/D TFTs. It can be seen that the turn-on characteristics are significantly improved for SiGe raised S/D TFTs. Approximately one order of magnitude improvement in the on/off current ratio is observed for SiGe raised S/D TFT, as compared to the conventional TFTs. The larger leakage current for conventional TFTs is probably due to the stronger horizontal electric filed near drain side, which results in smaller breakdown voltage for conventional TFTs, as will be discussed later.

Figure 4 depicts the output characteristics for both SiGe raised S/D and conventional TFTs. It can be seen that for the conventional TFTs, as the gate voltage gets higher, the I-V curves behave more like resistance. The total resistance (R_{total}) from drain to source is a composition of source/drain ($R_{S/D}$) and channel ($R_{channel}$) resistance, which can be expressed as the following equation:

$$R_{total} = 2R_{S/D} + R_{channel.}$$

With the ultra-thin source/drain region, the conventional TFT suffers from a high $R_{S/D}$. So when the gate bias increases, the output current is subject to be limited by the source and drain resistance ($R_{S/D}$), as shown in Figure 4. In contrast, due to its thick source/drain region, the $R_{S/D}$ is much smaller for SiGe-RSD TFT. As a result, the output current is not limited by the parasitic source/drain resistance, and therefore is much larger than that of the conventional TFT.

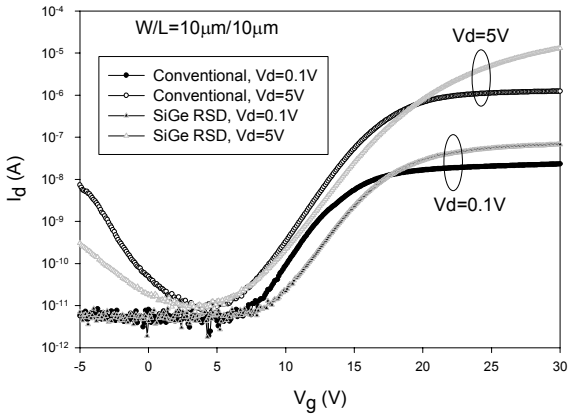

Figure 3. Comparison of I_d-V_g characteristics of SiGe raised S/D TFTs and conventional poly-Si TFTs

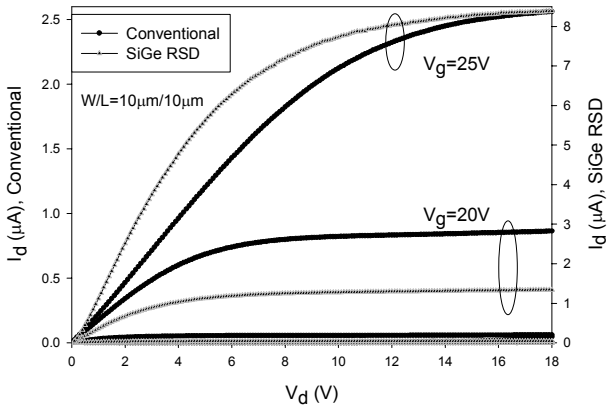

Figure 4. Comparison of I_d-V_d output characteristics of SiGe raised S/D TFTs and conventional poly-Si TFTs.

The scaling of channel dimensions in poly-Si TFTs is critical to realize high density AM-LCD with integrated driver circuits on the same glass panel. To this end, the drain breakdown voltage requirement must be satisfied. Figure 5 shows the drain breakdown voltage, which is defined arbitrarily as the drain voltage when the drain current equals 2 nA with V_{gs} = 5V, for both the conventional and SiGe-RSD TFTs. It can be seen from Figure 5 that for mask length (L_g) changing from 10 μm

to 1 μm, the breakdown voltage for conventional TFTs decreases from 10.7 V to 5.3 V (50%), while only 12% of difference (from 16.1 V to 14.2 V) in breakdown voltage is observed for SiGe RSD TFTs. The larger breakdown voltage for SiGe-RSD TFTs can be attributed to the thicker source/drain region and hence smaller horizontal electric field near the drain side [4], [5]. This result is also consistent with the larger leakage current observed in Figure 4 for conventional TFTs with L_g = 10 μm.

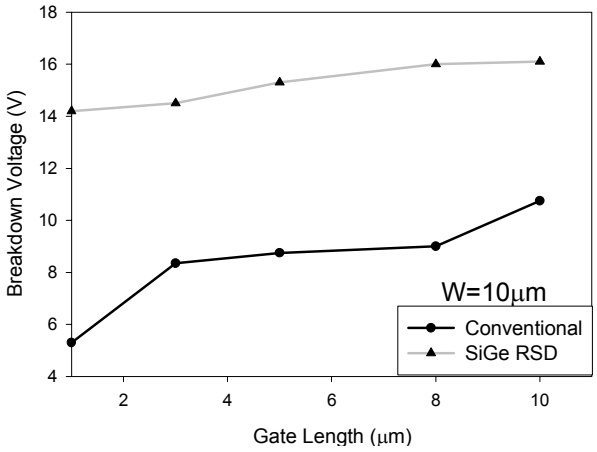

Figure 5. I_d-V_g curves as a function of different gate length (L_g) from 10 μm to 1 μm for conventional TFTs and SiGe raised S/D TFTs.

4. Conclusion

We have proposed an ultra-thin poly-Si TFT with self-aligned SiGe raised source/drain structure. The proposed structure was successfully fabricated without additional masks and is self-aligned in nature. Our experimental data show that the new SiGe raised S/D poly-Si TFT has higher turn-on current and on/off current ratio in comparison with the conventional TFTs. Moreover, the drain breakdown voltage for SiGe raised S/D poly-TFTs is significantly improved for smaller gate length. The new structure is therefore ideally suitable for implementing high-density and high-performance driver circuits on the glass panel for AM-LCD applications.

5. References

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