A Novel MEMS Technological Platform Aimed at RF Applications

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Abstract

A novel MEMS technological platform for RF passive components, namely RF MEMS switches, tuneable capacitors and high-Q suspended inductors, is reported. The proposed process employs a metal (Al, AlSi or Cu) as active movable layer and amorphous silicon or polycrystalline silicon as sacrificial layers, providing multi-air-gaps. Various types of substrates like bulk silicon and SOI can be used. Full dry releasing of suspended beams and membranes is performed with SF_6 or XeF_2, with unrivalled yield/reproducibility compared with any other wet etching techniques. The platform is used to validate new MEMS architectures and concepts, such as the suspended-gate MOSFET that can serve as both RF capacitive switches and tuneable RF capacitors.

1. Introduction

The end of the 20th century brought major changes in the radio-frequency (RF) technology, [1, 2]. The exponentially growing interests in mobile communications and networking of information have provided new challenges, with particular emphasis on more affordable and integrable technologies able to provide superior RF functionalities per unit of volume. Immediate impact has been observed on the research and development of silicon-based RF integrated circuits (ICs) with special emphasis on sub-micron silicon CMOS, SOI and SiGe heterojunction bipolar transistors (HBT's). New technologies have also emerged, stimulated by the potentially enormous markets. One of these is the micro-electro-mechanical-systems (MEMS) technology. Ironically, first developments in RF MEMS originated from requirements in airborne systems even if now the telecom mass market is the main driver of this field.

MEMS are the merger of the IC world with the micron-scale mechanical world. Conventional IC fabrication techniques stand along with more exotic chemical and mechanical processes, in order to provide the MEMS. MEMS devices are extremely attractive for RF ICs (especially wireless) because of their gains in terms of: (i) device and system miniaturisation (lower costs), (ii) integration (same planar technology to manufacture ICs), (iii) power savings (low power operated devices), (iv) higher performances (such as high-Q for passive devices) and (v) new integrated functionalities (like programmable or tuneable passive devices, resulting in programmable/tunable RF ICs).

In this paper, a novel MEMS technological platform aimed at RF applications is proposed. Various architectures such as: RF switches (contact and contactless), high-Q MEMS capacitors and high-Q inductors with and without programmable and/or tunable characteristics together with their performances are envisioned and, some of them, are demonstrated.

2. Novel Full Dry Micromachining Process with Sacrificial Silicon for Multi-Air Gaps

Conventional, largely accepted techniques for releasing suspended MEMS structures are: (i) standard polysilicon surface micromachining process, which involves a silicon dioxide sacrificial layer wet etch and a supercritical carbon dioxide drying process [3] and (ii) organic sacrificial layers released in oxygen plasma [4,5]. The fabrication process reported in this paper is in *total contrast with these processes.*

In the following, EPFL's surface micro-machining process developed for suspended-metal devices architectures with multi-air gaps (that can define more functional devices with suspended membranes) aimed at RF applications is described. It is called *full-dry* because all the steps involving etching processes (releasing of the membrane included) are essentially dry. These steps are carried out in inductively coupled plasma (ICP) reactors. Moreover, the reported fabrication process is fully compatible with CMOS post-processing. It follows that a key limitation of thermal budget, in order not to degrade the performances of underlying integrated circuits, is a systematic concern.

Fig. 1 depicts the simplified successive steps of the MEMS process with Al (AlSi) and two air gaps. First a silicon dioxide layer (with a thickness around 0.5μm) is grown in a wet atmosphere as shown in Fig. 1a. A low temperature oxide (LTO) deposited by LPCVD can replace the wet oxidation. Note that silicon-on-insulator (SOI) substrates are a preferable alternative for RF applications (that need high resistivity substrates). The second step of the process consists in metal layer (M1) deposition, Fig. 1 b: a relatively thick (>1μm) AlSi is sputtered. Using conventional photolithography techniques, the Al base electrodes and the contact pads are patterned by a chlorine-based plasma chemistry, Fig. 1 c. As shown in Fig. 1 d, the structures are then covered by a SiO_2 diffusion barrier layer, the thickness of which is around 50nm. This layer is used to prevent diffusion

between the silicon sacrificial layer and the aluminium base electrodes. Some detailed experiments demonstrated that the surface roughness under the released membrane can be significantly decreased with such a layer. The barrier layer can be obtained by deposition of a SiO_2 layer even by RF sputtering at a temperature of 200°C or by low pressure chemical vapour deposition (LPCVD) low temperature oxide (LTO): SiO_2, phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG). Next step, as shown in Fig. 1 e, is the deposition of an amorphous silicon sacrificial layer (ranging from 0.2µm up to a few of µm). Amorphous silicon (a-Si) can be deposited by different types of techniques such as RF or DC sputtering and plasma enhanced chemical vapor deposition (PECVD).

The patterning of amorphous silicon sacrificial layer is performed by isotropic SF_6 plasma process. Further photolithographic steps are needed in some cases (as for the RF suspended capacitors and switches) in order to provide a more complex three-dimensional shape of the membrane. One key step consists in *thinning down* the silicon sacrificial layer to define the RF capacitor as shown in Fig. 1 f. A second step consists in passing through the silicon sacrificial layer to prepare the mechanical anchors to the substrate for the suspended membranes. The resulting structure is shown in Fig. 1 g. The patterned sacrificial layer is then covered by a SiO_2 diffusion barrier layer of few tens of nm, Fig. 1 h. The second metal layer (M2) is then deposited onto the surface of the structure. One critical problem is the silicon step coverage by M2 for which various solutions have been identified. Using conventional photo-lithography, the Al membrane and the suspension beams are then patterned by chlorine-based plasma chemistry, Fig. 1 i. Next step is the patterning of the diffusion barrier layer via dry etching technique with C_xF_y RIE plasma (to give an access to silicon sacrificial layer).

Finally, the suspended metal membranes are released by dry etching of the silicon sacrificial layer in a fluorine-based chemistry with a high selectivity to SiO_2 and Al (releasing with XeF_2 is a process alternative to SF_6), as shown in Fig.1 j. An average under-etch rate of 0.9µm/min for 1µm air-gap and of 1.2µm/min for 2µm air-gap is obtained. Finally (and optionally), the diffusion barrier layer on electric contacts is removed by anisotropic C_2F_6 RIE plasma process. Further experiments are in progress in order to investigate the dependence of the under-etch rate of amorphous silicon with the aspect-ratio.

3. RF MEMS switches and capacitors

Various tuneable capacitor and RF switch architectures were designed, fabricated and characterised in order to validate the new proposed full-dry process. The Design-Of-Experiment (DOE) has included variations of some parameters such as: (i) membrane shape, (ii) membrane size, (iii) number of etch holes, (iv) suspension beams novel architecture.

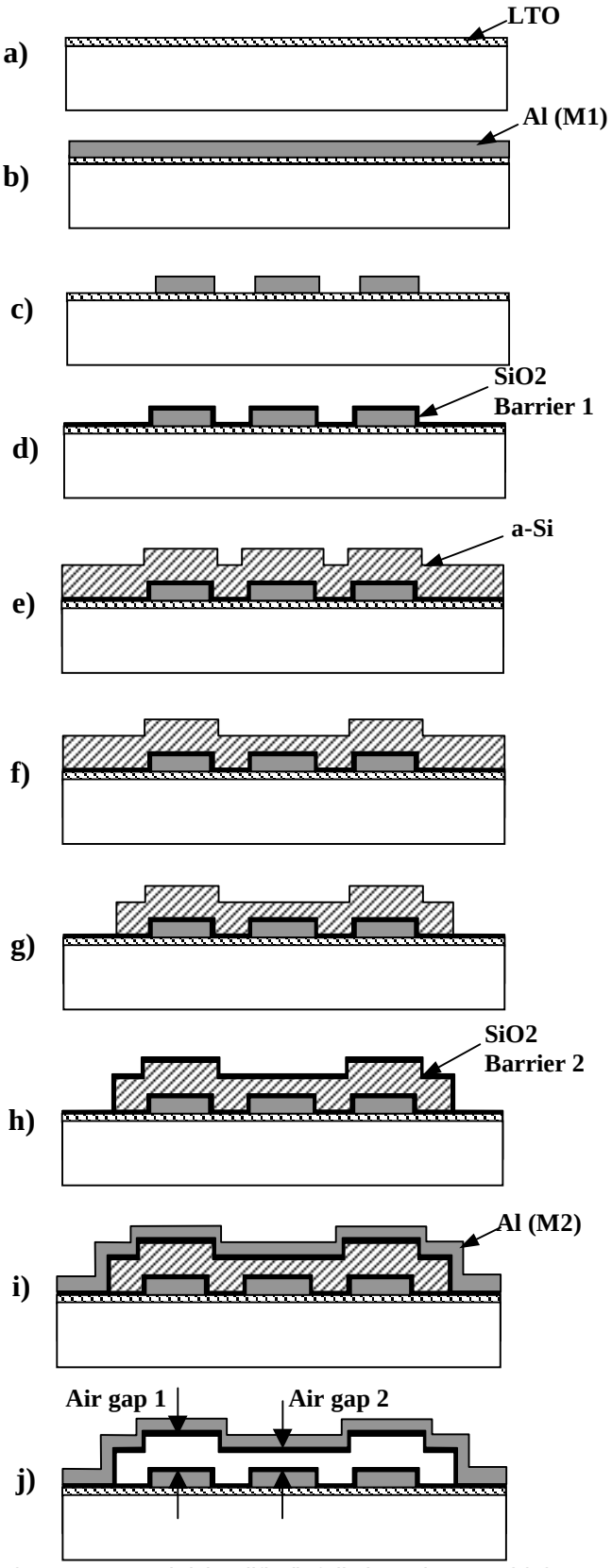

Figure 1. Novel (simplified) full dry micromachining process sequence with metal active layer, sacrificial a-Si and two air-gaps.

The design of tuneable capacitors target aims to CMOS-compatible devices with voltage operation below 5V, high quality factor over wide-band (up to around 10GHz) and a capacitance tuning range in excess of 70%. Fabrication of quasi-identical MEMS capacitor structures on both silicon and Silicon-On-Sapphire (SOS) substrates allows to quantitatively evaluate the RF performance gain in case of highly resistive substrates. Fig. 2 depicts a MEMS capacitor with an array of etch holes (square 2x2μm^2 holes) spaced by 10µm. Using etch holes substantially improve the etchant to access the sacrificial layer and reduces the releasing time. Different meander-like architectures with double or quadruple suspension beams are proposed to reduce the equivalent spring constant (see Fig. 3). The device shown in Fig. 2 corresponds to a single air-gap tuneable capacitor architecture with a surface of 316x316μm^2, 2µm air-gap and 2x2μm^2 etch holes spaced by 10µm. Figure 4 reports a tuneable capacitor with double-air gap [6] (and de-coupled electrostatic operation) resulting in significantly increased tuning range. The dimensions of the square-shaped RF capacitor are: array of 250x250 μm^2, 1µm air-gap and 10x50μm^2 etch holes laterally placed.

Quasi-static capacitance (QS-CV) measurements have been performed using a HP-4156C semiconductor analyser. We demonstrate a tuning range larger than 20% for single air gap metal-metal tuneable capacitors. Complementary extractions of pad capacitance using de-embedding structures and S-parameter measurements, for more accurate bias-dependent capacitance extraction are in progress. Fig. 5 clearly demonstrates the influence of the suspension beams design (with and without meanders, resulting in different equivalent spring constant), on the pull-in voltage that is reduced below 7V by the use of one meander. The leakage current, $I_{leakage}$, is an indicator of pull-in phenomena (key for the use of similar architectures as switches), when non-equilibrium between electrostatic and elastic forces is reached.

4. Suspended-gate MOSFET

The cross section and the principle of the SG-MOSFET are depicted in Figs. 6 a and b: the device combines in a top-down architecture a metal membrane MEMS switch and a MOS transistor. Typical device design is inspired by RF MEMS membrane switches, including suspension arms, is given in Figs. 6 and 7. Its electrostatic operation is as follows: when the gate voltage, V_g, is increased, the intrinsic gate-voltage, V_{gint}, which drives the MOS channel formation, is tuned according to a capacitor divider:

$$V_{g\,int} = \frac{V_g}{1 + C_{gc\,int} / C_{gap}} \qquad (1)$$

where C_{gcint}, C_{gap} are the intrinsic gate-to-channel capacitance of the underneath MOSFET and the air-gap capacitance, respectively. Recently, we have proposed a full analytical model for the SG-MOSFET [7].

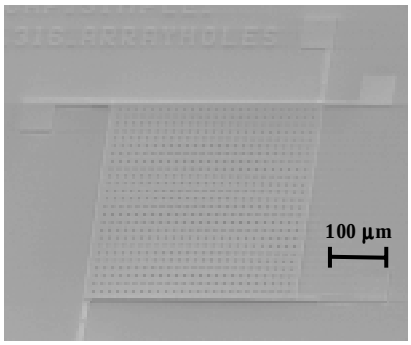

Figure 2. SEM picture of a single air gap tuneable capacitor with a surface of 316x316 μm^2, 2µm air-gap and 2x2 μm^2 etch holes spaced by 10µm.

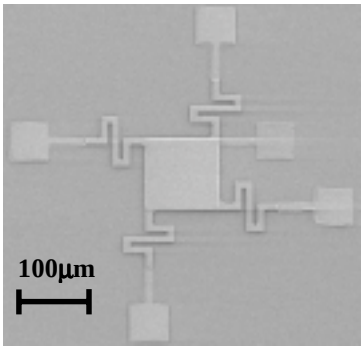

Figure 3. RF MEMS capacitor design with meanders included in the suspension arms.

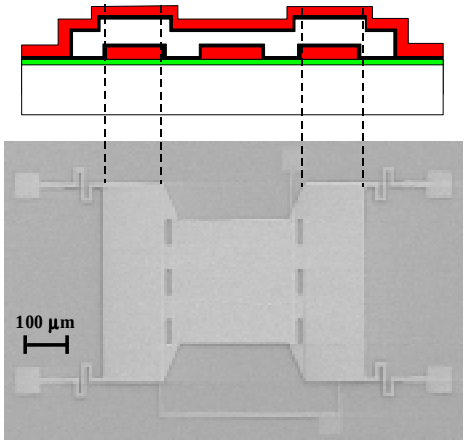

Figure 4. RF MEMS capacitor design with two different air-gaps and improved tuning range.

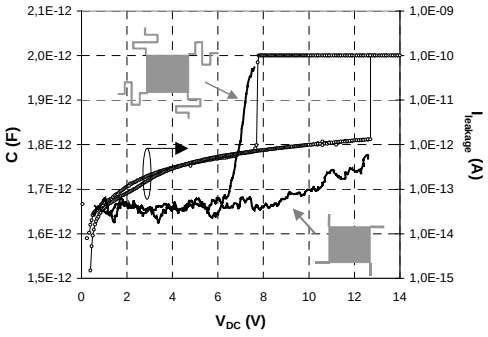

Figure 5. QS C-V of tuneable MEMS capacitors.

It is worth noting that SG-MOSFET membrane moves continuously downwards as long as the equilibrium is maintained between electrostatic and elastic forces:

$$\left|F_{elastic}\right| = kx = \frac{1}{2}\frac{\varepsilon_{air} A (V_g - V_{g\,int})^2}{(t_{gap0} - x)^2} = \left|F_{electr}\right| \qquad (2)$$

where x is the gate displacement, , t_{gap0} the initial air-gap dimension and V_{gint} the intrinsic (or internal) gate voltage. When V_g equals the pull-in voltage, V_{PI}, unstable equilibrium is reached and the switch (suspended membrane) moves from the 'off' to the 'on' state (t_{gap}=0). SG-MOSFET has been investigated with our recent analytical model [7] and optimised architectures have been designed and fabricated. We demonstrate (Fig. 7) that a thin thickness of the gate oxide (<20nm) is essential to provide a high C_{on}/C_{off} ratio (>100), as requested by RF switch applications. Moreover, SG-MOSFET has a *dynamic threshold voltage*, which is high in the *off state* and low in *the on-state*; it follows that it offers improved isolation (in *off state*) for RF capacitive switch applications. A low spring constant (<100N/m), provided by special meander-like hinge design, is needed for <5V actuation of SG-MOSFET. Other key characteristics of SG-MOSFET concern the specific *super-exponential* and *super-linear* drain current dependence on the gate voltage, at low drain voltage and the possibility *to obtain a subthreshold slope better than the theoretical solid-state bulk/SOI MOSFET limit (60mV/decade).*

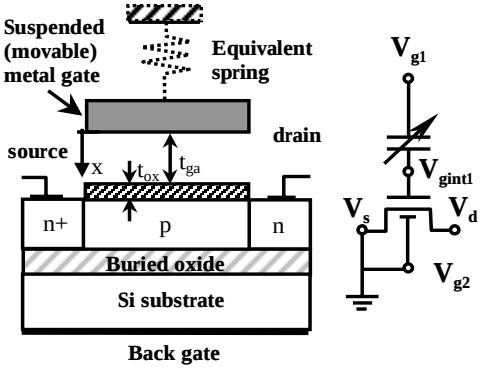

Figure 6. SOI SG-MOSFET: architecture and equivalent circuit with capacitor divider.

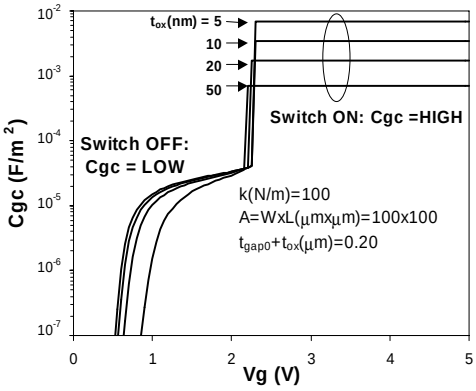

Figure 7. SG-MOSFET C_{gc} vs. V_g, characteristics with the gate oxide thickness as a parameter.

The full-dry EPFL's process reported in Fig. 1 has been specially adapted in order to fabricate *in-CMOS-process* SG-MOSFETs. For the first time, the *polysilicon of a standard CMOS process has been used as a sacrificial layer* in order to define, and, successfully realise, suspended gate devices with metal-over-gate architectures (Fig. 8 a and b).

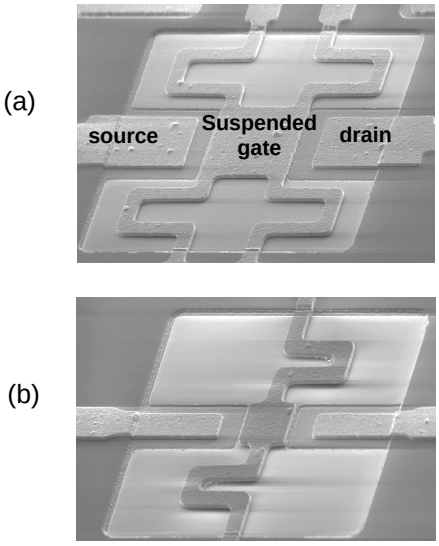

Figure 8. SEM images of two different designs of fabricated metal-over-gate SG-MOSFET.

5. Conclusion

A new surface micro-machining technological platform, dedicated to RF MEMS device architectures with suspended metal membranes, was reported. It employs the dry etching of sacrificial silicon (a-Si or polysilicon) in order to release suspended metal membranes. The process can provide multi-air-gaps for increased functionality and complex design. RF MEMS switches and tuneable capacitors, as well as original suspended-gate MOSFET architectures are reported based on adapted process variations. Further developments include metal membranes for suspended high-Q inductors and other complex 3-D architectures.

7. References

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