LOW PINCH-OFF VOLTAGE AMORPHOUS SILICON JUNCTION FIELD-EFFECT TRANSISTOR: SIMULATION AND EXPERIMENT

D. Caputo, G. de Cesare, F. Lemmi, F. Palma
Department of Electronic Engineering
and INFM-Unità di Roma
Via Eudossiana, 18 00184 Rome
Contacting Author: G. de Cesare
E-mail: decesare@die.uniroma1.it
Fax:+39-064742647
Phone:+39-0644585431

M. Tucci
ENEA Research Center
Portici Località Granatello
80055 (NA) Italy
E-mail: tucci@portici.enea.it

Abstract

In this work, a Junction Field Effect Transistor (JFET) based on amorphous silicon suitable for large area linear application is presented. The drain-source contacts are made on top of the n-layer of a glass/metal/p^+-i-n structure. The channel conductivity can be modulated by a reverse bias applied to the junction, which varies the depletion region width.
The depletion of the n-doped layer, hampered by the high defect density of the doped amorphous silicon material, has been studied by using a one-dimensional finite-difference simulator, which gives the free electron concentration as a function of reverse applied bias, dopant concentration and thickness of the intrinsic layer.
Based on simulation results a JFET with W/L=400 μm /40 μm was fabricated. Transistors with pinch-off voltages around –3.5V and transconductance values of the order of 10^{-7} A/V were obtained. These values are better than state-of-the-art thin-film transistors in similar bias conditions.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) based thin-film transistors (TFTs) are routinely manufactured for flat-panel liquid-crystal displays [1] and for active-matrix sensor arrays [2] on large-area glass substrates. More recently, the interest in flexible substrates has prompted the processing and study of TFTs on plastic materials [3]. Overall performance of these devices tends to remain lower than for glass substrates, but is fairly good if some precautions are taken in the process. In particular, one critical step is the growth of the gate dielectric, typically amorphous silicon nitride. It is generally found that a high quality material is grown only by using relatively high process temperatures (e.g. 300 °C). Lower temperatures result in a more defective silicon nitride layer and possibly in higher defect density at the channel interface. These cause increased gate leakage currents and reduced channel mobility, respectively, besides stability issues.
The device presented in this paper eliminates altogether the gate dielectric issue and appears interesting for applications on plastic substrates. In particular, the device can be designed for analog applications of a-Si:H, where the use of bipolar or MOS transistors, are limited by the very small minority carrier diffusion length or the low channel conductance, respectively.

2. Device structure and operation

Figure 1 describes the structure of an a-Si:H-based Junction Field-Effect Transistor (JFET), whose basic device structure is a p^+-i-n diode. The p^+-layer is contacted by a gate electrode. The n-layer is lightly doped and constitutes the JFET channel. A thin patterned n^+-layer is used to achieve local ohmic contact to the source and drain electrodes. The figure also shows a typical bias configuration used for regular operation.
Like a typical JFET, it operates in depletion mode, which means that a null gate-to-source (V_{GS}) voltage leaves the channel fully conducting. In normal operation, V_{GS} is negative and reverse biases the junction. The effect of the reverse bias is a gradual depletion of the doped layers. The modulation of the free electron concentration in the n-channel controls

the drain-to-source current (I_{DS}) and than the transistor effect.

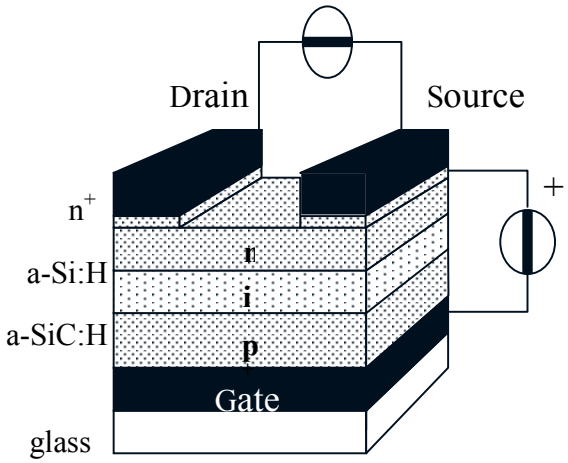

Fig. 1. Junction Field-Effect Transistor structure and typical operation configuration

If the n-channel defect density at the Fermi level is low enough, making V_{GS} more negative at some point causes the depletion region in the channel to reach the drain contact, helped by the positive drain-to-source voltage (V_{DS}). For more negative V_{GS}, a pinch-off operation begins and the edge of the fully depleted zone moves toward the source contact.

3. Depletion simulations

Amorphous silicon doped layers are typically very defective. This may complicate the depletion process and ultimately the JFET correct operation. In fact, a few parameters influence the voltages that need to be used to have it working properly. Here, first some general considerations are made on the implications of the use of particular parameters for the p^+-i-n device layers. Then, one-dimensional numerical simulations based on a finite-difference model of a-Si:H devices [4] are presented, to provide design specifications for a JFET which exhibits correct operation with a few volts for both V_{DS} and V_{GS}.

Intrinsic layer: a thinner i-layer guarantees larger electric field that enhance the depletion process at low voltages. This can ease the channel modulation and improve the JFET transconductance g_m. The high electric field also increases the reverse junction leakage currents [5, 6] and may need to be taken into account, depending on the application. In any case a high-quality intrinsic layer is desirable since it has less trapped charge. It both does not screen much the electric field and provides low gate leakage currents.

n-layer: a thicker n-layer is more conductive at any given V_{GS} and helps to obtain a large g_m. In fact, unlike the case of TFTs, in JFETs the actual channel thickness is not limited to thin accumulation layer and can be relatively large. However, it takes larger fields to fully deplete a thick n-layer, increasing the pinch-off voltage. The doping level also needs to be the result of a tradeoff. High doping levels guarantee high conductivity and large g_m values. However, they induce a large defect density in the layer, which can complicate or even practically forbid an effective depletion process. In this case in particular, numerical simulations are an extremely useful design tool.

p^+-layer: it needs to be thick enough not to fully deplete in the whole expected range of device operation. The chosen strongly p-doped amorphous silicon carbide layer, with a large density of gap states, allows a relatively low thickness to be safely used.

The simulations results that follow are meant to quantitatively address the effect of the doping level of the n-channel and of the thickness of the intrinsic layer. The n-channel thickness is kept constant to 1500 Å. The gap density of states has been chosen simple, with band tails (conduction bad tail temperature of 350K and valence band tail temperature of 500K) and acceptor/donor deep defect distribution ($8.85*10^{17}$ $cm^{-3}eV^{-1}$ at 0.91 and 0.81 eV respectively). The electron mobility is assumed to be 1 cm^2/Vs.

Figure 2 shows the electron concentration n along the JFET thickness in all the three layers, the n-channel first. The edges of the 3200 Å-thick i-layer are marked by two solid lines. Results are shown for three values of the bias voltage V_{BIAS} across the p^+-i-n junction. They point out that a concentration of dopant atoms of 10^{18} cm^{-3} is the highest possible to still guarantee a distinct modulation of n with such small bias voltages. Evidently, in the JFET three-dimensional real structure, the actual value of V_{BIAS} on the junction is given by the difference between the gate voltage and the channel potential at each position along the channel itself.

These results yield a clear quantitative design constraint and ultimately determine the ratio of the gas species in the process chamber when the n-channel is grown.

We have also investigated the effect of different i-layer thickness on the electron concentration in the channel region. In the simulation, the doping level has been kept set to the value extracted above of 10^{18} $atoms/cm^3$. It must be noted that only a fraction of the 10^{18} cm^{-3} dopant atoms is introduced in lattice sites

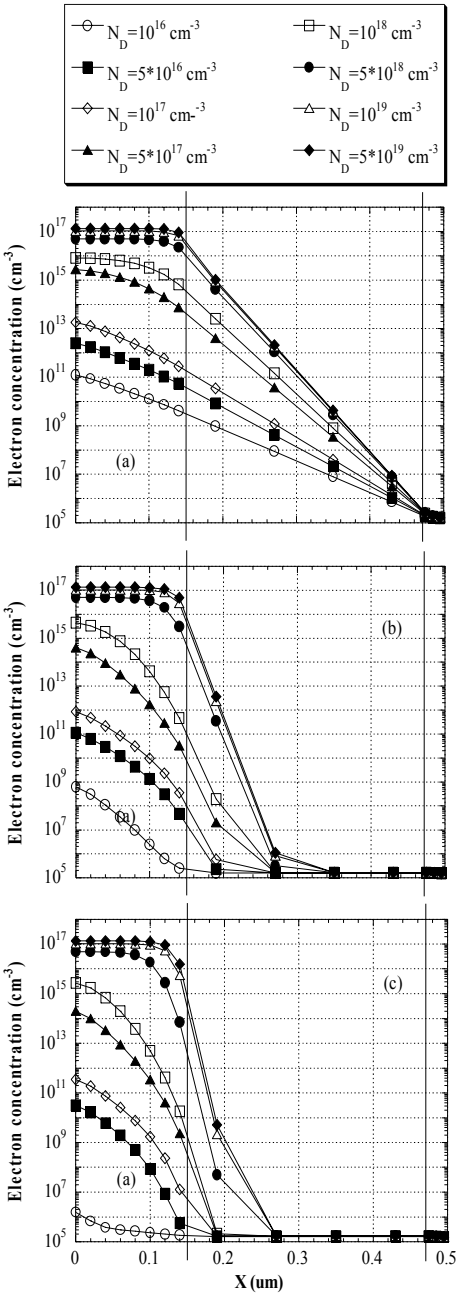

Fig. 2. Electron concentration along the JFET thickness. V_{BIAS} = 0 V (a), -1V (b), -2V (c). Results for several doping levels are reported.

and only a fraction of the electrons set free by these will actually be available for conduction, due to the presence of trap states.

As expected, we found that the thinner the i-layer the more effective the depletion process. In particular, a 8000 Å-thick intrinsic layer strongly reduces the modulation of the channel carrier density, making it practically unsuitable for low voltage operation.

However, a very thin (e.g. 400 Å) i-layer would cause very large leakage currents due to field enhancement of thermal emission of carriers and would probably affect the manufacturing yield. Therefore, an intermediate (e.g. 3200 Å) thickness can be chosen for the design of a robust and properly working JFET. The results prove that with a few Volts of applied bias a full depletion of the channel can be obtained, to guarantee a correct operation of the JFET. Simulations in fact yield the Fermi level position in the channel energy gap. As consistent with a relatively low effective doping level, the Fermi level stays relatively deep between 0.5 and 0.6 eV from the conduction band edge. The defect density at these energies is relatively low, in the range of $10^{16} \div 10^{17} cm^{-3} eV^{-1}$ as it is away from both the conduction band tail and the deep defects. Gauss law proves that such density of states is consistent with the depletion of a 1500 Å-thick layer by the electric fields actually in place.

4. Experimental results

According to the design indications provided above, JFETs were grown and tested. In the process chamber the ratio of Si to P atoms was kept such that approximately 10^{18} dopant atoms per cubic cm were introduced. The silane flow was 40 sccm while the phosphine flow was 0.5 sccm, diluted in silane at 5%.

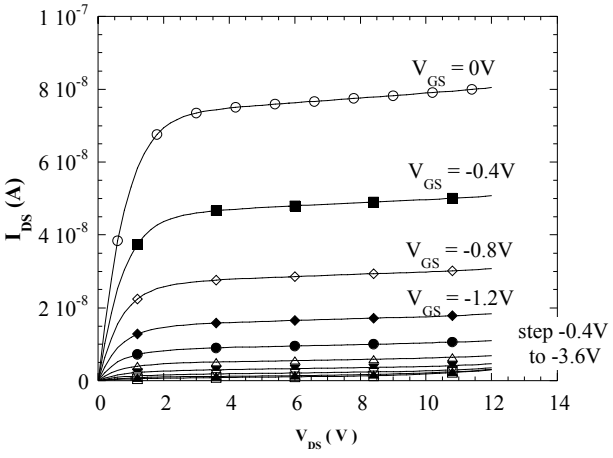

Fig. 3. Experimental output characteristics of a JFET with W/L = 400 µm / 40 µm. The process parameters have been chosen following the teaching of the simulation.

The intrinsic layer thickness was 3500 Å and the n-channel thickness was 1500 Å. The a-SiC:H p^+-layer was 400 Å-thick. Figure 3 reports the output characteristics of a device with W/L = 400 µm/40 µm. The experimental results clearly show a change of operating regime of the JFET at V_{DS} ranging from 1V to 2V, depending on the V_{GS} value. The change is attributed to the channel pinch-off, as expected in general in a JFET structure and as confirmed by the simulation study of the depletion with consistent voltage and doping values. From the curves reported, it is possible to estimate an approximate pinch-off voltage of –3.5V.

Until the voltage bias is unable bring the JFET into pinch-off, the potential profile along the channe can be calculated and is rather gradual. After pinch-off is reached, any further increase in V_{DS} (for a given V_{GS}) will drop on the drain side of the channel and modulate the actual channel length. The potential drop on the undepleted channel will stay constant instead. If the modulation ΔL of the channel length L is small compared to L itself, the differential resistance in the saturation region will be high, as desirable. In the presented JFET, the 40 µm-long channel seems to guarantee such a performance. A study is under way to trace the exact potential profile along the channel for the saturation region, as V_{DS} is made larger.

From the data in Fig. 3, experimental values of the transconductance g_m of the JFET can be extracted. In particular, values depend on the operating point that is chosen for the JFET to work as an amplifier. If the JFET is biased to work with a highly conducting channel (V_{GS} = 0V), g_m is approximately 10^{-7} A/V when for instance V_{DS} = 6V. This is better than state-of-the-art TFTs in similar bias conditions and confirms the expected advantage of using the JFET for linear circuits.

Finally, a confirmation of the agreement with the simulation results is presented in Fig. 4. Here, the values of the electron concentration n given by the simulation have been integrated along the thickness channel direction to ultimately provide an approximation of the I_{DS} current in the triode region. The good match further confirms the agreement of the simulation with the experimental device as processed along the simulation guidelines.

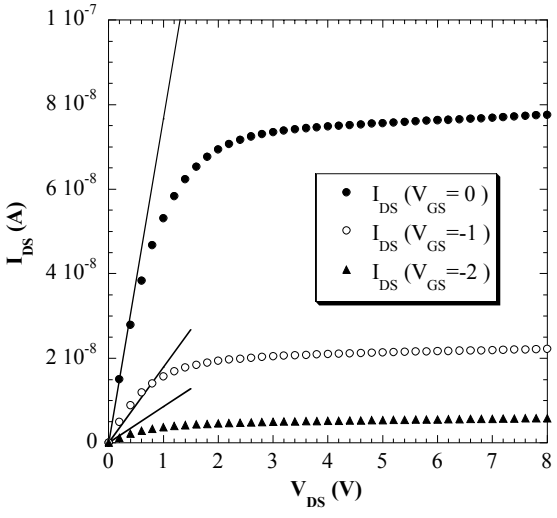

Fig. 4. Experimental output characteristics of the JFET as in figure 3 together with an approximation of the I_{DS} current in the linear region (solid lines) as obtained from the simulations.

5. Conclusions

An amorphous silicon-based JFET has been presented. It is fabricated without a high-quality high-temperature gate dielectric as it is the case for TFTs. This fabrication characteristic makes the JFET particularly interesting for processing on plastic substrates. The channel free electron concentration has been investigated by means of a one-dimensional finite-difference simulator as a function of the applied voltage bias, of the channel doping level and of the intrinsic layer thickness. From simulations, design guidelines have been extracted to achieve a device working with low pinch-off voltage. The realized JFET matches the design expectations, shows a pinch-off voltage at–3.5V and g_m values of 10^{-7} A/V in standard operating conditions.

References

[1] T. Tsukada in Technology and Applications of Amorphous Silicon edited by R.A. Street (Springer, Berlin, 2000) p. 7.

[2] R.A. Street in Technology and Applications of Amorphous Silicon edited by R.A. Street (Springer, Berlin, 2000) p.. 147

[3] H. Gleskova, S. Wagner, "Electrical stability of a-Si:H TFTs fabricated at 150 °C ", MRS Symp. Proc., 664 (2001), p. A19.7.1

[4] D. Caputo, U. Forghieri, F. Palma, "Numerical analysis of differential capacitance in a-Si:H solar cells: monitoring of light soaking experiment", Proc. of the 13th European Photov. Solar En. Conf., (1995) p. 187.

[5] R.A. Street, Philos. Mag. B, 63 (1991), p.1334.

[6] F. Lemmi, "Modeling of effects of material quality on fast characterization of state of the art a_Si:H p+-i-n photodiodes", J. Non-Cryst. Solids, 266-269 (2000), p. 1198.