Towards an Integrated Bulk/SOI Active Pixel APD Sensor: Bulk Substrate Inspection with Geiger Mode Avalanche Photodiodes

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Abstract

Assessment of bulk silicon quality after SOI removal and subsequent oxide removal is demonstrated utilising Geiger mode avalanche photodiodes. The dark count differences measured from Geiger mode operation of fabricated avalanche photodiodes was negligible between SOI and standard P-epi manufactured diodes. Photon count rates of illuminated test structures operating in Geiger mode were identical. This rapid test showed no differences among buried oxide plasma and wet etch removal. As plasma processing is preferred for the preferential opening of the buried oxide this is an important finding for subsequent device fabrication. The results of this rapid test assessment will be shown as well as the results from initial fabricated devices based on the findings from this work.

1. Introduction

Active pixel sensor arrays have been manufactured and incorporated into standard CMOS processes [1]. These detector arrays typically provide a pn junction or photogate for signal detection and integrated circuitry in each pixel for signal readout and processing. The photodiode detectors operate with no internal gain with each incident photon generating an electron-hole pair that is collected by the pn junction. The diodes are operated in photodiode mode (i.e. below breakdown) because CMOS circuitry must coincide with the detector in the same bulk silicon and voltages across the circuit must be minimised. Integrated operational amplifiers can be used to increase gain but the ultimate noise performance will suffer as amplifier noise is greater than detector noise. CMOS active pixel detector arrays are therefore not well suited for detecting low light levels. Avalanche photodiodes (APD) on the other hand provide a means of increasing the signal provided to the readout circuitry by utilising the internal multiplication gain mechanisms of the APD detector. Integration of APD detectors and readout circuitry is not possible at this time with bulk CMOS technology but is thought to be feasible using Silicon-on-Insulator (SOI) technology that allows for detector and readout circuit isolation.

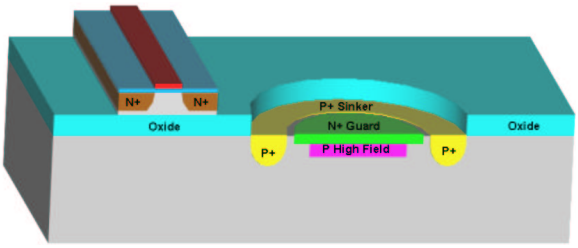

Figure 1. SOI/bulk APD detector

However, the silicon layers typically used in fully depleted SOI technology are very thin and this will decrease the quantum efficiency as only a small fraction of photons will be absorbed [2]. An alternate approach is to manufacture the detector in the bulk silicon beneath the insulating oxide layer as shown in Figure 1 and as recently reported in a hybrid bulk/SOI CMOS active pixel sensor [3]. For the fabrication of a bulk/SOI APD sensor it is necessary to etch the buried oxide back to the bulk silicon. Several different etching techniques are possible and it is necessary to assess the degradation of the etchant on the bulk silicon interface and it's effects on APD operation. By operating an APD beyond the breakdown voltage in Geiger mode it is possible to quickly and accurately determine the amount of process induced damage that has occurred and can provide *atto* Ampere resolution of measured dark current differences [4, 5].

2. Experimental

For this work, commercial bonded SOI wafers with CZ, P-type, <100>, 525μm thick substrates with 400nm thermal buried oxide layers and 340nm SOI film were tested. Three different oxide removal techniques were

performed to determine the impact on the bulk silicon beneath the buried oxide. All wafers received a plasma etch to remove the top SOI layer. The buried oxide layer were then etched to the bulk silicon layer through a buffered wet etch, a 100nm plasma over etch and a 200nm plasma over etch. Identical processing steps fabricated avalanche photodiodes using the standard CMOS compatible APD process at the NMRC. A standard P-epi wafer was included in the samples as a control.

3. Results

Forward and reverse leakage current testing were performed on the manufactured diodes. The extracted leakage current is shown in Figure 2 and Figure 3 for a 750μm in diameter large area APD [6].

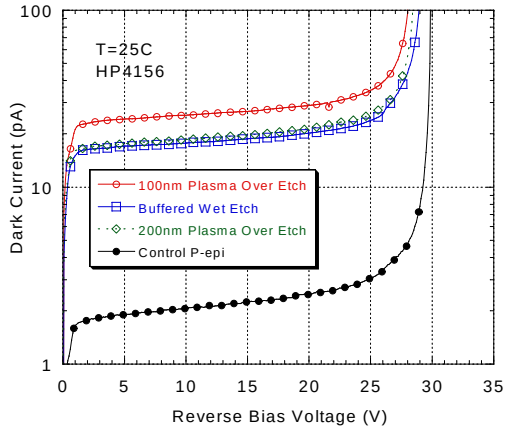

Figure 2. Reverse leakage current. 750μm APD

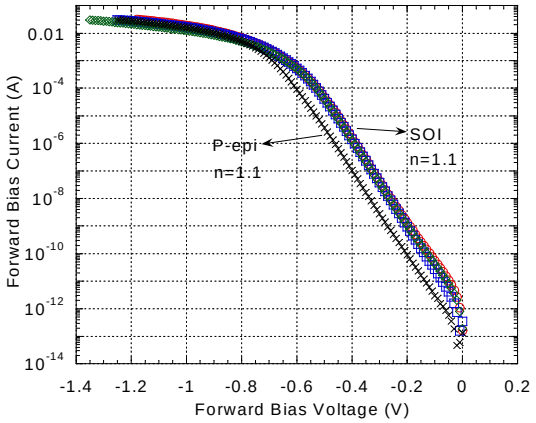

Figure 3. Forward bias current from a 750μm APD

Ideality factors of 1.1 were obtained for all of the 750μm detectors measured. Ambient light level gain measurements were performed and similar gains were observed across the four wafers, Figure 4 . The diodes were then operated in Geiger mode and the dark count per second was recorded for voltages that ranged from one volt to five volts above the breakdown voltage. This is a fast test with each computer controlled measurement taking only a few seconds and a relatively large sample size of 15 sites per wafer were measured as shown in Figure 5. The dark count shows that there are negligible differences in the buried oxide removal steps. The three SOI wafers showed better dark count performance than the P-epi wafer. The slope of the dark count versus excess bias voltage however does change between the SOI and P-epi wafers which is not well understood at this time. To ensure that the diodes were working effectively as photon counters, the diodes were illuminated on wafer with an LED source from a fixed operating distance. The measured photon count rate at various LED current intensities is shown in Figure 6 for 20μm and 15μm Geiger mode APD detectors. The deviation in the counting rate at the higher LED currents in the 20μm GM-APDs is due to the hold off time of the passive quenching circuit. The true count rate can be calculated using Equation 1 where N_{corr}

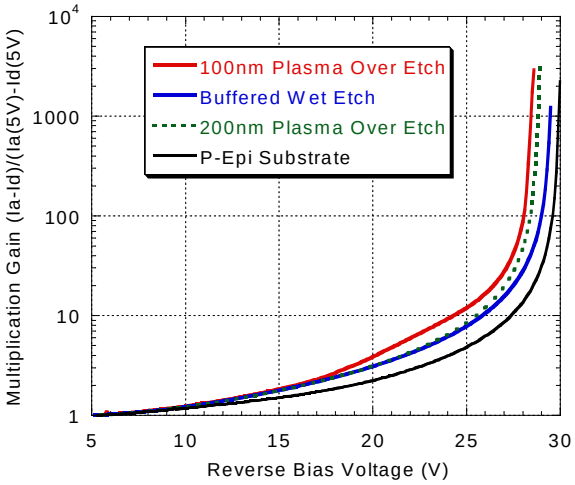

Figure 4. Multiplication gain curves. 750μm APD

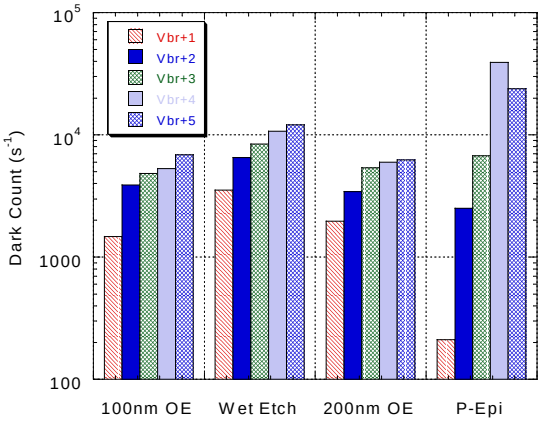

Figure 5. Dark count measured from the three SOI samples and one P-epi wafer. 15μm GM-APD measured at +1,2,3,4 & 5 beyond the breakdown voltage.

is the count rate corrected for the hold off time, t_{hoff}, influence on the measured count rate, N_{meas}.

$$N_{corr} = \frac{N_{meas}}{1 - (t_{hoff} N_{meas})} \quad (1)$$

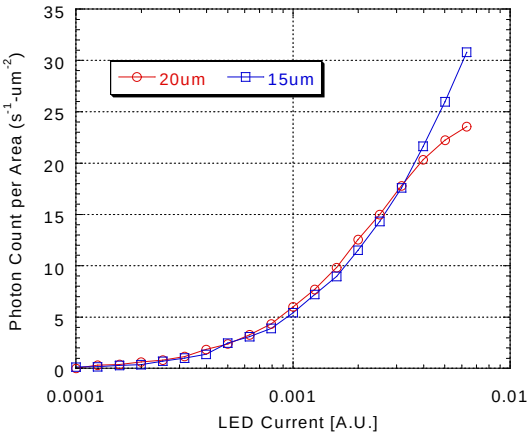

Figure 6. Uniformity among 15μm and 20μm GM-APDs

There are no issues surrounding the different area detectors and uniformity is seen throughout. The photon count rate for the three SOI wafers is shown in Figure 7 with no observed differences in the counting rates.

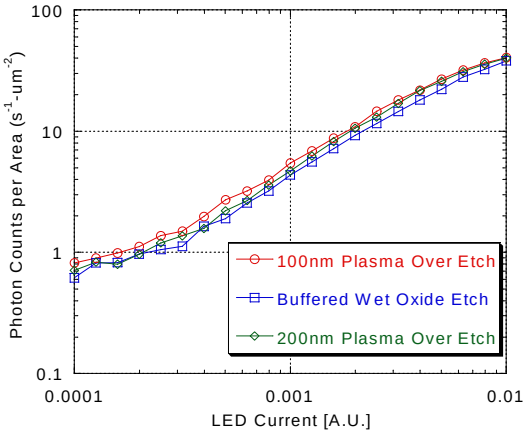

Figure 7. Photon count at various illumination levels from separate 15μm GM-APDs

From this initial rapid test using Geiger mode avalanche photodiodes it was determined that bulk silicon damage was not caused by the different etching procedures. If damage did occur during the oxide etch, the subsequent thermal gate oxide growth was sufficient for removal.

It will be shown that for the fabrication of SOI/bulk APD detectors, plasma etch processing can be used to for selective buried oxide removal. We will present the testing methodology and test structures necessary to rapidly assess the SOI bulk silicon interface using Geiger mode avalanche photodiodes and also initial testing of fabricated devices incorporating the SOI and APD design based on the initial process steps reviewed in this abstract. From this initial work, bulk fabrication of APD detectors allowing for a large collection volume and subsequent insulated SOI CMOS circuitry is feasible.

4. Acknowledgements

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