Failure Characterization of ESD Damage in Low Temperature Poly-Si TFTs

Chih-Chiang Chen
ERSO/ITRI
peterchen@itri.org.tw

Chang-Cheng Lin
ERSO/ITRI
jcherng@itri.org.tw

Wen-Yu Hung
ERSO/ITRI
amorphous@itri.org.tw

Yung-Hui Yeh
ERSO/ITRI
yhyeh@itri.org.tw

Abstract

The electrostatic discharge (ESD) induced failure is characterized for evaluating the yield and stability of LTPS TFTs. The impact of electrostatic discharge property is investigated in this study. The drain engineering and geometric effect relate to failure are also considered.

1. Introduction

Low temperature polycrystalline silicon (LTPS) technology has been the most promising method to realize system on panel and active matrix OLED [1-2]. The electrostatic discharge is one of the most critical issues, which low production yield. The TFT devices typically have worse ESD performance than those fabricated in bulk CMOS which has a relatively low thermal resistance. As the circuits all integrated in panel and continuous downscaling of device geometries, the low temperature polysilicon TFTs tend to be subject more electrostatic discharge during glass substrate transfer or process manufacture. The integrated circuit and active matrix array are easily deteriorated by ESD and defects occur in panel due to electrostatic breakdown. A common fallout observed in circuit is that holes or notching in the thin film and melting in the metal connection. According to Yanagisawa et al. [3], a soft failure of TFT under weak ESD is noticed. To better understand the influence of ESD induced catastrophic failure, we simulate the real environment by using a strong non-contact electrostatic discharge impulses to enhance failure phenomenon. In this study, LTPS TFTs were subjected to various electrostatic discharge pulse condition. Furthermore, the role of electrostatic discharge polarity has been examined and the drain engineering and geometric effect relate to severe damage also discussed.

2. Experimental

The top gate n-channel TFT with 1.5 μm LDD and self-aligned p-channel TFT was fabricated on Corning 1737 glass. The 50nm-thick polysilicon film was formed by XeCl excimer laser crystallization and 100nm thickness gate insulator was deposited by PECVD TEOS oxide, followed by a formed at 410C annealing. The source and drain regions are formed by the ion shower technique and impurities are actives at 450C furnace. Finally, the interlayer oxide and connection metal were formed. The TFT spacing between the gate edge and source and drain contact is 6 μm and 26 μm. To test the electrostatic discharge hardness on LTPS TFT, a non-contact mode ESD gun pulse is applied to active matrix array and the distance kept in 2cm.

3. Results and Discussion

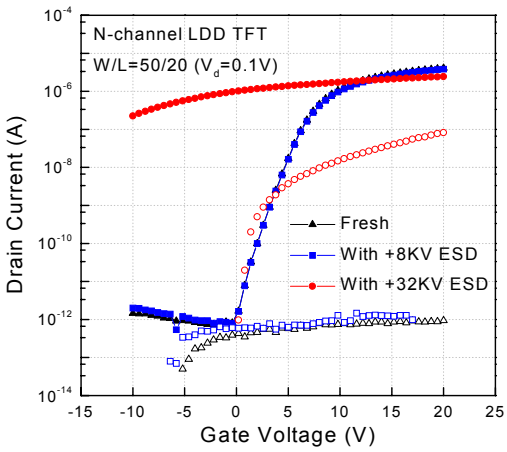

Figure 1. The transfer characteristics of ESD induced failure TFTs

Figure 1. Shows the characteristics of n-channel LDD devices suffer from vary electrostatic discharge pulse. When the small positive ESD voltage impact on TFT, about 7.1% degradation in mobility and 0.04V shift in threshold voltage (solid line). This phenomenon is due to interface state creating during slight impulse and so-call soft failure [3-4]. There is no certainty that such a slight impact will show latent effects and be a reliability hazard in device operation, but it has definitely been damage. The gate insulator that deposited in low temperature ambience can't sustain high voltage normally. As ESD

voltage increasing, the gate dielectric leakage rising (open line) which implying the insulator is burned out and become hard breakdown. The destructive failure is due to thermal effect by joule heating in device that is independent of the trapped charge at interface or in oxide [5][7]. This indicated that permanent damage has occurred rather than that revertible soft failure.

The probabilities of ESD failure are illustrated in Figure 2. The failure is defined as the gate leakage current exceeds 10^{-9}A. The electrostatic discharge amplitude is from 8KV to 32KV. It is clearly show that the fallout increases as electrostatic discharge are increased to 22KV and under 8KV electrostatic discharge level, there was not significantly decrease the fallout. The results indicated that n-channel TFTs had an average electrostatic discharge level of about 8KV and p-channel about 15KV. It also shows that n-channel TFT suffer more severe under positive impulse that attribute to trigger the parasitic n-p-n is more efficient than that of the parasitic p-n-p. The n-channel TFT is more easily to trigger and shunt all ESD current and eventually fail [5]. When the maximum ESD amplitude is at gate pad, the electrostatic discharge direct tunnelling through gate insulator while located at source/drain terminal, near drain edge is the main breakdown region for excess leakage current. It's most likely that pin-hole like semi-conductive paths are generated in insulator by ESD injecting [4].

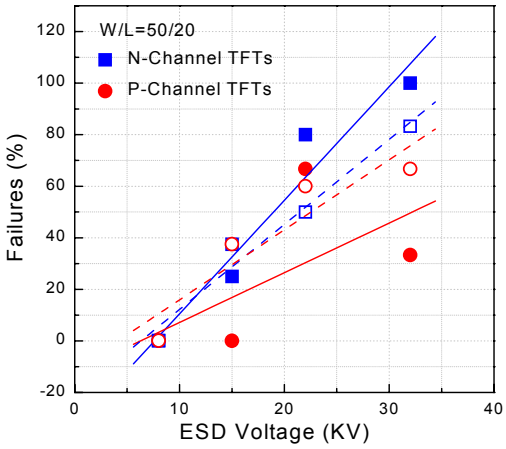

Figure 2. Failure distribution under ESD for both n- and p-channel TFTs
(Solid Line: positive ESD; Dash Line: negative ESD)

To reduce RC delay, low impedance is adopting that result in low ESD immunity and the drain contact to gate spacing (DCG) is key parameters to improve electrostatic discharge robustness. Figure 3 shows that the correlation between DCG and polarity ESD amplitudes. We find out the TFT with 6 μm DCG (solid line) has worse yield.. Moving the contact away from the gate edge to an optimum amount improve the fallout. It is due to the short DCG has low impedance path and provide ESD a good way to sluice and lead to some reduction in damage threshold. As applied electrostatic impact increase, raising in the power density, while current density and electric field increasing. As large DCG device under electrostatic discharge condition, the ballasting resistance between the contacts the hot spot is reduced but severe impulses make the fallout the same. We also find out that devices with gate metal overlap source/drain structure almost fail due to peak electric field locate overlap point where the power density is maximal. We consider that an optimum drain contact to gate spacing should be considered to improve the ESD robustness [6].

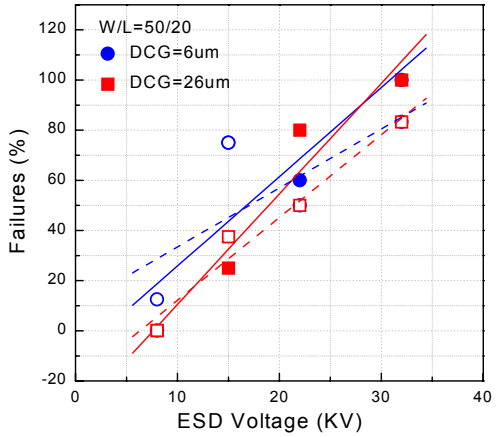

Figure 3. The correlation between DCG and positives ESD amplitudes
(Solid Line: 6 μm DCG; Dash Line: 26 μm DCG)

As it well knows, hot carrier effect and electrostatic discharge degrade device reliability and can be viewed as similar. ESD is fast and random with a short-term high current, while hot carrier degradation is slow and uniform with a long-term low current. Figure 4 shows the n-channel LDD devices with different drain contact to gate spacing structure under hot carrier injecting condition (V_d=12, 30V and V_g=4~16V). A threshold voltage shift severe in the positive direction can be observed and TFTs with 6 μm drain contact to gate spacing in low field injection shows more serious. It can be contributed that higher electric field and impact ionization efficiency caused severe chain reaction. We estimated that drain avalanche hot carrier effect is more like electrostatic injury than channel hot carrier effect. Device with 6 μm DCG were ravaged due to punch-through at drain side when drain voltage large to 16V. It also finds that the TFT with overlap structure can't sustain hard hot carrier condition. The experience is

similar to electrostatic discharge result and hot carrier stability seems to be a method to quality ESD robust engineering [7-8].

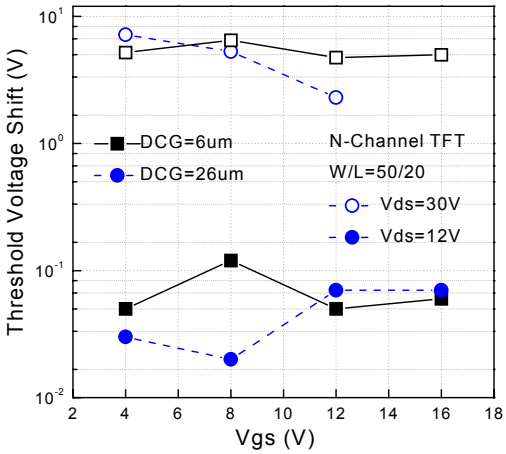

Figure 4. The threshold voltage shift under hot carrier stress condition
(Solid Line: 6 μ m DCG; Dash Line: 26 μ m DCG)

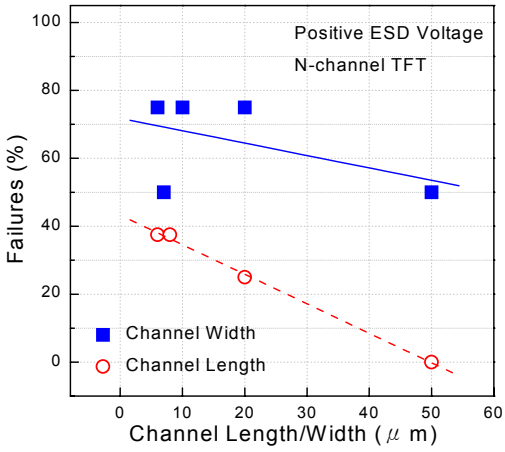

Figure 5. Relationship between Failure and channel geometric effect

For circuit integration, it is required to have small geometries to increase area density. Figure 5 shows the relationship between ESD Failure probability and geometric effect of n-channel TFT. The phenomenon of channel length effect is not conspicuous, which was covering by harsh electrostatic damage. An overview of different channel width with 50 μ m devices were indicated that under 20 μ m length the fallout yield has degraded about 80~100%. As for wide channel width, the current has been spread out and eliminate the current crowing at drain corner which reducing thermal effect. This phenomenon is most serious under 10 μ m width. We also find that channel width effect is more sensitive to electrostatic discharge than channel length. In most semiconductor device, push-pull circuit with large channel width is used to enhance the output capability and ESD immunity.

4. Conclusion

We have investigated the effect of electrostatic discharge induced failure damage on low temperature polysilicon TFTs. The relationship between ESD property and device failure characteristic were observed. In addition, it had been found that p-channel has higher electrostatic discharge capability, the higher ESD immunity. It is shows that hot carrier reliability relates to electrostatic discharge robustness. We also discussed the drain engineering and geometric effect of failure mechanism.

5. Acknowledgment

The authors thanks the FPD group of ERSO/ITRI for their comments and support.

6. References

[1] T. Nakamura, M. Karube, H. Hayashi, K. Nakamura, N. Tada, H. Fujiwara, J. Tsutsumi, T. Motai "Low Temperature Poly-Si TFT-LCD with Integrated Analog Circuit" *Asia Display/IDW '01*, pp.1603, 2001.

[2] S. Mark, S. H. Robert S., P. Leo , and K. H. Miltiadis "Polysilicon TFT technology for active matrix OLED displays " *IEEE Trans. Electron Devices*, Vol.48, No.5, pp. 845, 2001.

[3] T. Yanagisawa "Electrostatic Damage and Protection for TFT-LCDs" *SID '93 Digest,* pp.735,1993.

[4] S. Uchikoga, M. Kakinoki, K. Suzuki, M. Ikeda "Deterioration Mechanism of a-Si:H TFT Caused by Electrostatic Discharge" *AMLCD '94 Digest*, pp.128, 1994.

[5] N. Tosic, F. G. Kuper, T. Mouthaan "Transmission Line Model Testing of Top-Gate Amorphous Silicon Thin Film Transistors" in *Proc. IRPS*, 2000,p289.

[6] M. Tada, S.Uchikoga, M. Ikeda "Power-Density-Dependent Failure of Amorphous-Si TFT" *AMLCD '96 Digest*, pp.269, 1996.

[7] W. K. Chim, B. P. Yeo, P. S. Lim, D. S. H. Chan "Low-frequency Noise Characterization of Latent Damage in Thin Oxides Subjected to High-field Impulse Stressing" *IEEE Electron Device Lett.*, Vol.19, No.10, pp.363, 1998.

[8] A. Shian, C. Amitava, P. Thomas "Hot-electron Reliability and ESD Latent Damage" *IEEE Trans. Electron Devices*, Vol.35, No.12, pp. 2189, 1988.