Paper id	Title of the paper	Category of the paper
1	Evolution, Current Status and Future Trend of RF Transistors	Advanced Devices
3	Knowing the Key Factors in RF Power Amplifier Design	Advanced Devices
7	Design Sensitivity in Quasi-One-Dimensional Silicon-Based Photonic Crystalline Waveguides	Advanced Devices
31	High reproducible ideal SiC Schottky rectifiers by controlling surface preparation and thermal treatments	Advanced Devices
40	Improved Isolated RESURF Technology for a Multi Power BCD Process	Advanced Devices
46	Design Guidelines for Linear Amplification and Low-insertion loss in 5-GHz-band SOI Power MOSFETs	Advanced Devices
53	Future Trends in Intelligent Interface Technologies for 42V Battery Automotive Applications	Advanced Devices
59	Temperature-Dependent Characteristics of an n+-InGaAs/n-GaAs Composite Doped Channel (CDC) Heterostructure Field-Effect Transistor	Advanced Devices
61	On the n+-GaAs/p+-InGaP/n--GaAs High-Barrier Camel-Like Gate Transistor for High-Breakdown, Low-Leakage and High-Temperature Operations	Advanced Devices
63	An InGaP/GaAs Resonant-Tunnelling Bipolar Transistor (RTBT) with Multiple Negative-Differential-Resistance (MNDR) Phenomena	Advanced Devices
75	Application of Polycrystalline SiGe for Gain Control in SiGe Heterojunction Bipolar Transistors	Advanced Devices
82	Low Power, 3-bit CMOS Pipeline ADC with Reduced Complexity Flash Architecture	Advanced Devices
90	Study of Hot-spot Phenomena in Cellular Power Transistors by Analytical Electro-Thermal Simulation	Advanced Devices
94	Pseudo Dynamic Gate Design based on the Resonant Tunneling-Bipolar Transistor (RTBT)	Advanced Devices
99	Cost Effective Implementation of a 90 V RESURF P-type Drain Extended MOS in a 0.35 um Based Smart Power Technology	Advanced Devices
115	TCAD Based Design Methodology for Substrate Current Control in Smart Power ICs	Advanced Devices
122	A 12Volt, 12GHz Complementary Bipolar Technology for High Frequency Analogue Applications	Advanced Devices
124	Optimising High-Voltage Devices in a Smart Power Technology, using the RESurF-effect and TCAD.	Advanced Devices
129	Voltage-controlled substrate structure for integrated inductors in standard digital CMOS technologies	Advanced Devices
130	Temperature Effects of Low Noise InGaP/InGaAs/GaAs PHEMTs	Advanced Devices
146	Realization of a SCR on an Epitaxial Substrate Using Al Thermomigration	Advanced Devices
148	Engineering of 80V Vertical n-DMOS in a 0.35um CMOS Technology	Advanced Devices
171	The Advanced RESURF Structure to improve On-Resistance in BCDMOS	Advanced Devices
177	Fabrication and Experimental Results of Lateral Trench Electrode IGBT	Advanced Devices
187	A Low On-Resistance 700V Charge Balanced LDMOS with Intersected WELL Structure.	Advanced Devices
196	On the High Temperature Operation of High Voltage Power Devices	Advanced Devices
197	Lateral Trench Gate Super-Junction SOI-LDMOSFETs with Low On-Resistance	Advanced Devices
205	The Four-Gate Transistor	Advanced Devices
206	A novel, low-power Capacitive waveform transformer	Advanced Devices
213	A MOS Nanogap Device Structure for Characterisation of Nano-scale Objects	Advanced Devices
214	The Double-Bandgap-Narrowing Transistor	Advanced Devices
227	Enhanced intrinsic gain (gm/gd) of PMOSFETs with a Si(0.7)Ge(0.3) channel	Advanced Devices
235	High-performance Silicon-On-Glass VDMOS transistor for RF-power applications	Advanced Devices
237	Gate length scaling in high fMAX Si/SiGe n-MODFET	Advanced Devices
242	Reduction of Short-Channel Effects and Improvement in Microwave Characteristics for V-groove Gate Pseudomorphic Doped-Channel HFET with Dual V-groove Gate Structure	Advanced Devices

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251	Self Heating in InP DHBT Technology for 40 Gb/s ICs	Advanced Devices
257	Vertical high voltage devices on thick SOI with back-end trench formation	Advanced Devices
265	Experimental study of depletion mode Si/SiGe MOSFETs for low-temperature operation	Advanced Devices
6	Tunneling Phenomenon in SuperFlash Cell	CMOS and Memory Devices
9	Off-Leakage and Drive Current Characteristics of Sub-100-nm SOI MOSFETs and Impact of Quantum Tunnel Current	CMOS and Memory Devices
19	Hot carrier reliability improvement of PMOS I/O's transistor in advanced CMOS technology	CMOS and Memory Devices
20	Reduction of Bitline to Control Gate leakage for improved embedded 0.18 um FLASH Yield and Reliability	CMOS and Memory Devices
21	Reverse-Order Source/Drain (R-S/D) Combined with LDD Offset Spacer and Its Application to 50nm Physical-Gate-Length nMOSFETs	CMOS and Memory Devices
25	Degradation Dynamics for Deep Scaled p-MOSFET's during Hot-Carrier Stress	CMOS and Memory Devices
37	Performance and reliability of high density flash EEPROMs under CHISEL programming operation	CMOS and Memory Devices
50	Investigation of performance improvement and gate-to-junction leakage reduction for the 90nm CMOS gate stack architecture	CMOS and Memory Devices
56	Monitoring Flash EEPROM Reliability by Equivalent Cell Analysis	CMOS and Memory Devices
57	Fabrication of 0.1-um pMOSFETs with SiGe-Channel and Elevated B-Doped SiGe Source and Drain Layers	CMOS and Memory Devices
66	A Viable Self-aligned Bottom-Gate MOSFET Technology for High Density and Low Voltage SRAM	CMOS and Memory Devices
67	Impact of Tunnel Oxide Thickness on Erratic Erase in Flash Memories	CMOS and Memory Devices
70	Effect of Pulsed Stress on Leakage Current In MOS Capacitors For Non-Volatile Memory Applications	CMOS and Memory Devices
88	Highly Extendible Memory Cell Architecture for Reliable Data Retention Time for 0.10mm Technology Node and beyond	CMOS and Memory Devices
112	Electrical Characterisation of Silicon-Rich-Oxide Based Memory Cells Using Pulsed Current-Voltage Techniques	CMOS and Memory Devices
120	Temperature-Independence-Point Properties for 0.1um-scale Pocket-Implant Technologies and the Impact on Circuits Design	CMOS and Memory Devices
123	Comparison of the Gate Tunneling Current in Ultrathin-Oxide Inversion and Accumulation MOSFETs	CMOS and Memory Devices
133	Gate Material Properties Induced 0.25µm SRAM Marginality	CMOS and Memory Devices
134	Influence of Doping Profile and Halo Implantation on the Threshold Voltage Mismatch of a 0.13um CMOS Technology	CMOS and Memory Devices
137	SiGe pMOSFETs Fabricated on Novel SiGe Virtual Substrates Grown on 10µm x 10µm Pillars.	CMOS and Memory Devices
154	Impact of statistical threshold voltage fluctuation and quantum mechanical effects on cmos circuits with gigabit feature size	CMOS and Memory Devices
165	Ultra-Thin Oxide Lifetime Estimation Using Transistor Degradation	CMOS and Memory Devices
167	Substrate bias effect on cycling induced performance degradation of Flash EEPROMs	CMOS and Memory Devices
168	A Novel Dynamic Threshold Operation Using the Electrically Induced Junction MOSFET in the Deep Sub-micrometer CMOS Regime	CMOS and Memory Devices
178	Elevated Co-Silicide for sub-100nm High Performance and RF CMOS	CMOS and Memory Devices
180	Investigations on Poly-SiGe gate in full 0.1µm CMOS integration	CMOS and Memory Devices
191	High performance 0.1um CMOS device with suppressed parasitic junction capacitance and junction leakage current	CMOS and Memory Devices
192	Scaling Behaviour of Large-grain Polysilicon MOSFETs	CMOS and Memory Devices

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193	New mechanism of body charging in partially depleted SOI-MOSFETs with ultra-thin gate oxides	CMOS and Memory Devices
199	Substrate Effects on the Small-Signal Characteristics of SOI MOSFETs	CMOS and Memory Devices
203	Channel Engineering Study for 50 nm P-Channel MOSFET	CMOS and Memory Devices
204	Raised Source/Drain on 50nm CMOS Circuits : Propagation Delay and Dynamic Power Optimizations	CMOS and Memory Devices
211	50nm Schottky Barrier CMOS with Conventional Silicide	CMOS and Memory Devices
215	Understanding nMOSFET characteristics after soft breakdown and their dependence on the breakdown location	CMOS and Memory Devices
228	Advanced Junction Engineering for 60nm-CMOS Transistors	CMOS and Memory Devices
234	Programming by Tunneling in Nanocrystal Memories	CMOS and Memory Devices
247	Controlling STI-related parasitic conduction in 90 nm CMOS and below	CMOS and Memory Devices
256	Reliability and Retention Study of Nanocrystal Cell Array	CMOS and Memory Devices
259	65 nm Transistors for a 90 nm CMOS SOC Platform	CMOS and Memory Devices
262	A Novel CMOS Compatible Top-Floating-Gate Flash EEPROM Cell.	CMOS and Memory Devices
266	Influence of source-drain tunneling on the subthreshold behavior of sub-10nm double-gate MOSFETs	CMOS and Memory Devices
268	Improved Deep Sub-micron CMOS Ring Oscillator Performance with n-HDD and n-LDD P+ + As+ Co-Implant	CMOS and Memory Devices
270	Suitability of Scaled SOI CMOS for High-Frequency Analog Circuits	CMOS and Memory Devices
272	High Hot-Carrier and ESD Immunity Device for High-Voltage I/O NMOSFETs in 0.1-um CMOS Technology	CMOS and Memory Devices
275	Si Nanocrystal Based Memory Structures by Ultra Low Energy Implantation for Low Voltage/Low Power Applications	CMOS and Memory Devices
277	Fast Algorithm for Clock Grid Simulation	CMOS and Memory Devices
5	Impact of Deep N-well Implantation on Substrate Noise Coupling and RF Transistor Performance for Systems-on-a-Chip Integration	ITRS Roadblocks, Models and Process Steps
24	Post-Process CMOS Front End Engineering With Focused Ion Beams	ITRS Roadblocks, Models and Process Steps
30	A Tuneable Metal Gate Work Function Using Solid State Diffusion of Nitrogen	ITRS Roadblocks, Models and Process Steps
32	Impact of ALCVD and PVD Titanium Nitride Deposition on Metal Gate Capacitors	ITRS Roadblocks, Models and Process Steps
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51	Impact of Post Metal Etch Resist Strip in Plasma on Plasma Charge-Induced Erosion of Tungsten-Plugs	ITRS Roadblocks, Models and Process Steps
54	Suppression of CoSix Induced Leakage Current using Novel Capping Process for Sub-0.10um node SRAM Cell technology	ITRS Roadblocks, Models and Process Steps
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78	Characteristics of HfO2 pMOSFET with ultrashallow junction prepared by plasma doping and laser annealing	ITRS Roadblocks, Models and Process Steps
81	Diffusion Suppression in Silicon by Substitutional C Doping	ITRS Roadblocks, Models and Process Steps
84	Impact of p-Well Implantation Parameters on Junction Leakage	ITRS Roadblocks, Models and Process Steps
85	High Temperature CMOS Process with Dielectric Isolation	ITRS Roadblocks, Models and Process Steps
86	Impact of source/drain implants on threshold voltage matching in deep sub-micron CMOS technologies	ITRS Roadblocks, Models and Process Steps
96	Lithography Independent Fabrication of Nano-MOS-Transistors with W = 25 nm and L = 25 nm	ITRS Roadblocks, Models and Process Steps

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101	Stability of High-k Thin Films for Wet Process	ITRS Roadblocks, Models and Process Steps
105	Stability of High-k Thin Films in Moisture Ambience - The Effect of Dissolution Gas from Acryl Apparatus -	ITRS Roadblocks, Models and Process Steps
106	Electrical Characteristics Improvement of Dy2O3 Thin Films by In-situ Vacuum Anneal	ITRS Roadblocks, Models and Process Steps
107	Use of Oxynitride Dielectric to Maximise the Growth Rate of Selective Epitaxial Base Layer in a Self-Aligned Double-Polysilicon SiGe Bipolar Transistors	ITRS Roadblocks, Models and Process Steps
108	Annealing Condition Dependence of Electrical Characteristics.	ITRS Roadblocks, Models and Process Steps
109	Identification of Critical Parameters for Plasma Process-Induced Damage in 130 and 100 nm CMOS Technologies	ITRS Roadblocks, Models and Process Steps
111	Electrical Characteristics of Gd2O3 thin film deposited on Si substrate.	ITRS Roadblocks, Models and Process Steps
113	Characteristics of High-k Gd2O3 Films Deposited on Different Orientation of Si Substrate	ITRS Roadblocks, Models and Process Steps
126	Gate dielectrics for high performance and low power CMOS SoC applications	ITRS Roadblocks, Models and Process Steps
141	Reducing the Threshold Voltage Deviation for sub-100nm Transistors using Midbandgap-Gatematerials	ITRS Roadblocks, Models and Process Steps
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150	Mechanisms of dopant redistribution and retention in Silicon following ultra-low energy Boron implantation and excimer laser annealing	ITRS Roadblocks, Models and Process Steps
158	Impact of stochastic dopant variation and the copper size effect on gigascale integration	ITRS Roadblocks, Models and Process Steps
160	Process Integration of Crystalline Pr2O3 High-k Gate Dielectrics	ITRS Roadblocks, Models and Process Steps
163	Effect of annealing on wet oxidation of AlxGa1-xAs Layer	ITRS Roadblocks, Models and Process Steps
164	Si/SiGe Cross-hatching: a Good Indicator of Strained Si MOSFET Performance	ITRS Roadblocks, Models and Process Steps
173	Simulation of high-K tunnel barriers for nonvolatile floating gate memories	ITRS Roadblocks, Models and Process Steps
174	Through-Wafer Copper Electroplating for RF Silicon Technology	ITRS Roadblocks, Models and Process Steps
189	A New Latch-Up Free Complementary Bipolar Process using PBSOI Technique	ITRS Roadblocks, Models and Process Steps
194	Channel architecture optimisation to reduce RNCE of deep sub-micron devices	ITRS Roadblocks, Models and Process Steps
195	Gate oxide process impact on RNCE for advanced CMOS transistors	ITRS Roadblocks, Models and Process Steps
201	Influence of the Ge-concentration and RTA on the device performance of strained Si/SiGe pMOS devices	ITRS Roadblocks, Models and Process Steps
210	A Complete Evaluation of Trench Oxide Thickness Effect on Advanced ULSI	ITRS Roadblocks, Models and Process Steps
217	Effect of Si Cap Layer Thickness on Parasitic Channel Operation in SiSiGe MOS Structures	ITRS Roadblocks, Models and Process Steps
218	A Self-Aligned Double Poly-Si Process Utilizing Non-Selective Epitaxy of SiGe:C for Intrinsic Base and Poly-SiGe for Extrinsic Base	ITRS Roadblocks, Models and Process Steps
219	The characteristics of leakage current mechanisms and SILC effects of Al2O3 gate dielectric	ITRS Roadblocks, Models and Process Steps
221	Triple Gate Oxide by Nitrogen Implantation Integrated in a 0.13µm CMOS Flow	ITRS Roadblocks, Models and Process Steps
224	Determination of beryllium and self-interstitial parameters for modeling of Be activation implanted in InGaAs	ITRS Roadblocks, Models and Process Steps

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238	Thermal Nitridation of Chemical Dielectrics as an Easy Approach to Ultra-thin Gate Oxide Processing	ITRS Roadblocks, Models and Process Steps
239	Direct-Current Performance Improvements of Al0.45Ga0.55As/GaAs Digital Graded Superlattice-Emitter Heterojunction Bipolar Transistors by Wet-Oxidation	ITRS Roadblocks, Models and Process Steps
249	ZrO2 gate dielectrics prepared by e-beam deposition of Zr and YSZ films and post annealing processes	ITRS Roadblocks, Models and Process Steps
250	Optimization of Single Halo p-MOSFET Implant Parameters for Improved Analog Performance and Reliability	ITRS Roadblocks, Models and Process Steps
261	A New Compact Horizontal Current Bipolar Transistor (HCBT) Fabricated in (110) Wafers	ITRS Roadblocks, Models and Process Steps
269	RPN Oxynitride Gate Dielectrics for 90 nm Low Power CMOS Applications	ITRS Roadblocks, Models and Process Steps
2	Noise Analysis for a SiGe HBT by Hydrodynamic Device Simulation	Modeling and Characterization
4	Compact LDD/FD SOI CMOS Device Model Considering Energy Transport and Self Heating for SPICE Circuit Simulation	Modeling and Characterization
11	Evaluation of Interface Trap Density in a SiGe/Si Heterostructure Using a Charge Pumping Technique and Correlation between the Trap Density and Low Frequency Noise in SiGe-Channel pMOSFETs	Modeling and Characterization
12	Compact Breakdown Model for PD SOI NMOS Devices Considering BJT/MOS Impact Ionization for SPICE Circuit Simulation	Modeling and Characterization
13	A New Physical Modeling of Parasitic Capacitances of Deep-Submicron LDD MOSFETs	Modeling and Characterization
14	Dissipative transport in quantum wires	Modeling and Characterization
15	Influence of the Extrinsic Base on the Base Current Kink in SiGe BJTs	Modeling and Characterization
17	Static and RF behaviour of short-gate Fully-Depleted Silicon-on-Insulator MOSFETs: numerical and experimental analysis	Modeling and Characterization
18	Small Signal Characterization of Thin Film Single Halo SOI MOSFET For Mixed Mode Analog and Digital Applications	Modeling and Characterization
22	Comments on Existing 1/f Noise Models:Spice, HSPICE and BSIM3v3 for MOSFETs in Circuit Simulators	Modeling and Characterization
27	Nano crystal memory devices characterization using the charge pumping technique	Modeling and Characterization
28	Properties of Vacancies in Silicon Determined from Laser--Annealing Experiments	Modeling and Characterization
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33	Self-Consistent Solution of the Schrodinger and Poisson Equations for Accumulated MOS Capacitors with Ultra-thin Layers	Modeling and Characterization
34	Extraction of Si-SiO2 interface trap densities in MOSFET's with oxides down to 1.3 nm thick	Modeling and Characterization
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41	Threshold Variations for Undoped Double-Gate MOSFET's	Modeling and Characterization
42	Effects of Boron and Germanium Base Profiles on SiGe and SiGe:C BJT Characteristics	Modeling and Characterization
43	Simulation and Modeling of Nanocrystalline Silicon Thin Film Transistors	Modeling and Characterization
45	SILC Measurements of Thin SiO2 at Low Voltages: High-resolution measurements and interpretation	Modeling and Characterization
47	Coupled Monte Carlo Simulation of Si and SiO2 Transport in MOS Transistors	Modeling and Characterization
48	Metal Rings as Quantum Bits	Modeling and Characterization

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52	High-Frequency Bipolar Transistor Noise Modeling	Modeling and Characterization
55	On the origin of the 1/f1.7 noise in deep submicron partially depleted SOI transistors	Modeling and Characterization
60	Impact of Scaling Down from 0.25um to 0.18um CMOS Technology on 1/f Noise: Characterisation and Modelling	Modeling and Characterization
64	Characteristics of Polysilicon Resistors for Sub-Quarter Micron CMOS Applications	Modeling and Characterization
68	Inversion Layer Quantization Impact on the Interpretation of 1/f Noise in Deep Submicron CMOS Transistors	Modeling and Characterization
72	Microwave noise Modeling of the 0.18um Gate Length Mosfets with a 60GHz cut-off frequency	Modeling and Characterization
74	Modeling the C-V Characteristics of Heterodimensional Schottky Contacts	Modeling and Characterization
77	Implantation Dose Profiling by MOS C-V Measurements	Modeling and Characterization
79	Compact Quantum Mechanical Device Models for MOSFETs in Gigascale Integration(GSI)	Modeling and Characterization
80	Transmission Coefficient Estimation for High-K Gate Stack Evaluation	Modeling and Characterization
89	Deep Trap Modelling and Transient Measurements of a-Si:H p-i-n Diodes	Modeling and Characterization
95	A New Improved Model for LDMOS Transistors under Different Gate and Drain Bias Conditions	Modeling and Characterization
97	Investigating 50nm channel length vertical MOSFET containing a dielectric pocket, in a circuit environment	Modeling and Characterization
98	A method for extraction of power dissipating sources from interferometric thermal mapping measurements	Modeling and Characterization
102	Implementing Self-Heating Effects into a Volterra Simulator	Modeling and Characterization
104	Scaling considerations for fully-depleted SOI transistors down to the 20nm gate length regime	Modeling and Characterization
114	Accurate modeling of Quantum-Dot based Multi Tunnel Junction Memory: Optimization and process dispersions analyzes for DRAM applications	Modeling and Characterization
118	Investigation of the Thermal Noise of MOS Transistors under	Modeling and Characterization
119	Accurate Delay Metric for On-chip Resistive Interconnect	Modeling and Characterization
121	Low frequency noise in 0.12 µm Partially and Fully Depleted SOI technology	Modeling and Characterization
125	Design and simulation of an a-Si:H/GaAs heterojunction bipolar transistor	Modeling and Characterization
127	Efficient Monte Carlo Simulation of Tunnel Currents in MOS Structures	Modeling and Characterization
128	Improved Modified Local Density Approximation for the Modeling of Size Quantization in pMOSFETs	Modeling and Characterization
132	Quasi-analytical modelling of drain current and conductance of Single Electron Transistors with MIB	Modeling and Characterization
135	Coulomb Blockade in Thin SOI Nanodevices	Modeling and Characterization
136	Mixing Sources of Intrinsic Parameter Fluctuations in the Simulation of Sub-100nm MOSFETs	Modeling and Characterization
138	A Robust and Physically Based Compact SOI-LDMOS Model	Modeling and Characterization
140	Improved Compact RF-Noise Modelling for Deep Sub-Micron MOSFETs	Modeling and Characterization
143	Electron Transport in Semiconductor-Insulator Structures Using the Full-Band Dispersion Relation of Si and SiO2	Modeling and Characterization
147	Process and device simulation of power VDMOS transistors in Bipolar/CMOS/DMOS technology	Modeling and Characterization
149	Tunnelling and impact ionization in scaled double doped PHEMTs	Modeling and Characterization
151	Universal Test Structure and Characterization Method for Bias-Dependent Drift Series Resistance of HV MOSFETs	Modeling and Characterization
152	A New Test Structure for In-situ Measurements of interface Recombination During Surface Treatments	Modeling and Characterization
155	Impact of technology parameters on inverter-delay of UTB-SOI CMOS	Modeling and Characterization
162	Accurate Modelling of Thin-Film Resistor up to 40 GHz	Modeling and Characterization

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166	Efficient Analysis and Optimization of ESD Protection Circuits	Modeling and Characterization
175	A new approach to failure analysis and yield enhancement of very large-scale integrated systems	Modeling and Characterization
176	UIS-Failure of DMOS Power Transistors	Modeling and Characterization
179	Monte Carlo Simulation of Program and Erase Charge Distributions in NROM(TM) Devices	Modeling and Characterization
181	Constant and Switched Bias Low Frequency Noise in p-MOSFETs with Varying Gate Oxide Thickness	Modeling and Characterization
182	Temperature dependence of the hard breakdown current of MOS capacitors	Modeling and Characterization
183	Effects of random discrete impurities in ultra-short MOSFET using 3D Monte Carlo simulation	Modeling and Characterization
184	Exploring Methods for Adequate Simulation of Sub-100nm Devices	Modeling and Characterization
185	Effects of Stress-Induced Bandgap Narrowing on Reverse-Bias Junction Behavior	Modeling and Characterization
186	A Simple and Accurate HSPICE Compatible Gate Leakage Macro Model	Modeling and Characterization
190	A New S-parameter Measurement-Based Method for MOSFET Gate Resistance Extraction	Modeling and Characterization
198	Three-Dimensional Analysis of a MAGFET at 300 K and 77 K	Modeling and Characterization
208	An Improved Model for Electron Mobility Degradation by Remote Coulomb Scattering in Ultra-Thin Oxide MOSFETs	Modeling and Characterization
209	An Algorithm for Smoothing Three-Dimensional Monte Carlo Ion Implantation Simulation Results	Modeling and Characterization
216	A Compact Model of the MOS Tunnel Emitter Transistor	Modeling and Characterization
223	Experimental Verification of the Smoothie Database Model for Third and Fifth Order Intermodulation Distortion	Modeling and Characterization
225	Influence of dot size and density on the program characteristics of nanocrystal Flash memories	Modeling and Characterization
226	Electron Transport in Nanoscale Double-Gate MOSFETs from Monte-Carlo and Quantum Ballistic Simulation	Modeling and Characterization
230	Modeling of Accumulation MOS Capacitors	Modeling and Characterization
231	An experimental study of the influence of channel positioning on low-frequency noise in Si(0.7)Ge(0.3) pMOSFETs	Modeling and Characterization
232	Three-dimensional simulation of the channel stop implant effects in sub-quarter micron PMOS transistors	Modeling and Characterization
233	Physics of the subthreshold slope - initial improvement and final degradation in short CMOS devices	Modeling and Characterization
236	On Increasing the Accuracy of Simulations of Deposition and Etching Processes Using Radiosity and the Level Set Method	Modeling and Characterization
240	Conduction and Noise Modelling of Submicronic Devices: Comparison Between ISE-TCAD Software and Microscopic Simulations	Modeling and Characterization
241	The RF potential of high-performance 100nm CMOS technology	Modeling and Characterization
243	A Novel General Direct Extraction Technique Used For a RF MOSFET Small-Signal Equivalent Circuit	Modeling and Characterization
244	Measurement of MOSFET LF Noise Under Large Signal RF Excitation	Modeling and Characterization
245	Comparative study of 1/f noise in bulk and SOI MOS devices	Modeling and Characterization
246	Investigation of the Extrinsic Base Effect on High Frequency Performance of SOI Lateral Bipolar Transistors (LBT)	Modeling and Characterization
248	CMOS circuit analysis with luminescence measurements and simulations	Modeling and Characterization
252	Unified 2D Short Channel Effects Model for Bulk CMOS FETs	Modeling and Characterization
253	Investigation on Convergence and Stability of Self-Consistent Monte Carlo Device Simulations	Modeling and Characterization
255	Physically-Based Matching Model for Deep-submicron MOS Transistors	Modeling and Characterization
258	Modeling of ballistic nanoscale MOSFETs	Modeling and Characterization

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263	Improvement in the prediction of Boron diffusion during a Spike Annealing for Ultra-Shallow Junctions	Modeling and Characterization
264	Tunnel Barrier Properties of Polycrystalline-Si Single-Electron Transistor	Modeling and Characterization
267	Benchmarking of Table Methods for MOSFET modelling	Modeling and Characterization
271	Influence of the Inner Miller-Effect on the Input Capacitance of CMOS Transistors	Modeling and Characterization
273	Scaling of MOSFET Transconductance with Gate Oxide Thickness and Effect of Remote Charge Scattering	Modeling and Characterization
276	Source/Drain Parasitic Resistance Role and Electrical Coupling Effect in sub 50nm MOSFET Design	Modeling and Characterization
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16	Automatic Order Reduction of Thermo-Electric Models for MEMS: Arnoldi versus Guyan	Sensors and Biosensors
23	Micromachined Mercury Sensor	Sensors and Biosensors
26	A CMOS Photodiode Array with Linearized Spectral Response and Spatially Distributed Light Intensity Detection for the Use in Optical Storage Systems	Sensors and Biosensors
49	An Ultra-Thin Polycrystalline-Silicon Thin-Film Transistor with SiGe Raised Source/Drain	Sensors and Biosensors
65	Clamped-Clamped Beam Micro-Mechanical Resonators in Thick-Film Epitaxial Polysilicon Technology	Sensors and Biosensors
69	Variable-Gain Inversion Layer Emitter Phototransistor in CMOS Technology	Sensors and Biosensors
71	LOW PINCH-OFF VOLTAGE AMORPHOUS SILICON JUNCTION FIELD-EFFECT TRANSISTOR: SIMULATION AND EXPERIMENT	Sensors and Biosensors
76	Photoelectric and Tensometric Properties of a Metal Phthalocyanine-Silicon Junctions	Sensors and Biosensors
83	Device Model of Integrated QWIP-HBT-LED Pixel for Infrared Focal Plane Arrays	Sensors and Biosensors
87	Fast polymer integrated circuits based on a polyfluorene derivative	Sensors and Biosensors
91	Integrated Si-based Opto-Couplers: a Novel Approach to Galvanic Isolation	Sensors and Biosensors
92	Numerical and Analytical Study of 6H-SiC Detectors with High UV Performance	Sensors and Biosensors
103	Thick Film Gamma Radiation Sensors with Sensitive Layers of NiO and La2O3–Fe2O3 Mixture	Sensors and Biosensors
110	Passive DNA Sensor with Gold Electrodes Fabricated in a CMOS Backend Process	Sensors and Biosensors
116	Numerical simulation of parameters of ZnCdHgTe films and	Sensors and Biosensors
117	Simulated influence of bulk traps on the subthreshold characteristics of an organic field effect transistor	Sensors and Biosensors
131	Monolithic Integration of a Novel Microfluidic Device with Silicon Light Emitting Diode-Antifuse and Photodetector	Sensors and Biosensors
139	Quantum Dot Materials and Devices for Light Emission in Silicon	Sensors and Biosensors
153	Integrated Photodiodes in Standard BiCMOS Technology	Sensors and Biosensors
156	Electron Transit Time Enhancement In Photodetectors For High Speed Imaging	Sensors and Biosensors
159	Photodetector with Internal Aiding Field Based-on GaAs/AlGaAs Heterostructures	Sensors and Biosensors
161	Novel small-dimension poly-Si TFTs with improved driving current and suppressed short channel effects	Sensors and Biosensors
169	Design of a Remote Control System for a Wireless Microrobot	Sensors and Biosensors
170	Optoelectronics properties of FTO/SRO/Si radiation sensors	Sensors and Biosensors
172	A Comparative Analysis of Active and Passive Pixel CMOS Image Sensors	Sensors and Biosensors
200	Volume shrinking in Micro-Fluidic Self-Assembly	Sensors and Biosensors
202	LaNixFe1-xO3 thin films: p-type ethanol sensors	Sensors and Biosensors
207	Hybrid metal-organic photodetectors based on a new class of metal-dithiolenes	Sensors and Biosensors

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212	Array-Based Electrical Detector of Integrated DNA Identification System for Genetic Chip Applications	Sensors and Biosensors
220	Bulk Wafer Defects Observable in Vision Chips	Sensors and Biosensors
222	Towards an Integrated Bulk/SOI Active Pixel APD Sensor: Bulk Substrate Inspection with Geiger Mode Avalanche Photodiodes	Sensors and Biosensors
254	A CMOS Compatible Single-Photon Avalanche Diode	Sensors and Biosensors
260	A Biosensor for Direct Detection of DNA Sequences Based on Capacitance Measurements	Sensors and Biosensors
274	A Novel MEMS Technological Platform Aimed at RF Applications	Sensors and Biosensors