Investigation of performance improvement and gate-to-junction leakage reduction for the 90nm CMOS gate stack architeture.

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Abstract

An investigation of the gate stack for 90nm gate length CMOS is presented. The optimised 90nm nMOS and pMOS transistors exhibit state of the art DC and switching characteristics. Nominal nMOS and pMOS drive currents of 760μA /μm and 320μA /μm with an Ioff state current of 2nA /μm (V_{DD} =1.2V) have been realized. An inverter delay of 15ps at 1.2V operating voltage has also been measured.

1. Introduction

The gate stack architecture continues to be a key component in optimising device performance. Due to the unavailability of a mature high-k material, gate leakage remains a critical problem in scaling the gate dielectric. In addition to the scaling of the gate dielectric, proper gate activation of both nMOS and pMOS gates while keeping the boron penetration in the pMOS case under control, is also imperative for achieving improved device performance.

One specific gate leakage mechanism that becomes more dominant when reducing the gate oxide thickness is the gate to junction leakage when the drain is biased with all other terminals grounded (nMOS of inverter with input equal to "0"). As the gate dielectric thickness reduces to below 1.8nm, the gate to junction leakage becomes comparable to the conventional source-drain short channel leakage.

This paper investigates the effect of different gate electrode materials (as deposited poly and amorphous gates), different gate electrode thicknesses (150nm versus 100nm) and different gate re-oxidation recipes, on gate activation, gate to junction leakage and overall performance.

2. Experiment

CMOS transistors with gate lengths down to 60nm were fabricated. Shallow trench isolation was used for isolation. Well and channel implants were performed through a 20nm thermal oxide. The gate stack consisted of 1.5nm target thicknesses for the gate dielectric and either 150nm or 100nm for the gate electrode thickness. As deposited poly silicon and amorphous silicon were investigated. A 1.5nm furnace oxide grown in NO was processed as the reference wafer while all other wafers received a 1.5nm Rapid Thermal Oxidation (RTO) followed by a Remote Plasma Nitridation (RPN) step. Special DUV lithography was applied at the gate level to pattern gates down to 60nm – 70nm from 130nm design values on the mask. After gate etch, the wafers received one of the experimental sidewall oxidation recipes. The experimental sidewall recipes were:

a) A 0.8nm furnace oxidation in O_2 performed at 550°C
b) A 3.5nm In-Situ Steam Generated (ISSG) oxidation at 1000°C
c) A 3.5nm ISSG oxide followed by a RPN treatment.

Extension junctions and pocket implants were performed after the sidewall oxidation. Some wafers also received a 1000°C, 1 second anneal to reduce the defects from the extension and pocket implants and therefore reduce the amount of transient enhanced diffusion during the spacer thermal budget. A standard "D" shaped nitride spacer was formed. The deep junctions were implanted, and the NMOS devices received an additional phosphorous co-implant to help improve the gate dopant activation. An 1100°C spike anneal was used for dopant activation. Cobalt silicidation was performed using a 10nm/8nm layer of Cobalt/Titanium. Processing was completed up to level 1 metal.

3. Results and discussion

The I_{off}-I_{on} characteristics of the nMOS and pMOS transistors with poly or amorphous gate electrodes and different gate re-oxidation recipes are compared in Figure 1 and Figure 2, respectively.

As expected it can be clearly observed that the performance for both nMOS and pMOS devices is significantly better for a poly gate electrode. This is consistent with previous reports [1],[2], that the activation of the as deposited poly gate is much better than that of the as deposited amorphous gate for a fixed thermal budget. This is proved in Figure 3 in which the inversion parts of the nMOS and pMOS CV curves are shown. To activate the amorphous gate properly, a higher thermal budget would be necessary. The lower thermal budget for the activation of poly gates is favourable especially from the point of view of minimising the Short Channel Effects (SCE).

The various sidewall oxidation recipes have no significant effect on the off-state versus on-state characteristics.

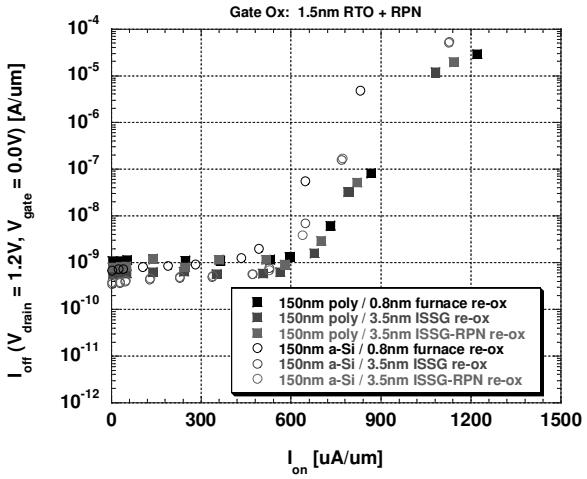

Figure 1 NMOS off-state current versus on-state current at 1.2V. Poly and amorphous gate morphology are compared with the different sidewall oxidation recipes. Each marker represents an average of at least 20 measurements for a given gate length.

No significant difference can be observed in the nMOS I_{off}-I_{on} characteristics for 150nm versus 100nm thick poly or amorphous gates and 3 different gate re-oxidations (see Figure 4). However, as can be seen from Figure 5, for pMOS transistors with a 150nm thick gate electrode appears to be substantially better. Boron penetration and HDD implant penetration are two probable reasons for poor performance of the 100nm thick gate electrodes.

Figure 6 and Figure 7 illustrate the measured gate to junction leakage for nMOS and pMOS devices, respectively. The horizontal scale is determined from SEM measurements after gate etch and strip. The almost constant value of the leakage independent of gate length proves that it is indeed localised in the gate to junction overlap region. It can be seen that the gate to junction leakage is lower for amorphous gates, especially in case of pMOS transistors. Comparing Figure 6 and Figure 7 with Figure 1 and Figure 2, we may draw a conclusion that the nMOS I_{off} current is already determined by this gate to junction leakage while the pMOS I_{off} current is dominated by the junction leakage.

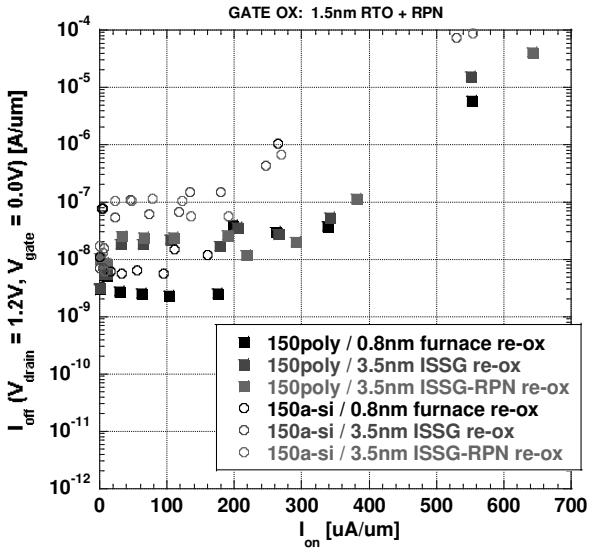

Figure 2 PMOS off-state current versus on-state current at -1.2V. Poly and amorphous gate morphology are compared with the sidewall oxidation recipes. Each marker represents an average of at least 20 measurements for a given gate length.

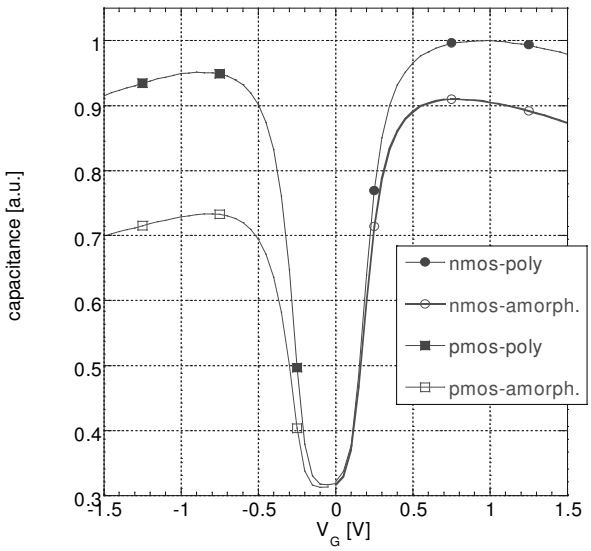

Figure 3 Comparison of the inversion parts of the CV curves measured on the nMOS and pMOS transistors from Figure 1 and Figure 2.

This observation proves that the gate to junction leakage starts to play an important role in device optimisation. The obvious way to minimise this leakage for the same oxide thickness is to minimise the gate to

extension junctions overlap area. This can be achieved for example by using shallower extension junctions, off-set spacers or notched gates [3]. Another way, investigated in this paper is to use a thicker re-oxidation. This should lead to a small off-set of the extension junctions as well as to a local thickening of the gate oxide at the gate edge. Both these effects should lead to a reduction of the gate to junction leakage.

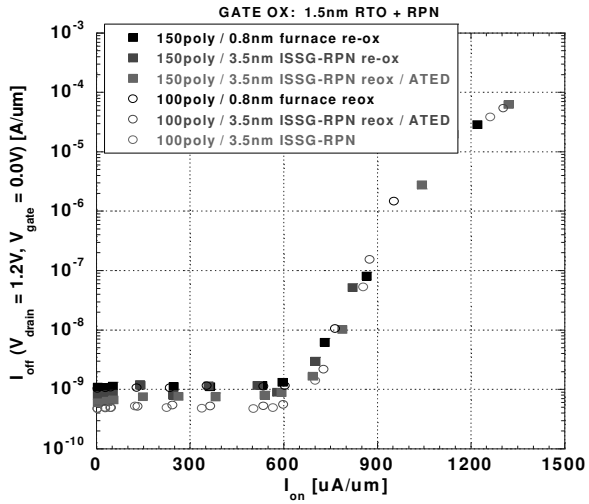

Figure 4 NMOS off-state current versus on-state current at 1.2V. The comparison is for 150nm poly silicon gate electrode thickness versus 100nm poly silicon gate electrode thickness. Each marker represents an average of at least 20 measurements for a given gate length.

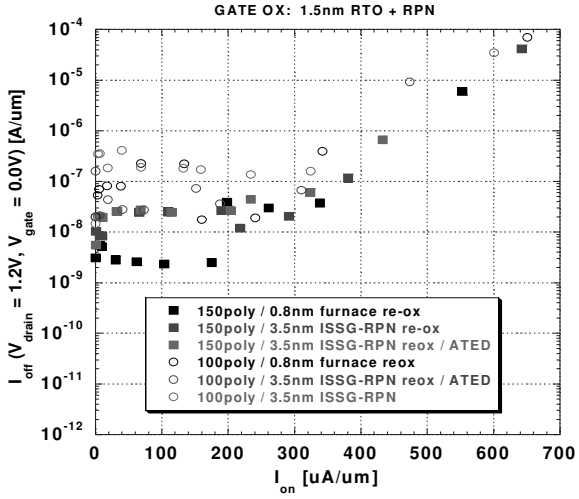

Figure 5 PMOS on-state current versus off-state current at -1.2V. The comparison is for 150nm poly silicon gate electrode thickness versus 100nm poly silicon gate electrode thickness. Each marker represents an average of at least 20 measurements for a given gate length.

Expected tendencies can be observed in case of nMOS and pMOS transistors with amorphous gates, but not for pMOS transistors with poly gate.

The V_T as function of the physical gate length (measured after gate etch by SEM) of the nMOS and pMOS transistors with the optimised gate stack can be found in Figure 8. I_{off} as a function of I_{on} characteristics can be seen in Figure 9.

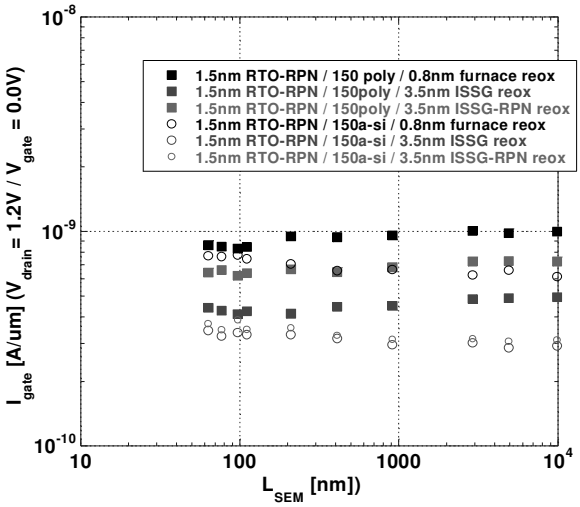

Figure 6 NMOS gate to junction leakage current at V_{drain} = 1.2V (V_{gate} = V_{source} = V_{well} = 0). The comparison is for 150nm poly silicon gate electrode thickness versus 100nm poly silicon gate electrode thickness and different sidewall oxidation recipes. Each marker represents an average of at least 20 measurements for a given gate length.

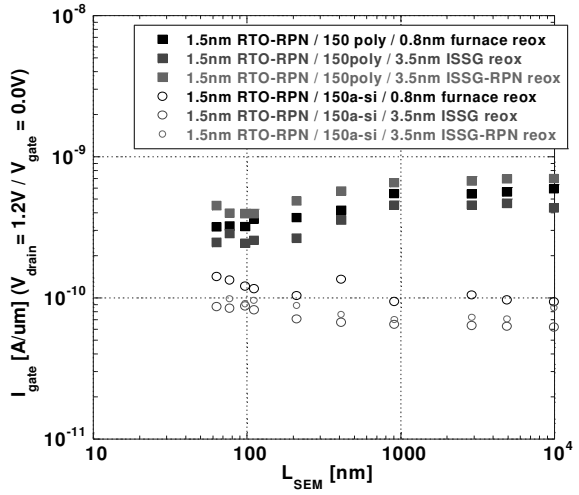

Figure 7 PMOS gate to junction leakage current at V_{drain} = -1.2V (V_{gate} = V_{source} = V_{well} = 0). The comparison is for 150nm poly silicon gate electrode thickness versus 100nm poly silicon gate electrode thickness and different sidewall oxidation recipes. Each marker represents an average of at least 20 measurements for a given gate length.

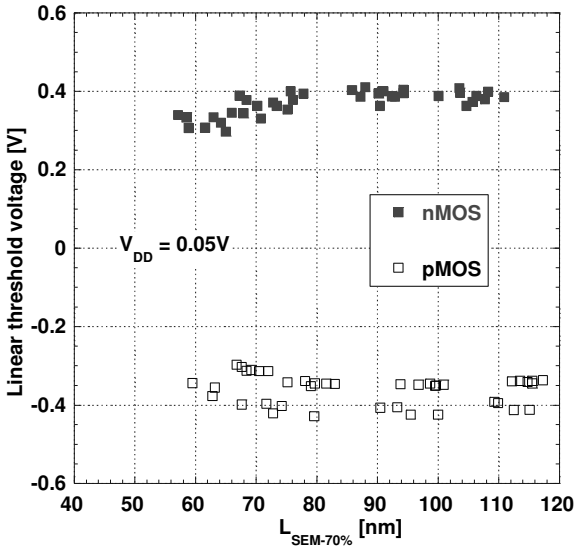

Figure 8 nMOS and pMOS $V_T = f(L_G)$ characteristics for the optimised gate conditions.

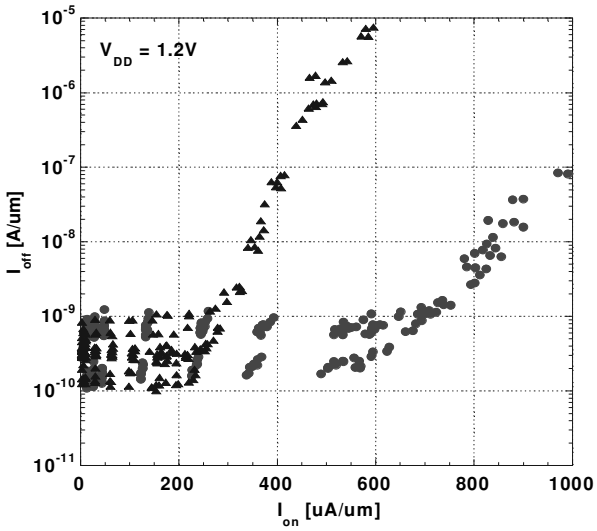

Figure 9 $I_{off} - I_{on}$ characteristics of the optimised nMOS and pMOS transistors measured for V_{DD} = 1.2V.

The nMOS and pMOS I_D-V_G characteristic of transistors with L_G = 90nm are presented in Figure 10 and ring oscillator gate delay as a function of dissipated energy in Figure 11.

4. Conclusions

A gate stack optimisation strategy from the point of view of minimising the gate to junction leakage and optimising the gate activation was presented. Poly gate electrodes (as deposited) exhibit significantly better gate activation as compared to amorphous gate electrodes. 3.5nm gate re-oxidation yields a reduction in gate-to-junction leakage relative to the 0.8nm re-oxidation. Sidewall oxidation on amorphous material also yields lower gate to junction leakage; however the device performance is much worse with amorphous gate electrodes.

The optimised nMOS and pMOS transistors with 90nm gate length exhibit very good dc and switching performance.

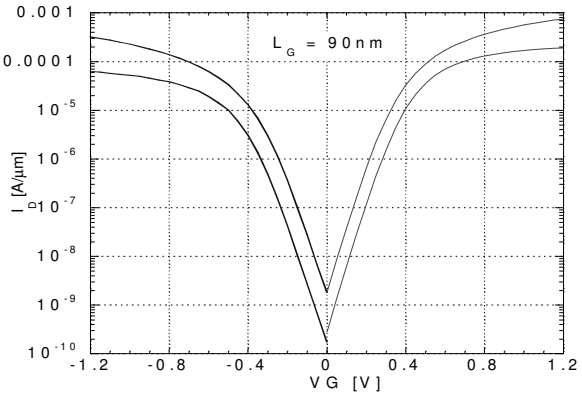

Figure 10 I_D-V_G characteristics for LG = 90nm, nMOS and pMOS.

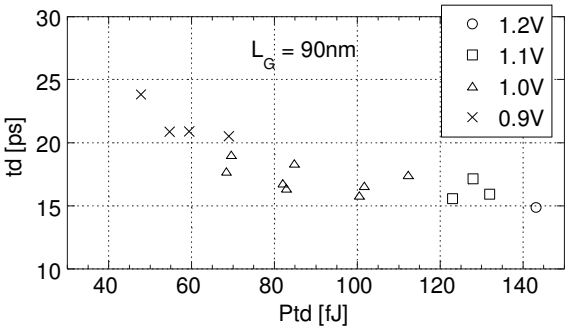

Figure 11 Ring oscilator delay as function of energy for L_G = 90nm.

Acknowledgements

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