Fabrication of 0.1-μm pMOSFETs with SiGe-Channel and Elevated B-Doped SiGe Source and Drain Layers

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Abstract

Buried $Si_{1-x}Ge_x$-channel (x=0-0.5) pMOSFETs with near 0.1 μm gate length have been successfully fabricated using a super self-aligned ultra-shallow junction formation technique, which is consisted of the selective in-situ B-doped $Si_{0.55}Ge_{0.45}$ epitaxy on source/drain by CVD and subsequent thermal diffusion of B from B-$Si_{0.55}Ge_{0.45}$ film into substrate. Normal saturation characteristics and fairly good current drivability are observed. It is found that, although the $Si_{1-x}Ge_x$-channel pMOSFET is a buried channel type, its short channel effect is well suppressed, compared with conventional surface-channel Si pMOSFETs. This is considered to be due to the ultra-shallow junction depth estimated adjacent just below the SiGe/buffer Si interface, and due to suppression of drain and source depletion-layer widths into the SiGe channel, which is originated from energy-band-gap narrowing by introducing Ge.

1. Introduction

In order to realize the optimised MOSFET structure with sub-0.1-μm gate length, a new junction formation process such as the super self-aligned ultra-shallow junction formation technique instead of the conventional ion implantation method is essential. In the devices fabricated with such a new technique, the precise diffusion control of dopant is extremely important because the source/drain punch-through, which is an especially crucial problem for those devices, should be suppressed [1-2]. Moreover, the improvement of the effective carrier mobility in the channel region is also indispensable. By the confinement of holes in the strained $Si_{1-x}Ge_x$ quantum well, separated from the gate oxide by a thin Si spacer layer, hole mobility can be improved due to the lower effective mass in $Si_{1-x}Ge_x$ and movement away from scattering sites at the Si/SiO_2 interface [3]. It has been reported that the introduction of the high quality $Si_{1-x}Ge_x$ with x=0.5 in the channel region leads to a drastic improvement of the pMOSFET performance [4-5].

In this study, we report that $Si_{1-x}Ge_x$-channel (x=0-0.5) 0.1-μm pMOSFETs with super self-aligned ultra-shallow junction formed by selective in-situ B-doped $Si_{0.55}Ge_{0.45}$ chemical vapor deposition (CVD) have been successfully realized. The schematic device structure is shown in Fig. 1. Furthermore, it is clarified that the short channel effect is sufficiently suppressed for $Si_{1-x}Ge_x$-channel devices, compared with conventional surface-Si-channel devices, because of the ultra-shallow junction depth.

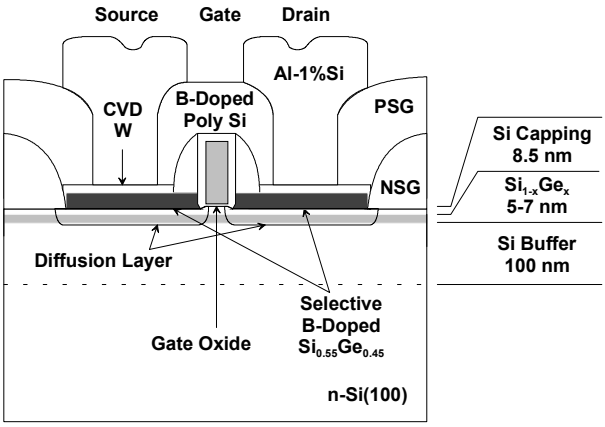

Fig. 1. Schematic cross section of $Si_{1-x}Ge_x$-channel super self-aligned ultra-shallow junction electrode pMOSFET (S^3EMOSFET).

2. Fabrication process

Typical $Si_{1-x}Ge_x$-channel pMOSFETs fabrication process using a self-aligned poly Si gate is shown in Fig. 2. High quality $Si/Si_{1-x}Ge_x$ (x=0-0.5)/Si heterostructure was deposited on 1-2 Ωcm n-type Si(100) surface utilizing an ultra-clean hot-wall low-pressure CVD (LPCVD) system, which was made ultra-high vacuum compatible with gate valves and a turbo-molecular pump system [4-5]. After the buffer Si deposition at 750°C, the 5~7-nm-thick $Si_{1-x}Ge_x$ layer was deposited at 450-500°C using a SiH_4-GeH_4-H_2 gas system with subsequent 10-nm-thick capping Si deposition at 500°C. The total pressure for $Si_{1-x}Ge_x$ and capping Si deposition was

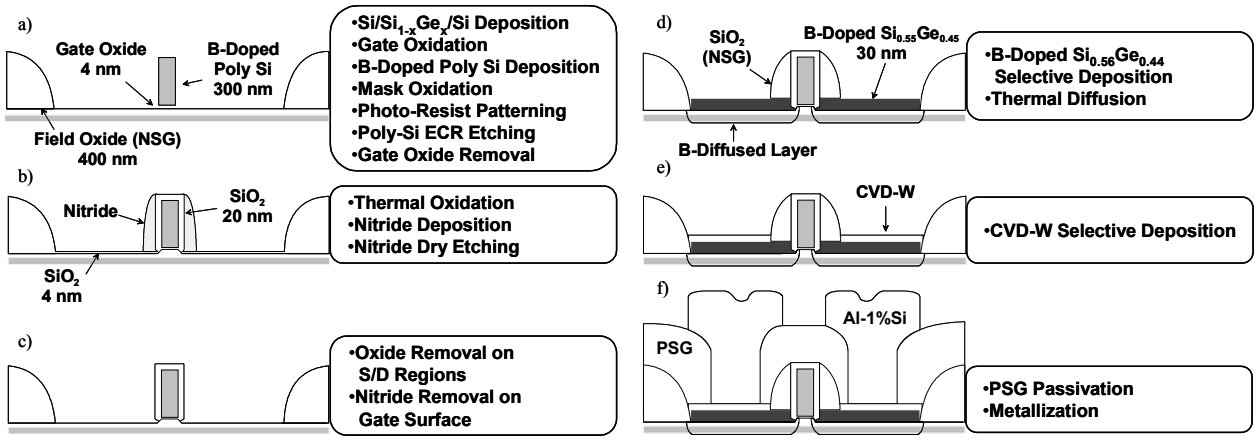

Fig. 2. Typical fabrication process of S^{3}EMOSFET.

about 30 Pa and the partial pressures of SiH_4 and GeH_4 were 6 and 1-1.5 Pa, respectively, with H_2 carrier. The Ge fraction and the thickness of $Si/Si_{1-x}Ge_x/Si$ heterostructure were evaluated by four-crystal X-ray diffraction technique and subsequent simulation. A 400-nm-thick field oxide was formed on the heterostructure at 400^{o}C by CVD and a thermal gate oxide with 4-nm thickness was grown by wet oxidation at 700^{o}C. Then, 300-nm-thick in-situ B-doped polycrystalline Si was deposited using a Si_2H_6-B_2H_6-H_2 gas system by LPCVD at 550^{o}C followed by thermal wet oxidation at 700^{o}C to form a 20-nm-thick etching mask. The mask was patterned by photolithography using a stepper and the gate length reduction was done by resist-ashing with oxygen plasma. After the mask oxide was etched in a wet chemical solution, the poly Si was dry etched by highly selective electron-cyclotron-resonance (ECR) Cl plasma [6], and then the gate oxide on the source/drain (S/D) was removed (Fig. 2-a). A 700^{o}C wet thermal oxidation is conducted to form a thin oxide around the gate poly Si and on the S/D. Due to the impurity concentration difference, the oxide thickness on B-doped poly Si and S/D surfaces were different as 20 nm and 4 nm, respectively. Next, the 30-nm-thick nitride film was deposited by LPCVD at 700^{o}C using a SiH_4-NH_3-N_2 gas system, followed by anisotropic nitride removal on the S/D regions using reactive-ion-etching (Fig. 2-b). By wet etching, the oxide on S/D regions was removed, and so did the nitride on the gate sidewalls (Fig. 2-c). Then, the 30-nm-thick in-situ B-doped $Si_{0.55}Ge_{0.45}$ was selectively deposited on the S/D regions at 550^{o}C by LPCVD using a SiH_4-GeH_4-B_2H_6-H_2 gas system [7-8]. Subsequently, the 200-nm-thick CVD SiO_2 was deposited at 400^{o}C, and the thermal diffusion was conducted at 750^{o}C for 3 hours in Ar atmosphere to form an ultra-shallow junction. After the CVD SiO_2 was dry etched as shown in Fig. 2-d, tungsten was selectively deposited by CVD on the B-doped $Si_{0.55}Ge_{0.45}$ surfaces using a WF_6-SiH_4-Ar gas system in order to reduce the S/D series resistance (Fig. 2-e) [1-2]. The CVD-W deposition temperature was 200^{o}C after 500^{o}C preheating to suppress wormhole failures (i.e., destruction of p-n junctions by W penetration) [9]. Then, the phosphosilicate glass passivation was conducted by CVD and holes were opened for contacts. Al-1%Si was sputtered at this stage and patterned (Fig. 2-f).

3. Results and discussion

Typical drain-current-voltage characteristics and subthreshold behaviour of a $Si_{0.5}Ge_{0.5}$-channel pMOSFET with a gate length of 0.12 μm are shown in Figs. 3-a and 3-b. The cross-sectional SEM micrograph of the 0.12-μm $Si_{0.5}Ge_{0.5}$-channel S^{3}EMOSFET is also shown in Fig. 3-c. The maximum saturation drain current (I_D) is estimated as about 620 μA/μm at the gate voltage (V_G) = the drain voltage (V_D) = -2 V, and the subthreshold slope as about 89 and 130 mV/decade at V_D = -50 mV and -1.5 V, respectively. The subthreshold slope of the $Si_{0.5}Ge_{0.5}$-channel devices with longer gate lengths than 0.12 μm, for example 0.16 μm, is smaller than 77 mV/decade even at V_D= -1.5V. The drain current drivability of the $Si_{1-x}Ge_x$-channel S^{3}EMOSFETs with a Ge fraction of 0.4 or 0.5 and with a gate length of 0.51 or 0.46 μm, respectively, is significantly improved by a factor of about 30%, compared with the conventional Si-channel device with a 0.51-μm gate length (Fig. 4-a), and their maximum linear transconductance ($g_{m\ max}$) at V_D = -50 mV is enhanced by about 65% (Fig. 4-b). It suggests that the effective mobility of holes in the $Si_{1-x}Ge_x$-channel significantly increases compared with that in the surface-Si-channel as reported earlier [3-5].

Typical quasi-static capacitance-voltage (*C*-*V*) characteristics for 50 x 50 μm^2 MOS capacitor with Si or $Si/Si_{0.6}Ge_{0.4}/Si$ heterostructure, which suffered the entire S^{3}EMOSFET fabrication processes, reveals the plateau in the inversion region indicating that holes appear in the $Si_{0.6}Ge_{0.4}$ quantum well (Fig. 5). It has been reported [10-11] that the band gap of strained $Si_{1-x}Ge_x$ decreases with increasing Ge fraction mainly by the valence band offset. Therefore, it is considered that the threshold voltage (V_T) is strongly related to the band gap of $Si_{1-x}Ge_x$ layer [5]

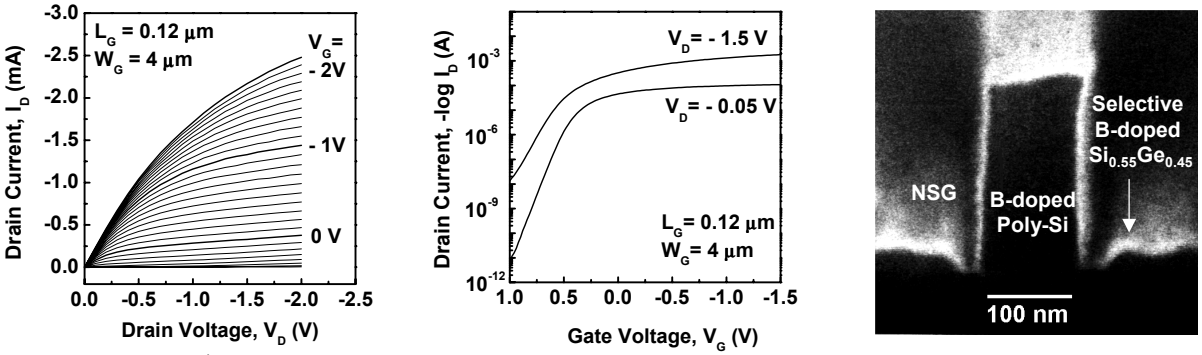

Fig. 3. Typical a) I_D-V_D, b) I_D-V_G characteristics and c) the cross-sectional SEM micrograph of 0.12-μm $Si_{0.5}Ge_{0.5}$-channel S^3EMOSFET.

and the V_T decreases with increasing Ge fraction of $Si_{1-x}Ge_x$-channel as shown in Fig. 4-c.The dependences of threshold voltage on gate length of the $Si_{1-x}Ge_x$-channel S^3EMOSFETs are shown in Fig. 6 with Ge fraction as a parameter. It is found from the figure that the roll-off characteristics are improved for the $Si_{1-x}Ge_x$-channel MOSFETs, compared with the conventional Si-channel MOSFETs. The dependences of V_T on V_D for the $Si_{1-x}Ge_x$-channel devices with a nearly equal gate length are shown in Fig. 7. It is observed from Fig. 7 that the dependences are suppressed for the $Si_{1-x}Ge_x$-channel S^3EMOSFETs, compared with the Si-channel MOSFETs. These results indicate that, although the $Si_{1-x}Ge_x$-channel MOSFET is a buried-channel type, the short channel effect in the $Si_{1-x}Ge_x$-channel S^3EMOSFETs is well suppressed compared to the surface-channel type of Si-channel devices. This is due to the ultra-shallow junction depth and the suppression of the drain and source depletion-layer widths into the SiGe channel, as explained following. From the *I-V* characteristics of the p^+-drain/n-substrate junction of S^3EMOSFETs with various thicknesses of capping Si and $Si_{1-x}Ge_x$ layers, the junction depth was inferred to be about 20 nm, which is extremely shallow, i.e., slightly below the $Si_{1-x}Ge_x$/buffer Si interface. Under the gate voltage condition of threshold voltage, the junction between the drain (or the source) and the channel is located in the junction of the p^+-SiGe drain (or the p^+-SiGe source) and the buried SiGe-channel for the $Si_{1-x}Ge_x$-channel MOSFETs. On the other hand, the junction between the drain (or the source) and the channel is located in the junction of the p^+-Si drain (or the p^+-Si source) and the surface Si-channel for the conventional Si MOSFETs. Therefore, the drain (or the source) depletion layer width into the channel region is narrower in the $Si_{1-x}Ge_x$-channel MOSFETs, compared with the conventional Si MOSFETs, which is due to the reduction of the energy band gap by introducing Ge. Therefore, despite the buried channel type, short channel effects are well suppressed in the $Si_{1-x}Ge_x$-channel MOSFETs.

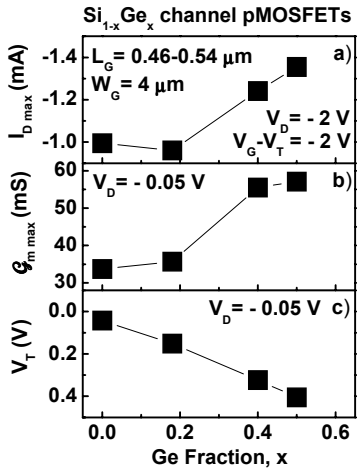

Fig. 4. Dependences of a) maximum saturation drain current, b) maximum linear transconductance and c) threshold voltage on the Ge fraction of the $Si_{1-x}Ge_x$-channel S^3EMOSFETs.

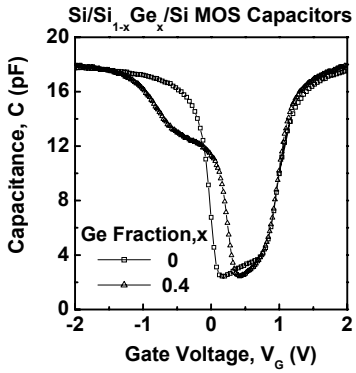

Fig. 5. Typical quasi-static *C-V* curves of the n-Si and the $Si/Si_{0.6}Ge_{0.4}$/n-Si MOS capacitors. Gate material is B-doped polycrystalline Si with 300-nm thickness, and the gate area is 50 x 50 μm^2. The gate oxide thickness is about 4 nm. The substrate is n-Si(100) with 1 x 10^{15} cm^{-3} doping.

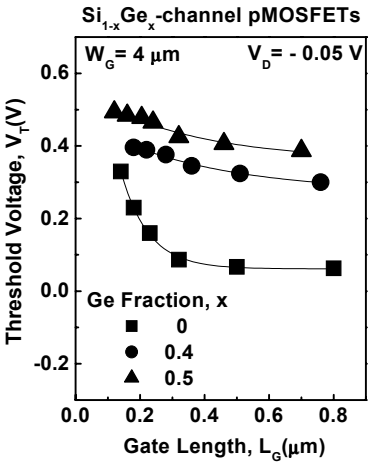

Fig. 6. Dependences of the threshold voltage when V_D = -50 mV on the gate length of the $Si_{1-x}Ge_x$-channel S^3EMOSFETs.

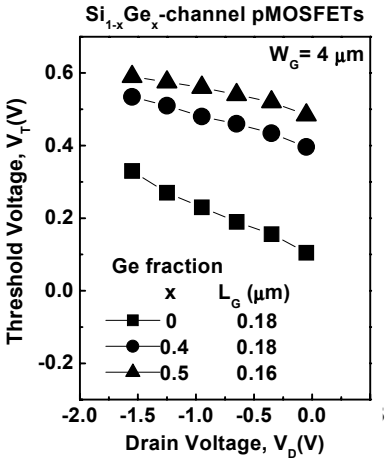

Fig. 7. Threshold voltage dependences upon the drain voltage in the $Si_{1-x}Ge_x$-channel S^3EMOSFETs.

4. Conclusion

We have successfully fabricated 0.1-μm gate $Si_{1-x}Ge_x$-channel pMOSFETs using a super self-aligned ultra-shallow junction formation technique, which consists of the selective in-situ B-doped $Si_{0.55}Ge_{0.45}$ epitaxy on source/drain by CVD and subsequent thermal diffusion to form a shallow junction electrode. The $Si_{0.5}Ge_{0.5}$-channel S^3EMOSFET shows high current drivability. Despite the buried-channel type, the increase in threshold voltage with the reduction of gate length and the decrease in drain voltage are suppressed in the $Si_{1-x}Ge_x$-channel devices, compared with conventional surface-channel Si MOSFETs. The suppression of short channel effects is originated from the ultra-shallow junction depth, and the suppression of the drain and source depletion-layer widths into the SiGe channel due to energy-band-gap narrowing by introducing Ge.

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References

[1] J. Murota, M. Ishii, K. Goto, M. Sakuraba, T. Matsuura, Y. Kudoh and M. Koyanagi, "Fabrication of 0.1μm MOSFET with super self-aligned ultrashallow junction electrodes using selective $Si_{1-x}Ge_x$ CVD", *Proc. of the 27th ESSDERC*, Germany, September 22-24,1997, pp. 376-379.

[2] T. Yamashiro, T. kikuchi, M. Ishii, F. Honma, M. Sakuraba, T. Matsuura, J. Murota and T. Tsuchiya, "Super self-aligned technology of ultra-shallow junction in MOSFETs using selective $Si_{1-x}Ge_x$ CVD", *Mater. Sci. Eng*., **B89** (2002) pp 120-124.

[3] P. M. Garone, V. Venkataraman and J. C. Sturm, "Hole mobility enhancement in MOS-gated Ge_xSi_{1-x}/Si heterostructure inversion layers", *IEEE Electron Device Lett*., **13** (1992) pp. 56-58.

[4] J. Murota and S. Ono, "Low-temperature epitaxial growth of Si/$Si_{1-x}Ge_x$/Si heterostructure by chemical vapor deposition", *Jpn. J. Appl. Phys.*, Pt. 1, **33** (1994) pp. 2290-2299.

[5] K. Goto, J. Murota, T. Maeda, R. Schürtz, K. Aizawa, R. Kircher, K. Yokoo and S. Ono, "Fabrication of a $Si_{1-x}Ge_x$ channel MOSFET containing high Ge fraction layer by low-pressure chemical vapor deposition", *Jpn. J. Appl. Phys.*, Pt. 1, **32** (1993) pp 438-441.

[6] T. Matsuura, H. Uetake, T. Ohmi, J. Murota, K. Fukuda, N. Mikoshiba, T. Kawashima and Y. Yamashita, "Directional etching of Si with perfect selectivity to SiO_2 using an ultraclean electron cyclotron resonance plasma", *Appl. Phys. Lett.*, **56** (1990) pp. 1339-1341.

[7] F. Honma, J. Murota, K. Goto, T. Maeda and Y. Sawada, "Ultrashallow Junction Formation Using Low-Temperature Selective $Si_{1-x}Ge_x$ Chemical Vapor Deposition", *Jpn. J. Appl. Phys.*, Pt. 1, **33** (1994) pp. 2300-2303.

[8] J. Murota, Y. Takasawa, H. Fujimoto, K. Goto, T. Matsuura and Y. Sawada, "Low-temperature epitaxial growth mechanism of $Si_{1-x}Ge_x$ films in the silane and germanium reactants", *J. Phys. IV France*, **5** (1995) pp. C5-1165-1172.

[9] Y. Yamamoto, T. Matsuura and J. Murota, "H-termination effects on intial growth characteristics of W on Si using WF_6 and SiH_4 gases", *J. Phy. IV France*, **9** (1999) pp. Pr8-431-436.

[10] R. Braunstein, A. R. Moore and F. Herman, "Initial optical absorption in germanium-silicon alloys", *Phys. Rev.*, **109** (1958) pp. 695-710.

[11] R. People, " Indirect band gap of coherently strained Ge_xSi_{1-x} bulk alloys on <001> silicon substrates", *Phys. Rev. B*, **32** (1985) pp. 1405-1408