A Viable Self-aligned Bottom-Gate MOSFET Technology for High Density and Low Voltage SRAM

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Abstract

This paper reports the implementation of the bottom-gate MOSFET which possesses the following fully-self-aligned structural features: 1) self-aligned source/drain to bottom-gate; 2) self-aligned thick source/drain to thin channel; 3) self-aligned and mask-free lightly-doped-drain (LDD). The complete self-alignment is realized by combining a conventional ion implantation and a subsequent CMP step. The process is applied to the poly-Si film, which is crystallized from an a-Si film deposited by LPCVD using Metal-Induced Uni-lateral Crystallization (MIUC) technique and is grain-enhanced further in a high temperature annealing step. Deep sub-micron Fully Self-Aligned Bottom-Gate (FSABG) PMOS transistors with channel length less than 0.5 μm are fabricated. The measured performance parameters include threshold voltage of -0.43V, subthreshold swing of 113 mV/dec, effective hole mobility of 147 cm^2/V-s, off-current of 0.17 pA/μm and on-off current ration of 7.1×10^8.

1. Introduction

Static random access memories (SRAMs) have been widely used for L1 and L2 caches due to their superior speed performance [1]. The 6-transistor cell in the SRAMs has been the dominating architecture due to its large static noise margin and good compatibility to CMOS process. The implementation of the 6-transistor cell can utilize either full CMOS or 3D architecture. The former has the advantages of low-power consumption and high stability at low supply voltage, but requires larger cell area. The latter using 2 stacked load transistors (TFTs) combines the low-power advantage of the full CMOS cell and the high-density advantage of a resistor-load. However, the stability of the load-stacked cell degrades with power supply voltage scaling due to the poor load-transistor performance. Besides material issue, one major reason for the poor load-transistor is the use of bottom-gate structure for high circuit density and good topography [2]. The bottom-gate structure results in significant performance variations when device dimension is scaled into deep sub-micron regime due to its nonself-aligned process [3]. Over the years, various efforts have been made to improve the performance of both top and bottom gate devices [4]-[7]. However, to the best of our knowledge, no self-aligned bottom-gate device with performance comparable to single crystal MOSFET has been proposed so far.

In this paper, a simple self-aligned bottom-gate MOSFET technology is proposed. The method for realizing the self-alignment is described in detail. The device results are analyzed and discussed.

2. Device Fabrication

The key processing steps are shown in Fig.1. Silicon wafers with 5000 Å of thermally grown oxide were used as starting substrates. A 2500 Å of amorphous silicon film was deposited at 550 °C by LPCVD as bottom-gate material. The film was heavily doped with boron by ion implantation, and subsequently patterned. The gate oxide was then grown at 850 °C after a 500 Å LTO spacer formation by LTO deposition and subsequent etch-back. Following that, a 3000 Å a-Si film and a 200 Å LTO were deposited by LPCVD. The a-Si film was doped with BF_2 by implantation as shown in Fig. 1(a). The dose and energy are 3×10^{15} cm^{-2} and 45 KeV respectively. After removing the LTO screen, chemo-mechanical polish (CMP) was performed for a total time of 100 seconds to smooth down the surface as shown in the Fig. 1(b). In the process, the elevated portion of the a-Si on the gate was thinned first. It took less than 50 seconds to planarize the step even though the amount of a-Si removed is 2500 Å high. Once the surface is planarized, the a-Si removal rate is significantly reduced to about 200 Å/minute because whole a-Si covering the entire wafer is being polished at this stage. The remaining a-Si on the gate served as device channel and its thickness was about 300 Å after the CMP step. The huge removal rate difference before and after the surface planarization plays a similar role to the conventional polish stop, offering a good controllability to the channel region thickness. The simulated boron concentration at the top surface of the channel region is less than 1×10^{14} cm^{-3}. The a-Si film was then recrystallized using a low temperature Metal (Ni) Induced Uni-lateral Crystallization (MIUC) process as shown in Fig. 1(c). The MIUC process consists of the deposition of a 4000Å LTO, the opening of a 2 μm wide seeding window, the evaporation of a 50 Å Nickel film, and the annealing at 550°C for 24 hours in nitrogen ambient. The unconsumed Nickel and the LTO were then removed.

The full details of the MIUC process can be found in [7]. Afterwards, As+ implantation with 350 Å LTO as screen was performed to adjust threshold voltage as shown in Fig. 1(d). The implant dose and energy are 1×10^{12} cm^{-2} and 33 KeV respectively. A high temperature annealing was then carried out at 850 °C for half an hour in oxygen ambient after the active area definition. The thickness of the channel region was reduced to about 250 Å and the grain size was significantly enlarged after the oxidation step. The dopant concentration along the direction from source to drain at 150 Å away from top surface was simulated and plotted in Fig. 2. Note that self-aligned symmetric LDD was also formed. The lower boron concentration at the LDD region was caused by the thicker a-Si film at the two edges of the gate as shown in Fig. 1(a). In thus, a number of self-alignment features are achieved including: 1) self-aligned source/drain doping to gate; 2) self-aligned thick source/drain and thin channel to gate; 3) self-aligned and mask-free LDD. The SEM photograph of the devices at this step is shown in Fig. 3. Finally, the process was completed with conventional back-end steps. The entire process only requires 4 masks, no more than that for the conventional top-gate MOSFET. Conventional non-self-aligned bottom-gate (NSABG) MOS transistors were also fabricated in the same run for comparison. An additional mask was used for the source/drain doping and channel region definition in the NSABG process.

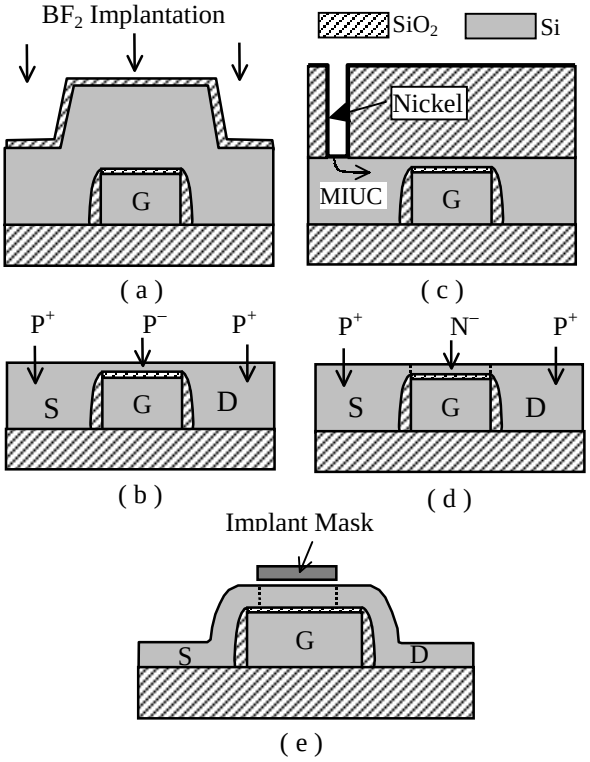


Fig. 1. Key fabrication steps of the p-channel FSABG MOS transistor (steps a to d) and the formation of NSABG MOS transistor (step e).

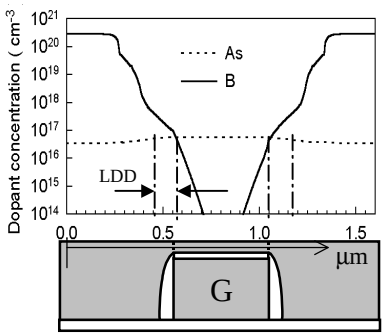


Fig. 2. The dopant concentration along the direction from source to drain at 150 Å away from the top surface after the high temperature annealing.

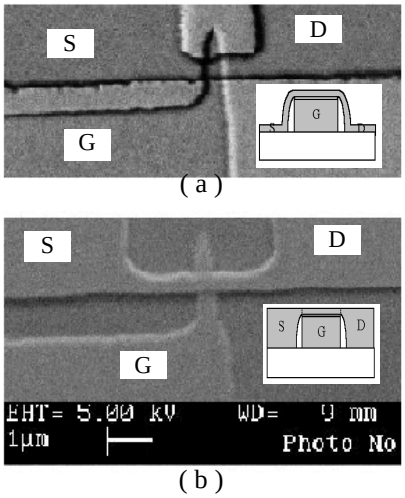


Fig. 3. Bird-eyed views of the fabricated transistors. (a) Non SABG, (b) FSABG.

The misalignment errors could be very large due to the outdated facility (contact alignment) used in this work. For the fair comparison, the bottom-gate length of the non-self-aligned device was drawn longer than channel length as showed in Fig. 1(e) to ensure that the entire channel region is gated.

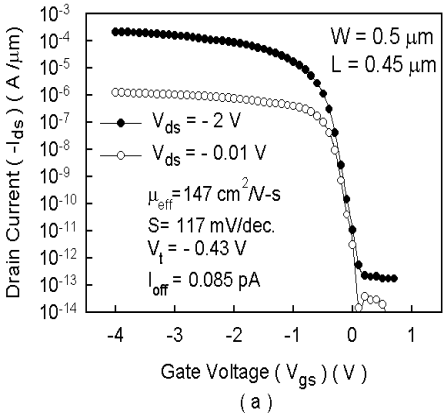
3. Results and Discussions

Fig. 4 shows the measured transfer and output characteristics of a fabricated p-channel FSABG-MOS transistor. The gate length (L), gate width (W), gate oxide thickness (T_{OX}), and Si film thickness (T_{Si}) in the channel region are 0.45 μm, 0.5 μm, 131 Å, and 250 Å, respectively. The effective mobility, subthreshold slope, threshold voltage, off-current and on-off current ratio of the FSABG PMOSFET are measured to be 147 cm^2 /V-s, 113 mV/dec, –0.43V, 0.085 pA and 7.1×10^8, respectively. The performance is a little inferior to that of the conventional bulk or SOI PMOSFET (top-gate) which usually has a mobility of 200~300 cm^2/V-s and

subthreshold swing of 70~90 mV/dec. This is caused by the imperfect crystal silicon quality and higher interface trap density of the MIUC silicon film used to fabricate the devices in this work. The MIUC film usually contains some grain boundaries that results in the smaller mobility. It is believed that the SOI-like device performance can be recovered by further device scaling [8]. In addition, the interface of the bottom-gate device was formed by the deposition process. The deposited interface usually has more interface traps than the conventional thermally oxidized interface. The higher trap density is responsible for the gentler sub-threshold slope. In spite of the imperfect performance, the device is good enough for low voltage SRAM applications due to both the high on-current at low voltage and the very low off-current for standby mode. Better device performance is expected with further process optimization.

Fig. 5 shows the gate transfer characteristics of the FSABG PMOS transistor and conventional NSABG PMOS transistors whit 300 Å and 1000 Å silicon film thickness. The L in the figure stands for the gate length for the FSABG and the mask length for the NSABG as shown in the Fig. 1(e). Compared to the FSABG transistor, both NSABG devices show much higher off-current. This verifies the formation of the LDD in the FSABG device predicted by the simulation as shown in Fig. 2. Furthermore, the NSABG transistor with 300 Å channel has a much smaller on-state current even though it exhibits a similar sub-threshold characteristics. This apparently arises from the poor source/drain contact and high source/drain sheet resistance due to the thin parasitic source/drain region. On the other hand, the NSABG device with 1000 Å channel has a much higher threshold voltage (-1.3 V) and off-current (3 pA) as well as the significantly degraded sub-threshold swing (328 mV/dec). Two factors are responsible for the poor performance of the thick channel device. Firstly, the thicker body (or channel) leads to the higher V_T and gentler sub-threshold slope similar to the case in SOI devices. Secondly, the thicker film usually has the poorer electrical property when crystallized by MILC [9]. These experimental results indicate the importance of combining of a thin channel and a thick source/drain to achieve high performance bottom-gate devices. The proposed technology provides a simple mean to achieve all the desirable features for bottom gate devices.

Fig. 6 shows the gate transfer characteristics of the FSABG MOSFET with wide (5 μm) and narrow (0.5 μm) channels, respectively. It can be seen that the performance of the device with 5μm channel width is quite inferior to that of 0.5 μm channel length. The off-current is high up to 7.81×10^{-12} A/μm, and sub-threshold slop is also degraded to 184 mV/dec. The higher off-current and gentler sub-threshold behavior are believed to due mainly to the higher trap density at the interface between the channel and the gate oxide in the wide device. The earlier work pointed out that the interface trap density could be reduced by a post-oxidation step [6] just as done in this work. However, the reduction in trap density is only effective significantly to the devices with submicron channel width. In addition, the narrower devices probably contain fewer grain boundaries. As a result, the transistors with 0.5 μm channel width exhibits much better performance. Fortunately, only the narrow channel (W < 0.5 μm) load transistors are required in the SARM applications.



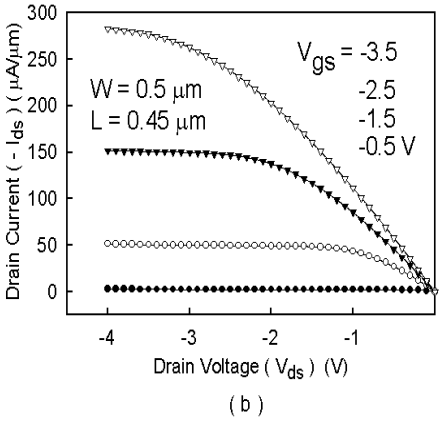


Fig. 4. (a) gate transfer characteristics and (b) output characteristics of SABG PMOSFET. Gate oxide thickness = 115 Å.

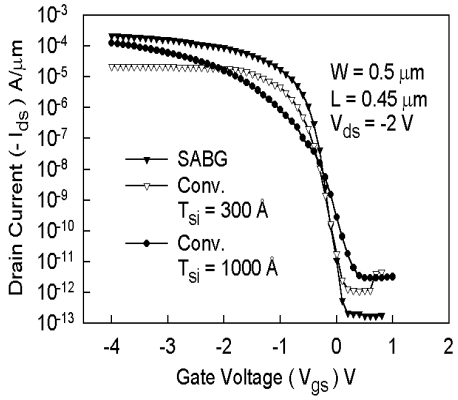


Fig. 5. Experimental gate transfer characteristics of the SABG and the conv. Non SABG MOSFETs with thick and thin channel thickness.

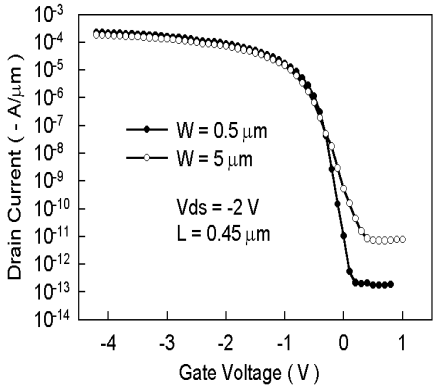


Fig. 6. Experimental gate transfers of SABG FETs with different channel width.

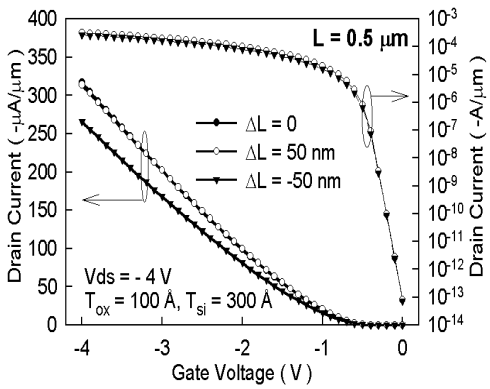


Fig. 7. Simulated current variation of Non SABG FET with L = 0.5 μm.

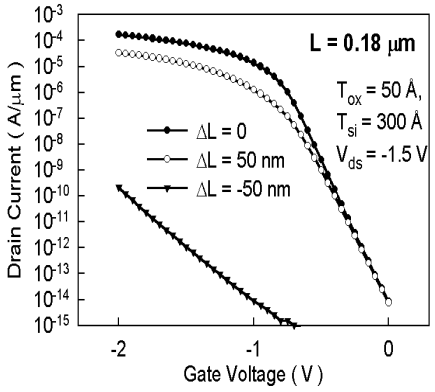


Fig. 8. Simulated current variation of Non SABG FET with L =0.18 μm.

The non-self-alignment effects are also studied using Medici device simulator. Fig.7 and Fig.8 show the simulated performance variations caused by the non-self-aligned process. It is seen the device cannot be turned on at al with ± 50 nm misalignment if device is scaled down to 0.18 μm generation.

4. Conclusions

A fully-self-aligned bottom-gate (FSABG) MOS transistor technology has been proposed and demonstrated for the first time. Conventional ion implantation and subsequent CMP have been employed to implement the fully-self-aligned device configuration. In spite of a fully-self-aligned process, it only requires 4 masks, the same as the conventional top gate technology. Deep submicron FSABG PMOSFETs with performance comparable to the bulk or SOI MOSFETs have been achieved. The proposed bottom-gate transistor is suitable for high density and low voltage SRAM as well as other 3D IC applications.

Acknowledgement

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References

[1] C. Y. Chang, and S. M. Sze, "ULSI Device", *JOHN WILEY &SONS, INC*. pp. 333-362, 2000.

[2] C. T. Liu, C. H. Yu, A. Kornblit, and K. H. Lee, "Inverted thin-film transistors with a simple self-aligned lightly doped drain structure," *IEEE Trans. Electron Devices*, vol. 39 pp. 2803-2809, 1992.

[3] Y. Takao, H. Shimada, N. Suzuki, Y. Matsukawa and N. Sasaki, "Low-power and high-Stability SRAM technology using a laser-recrystallized p-channel SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2147-2152, 1992.

[4] J. Jang, J. Y. Oh, and S. K. Kim, "Electric-field-enhanced crystallization of amorphous silicon," *Nature*, vol.395, no. 6701, pp. 481-483, 1998.

[5] A. Hara, Y. Mishima, T. Kakehi, F. Takeuchi, M. Takei, K. Yoshino, K. Suga, M. Chida, and N. Sasaki, "High Performance Poly-Si TFTs on a Glass by a Stable Scanning CW Laser Lateral Crystallization," in *IEDM Tech. Dig*., pp.747-751, 2001.

[6] M. Sasaki and T. Kimura, **"**The impact of oxidation of channel polysilicon on the trap-density of submicron bottom-gate TFT's**,"** *IEEE Electron Device Letters*, vol. 15, no. 1, pp.1-3, 1994.

[7] H. Wang, M. Chan, S. Jagar, V. M. C. Poon, M. Qin, Y. Wang, and P. K. Ko, "Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method," *IEEE Trans. on Electron Devices*, vol. 47, no.8, pp. 1580-1586, 2000.

[8] S. Jagar, H. Wang, and M. Chan, "Effects of longitudinal and latitudinal grain boundaries on the performance of large-grain polysilicon MOSFET," *IEEE Electron Device Letters*, vol. 22, no.5, pp. 218 –220, 2001.

[9] Z. Jin, H. S. Kwok, and Man Wong, " Performance of thin-film transistors with ultrathin Ni-MILC polycrystalline silicon channel layers," *IEEE Electron Device Letters*, vol. 20, no.4, pp.167–169, 1999.