High performance 0.1μm CMOS device with suppressed parasitic junction capacitance and junction leakage current

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Abstract

High performance 0.1μm MOSFETs with a 70nm physical gate length and 1.7nm gate oxide thickness are demonstrated. By reducing the parasitic junction capacitance and suppressing the junction leakage current (Ileak,j), high speed/low power transistors are fabricated with a superior driving current. Careful optimization in channel, pocket and source/drain (S/D) doping profile results in a reduction of N+/PW area junction capacitance (Cja) to 0.8fF/μm^2 and P+/NW Cja to 0.7fF/μm^2. In addition, area diode leakage current (Ileak,a) <50nA/cm2 and periphery diode leakage current (Ileak,p) <0.1fA/μm are achieved. In this work, NMOS drive current and PMOS drive current are 840μA/μm and 380μA/μm respectively, at 1.2V with an off-state current (Ioff) 15nA/μm. With the reduced parasitic capacitance and the high driving current, the unloaded ring oscillator has 10.5ps/stage at 1.2V operation.

1. Introduction

Requirements for high speed CMOS are a high drive current and a low parasitic capacitance while the low power CMOS need a low standby leakage current. To satisfy these requirements, we need to reduce the parasitic junction capacitance (Cj) and suppress Ileak,j as optimizing 0.1um high performance MOSFETs. However, the transistor degradation can be occurred due to the effort for reducing the parasitic Cj and Ileak,j such as the addition of another process or the aggressive scale-down. This work addresses particular issues with the parasitic parameters as considering the high performance MOSFETs. In this paper, the high performance devices are demonstrated with a careful tailoring of the channel doping profile, the pocket implantation and graded S/D implantation without any degradation of the transistor performance.

2. Experimental

Dual gate 0.1μm CMOS process flow is implemented with a precise control of the doping profile in the channel region, S/D extension (SDE) with abrupt pocket and deep S/D junction. Isolation is formed with shallow trench isolation 4kÅ. Although the use of indium will result in a steeper doping profile, boron is preferable as a main p-type dopant because of the low solid solubility limit of indium and the narrow width effects of a narrow channel device. The channel of NMOS was doped by using boron dose of 2-6x10^{12}/cm^2 with energies varying from 10 to 40keV and PMOS channel was doped by using arsenic dose of 2-6x10^{12}/cm^2 with energies varying from 100 to 200keV. The gate dielectric was grown by using NO gas and the gate poly electrode was formed subsequently. An offset spacer for reducing the gate to S/D overlap capacitance (Cgdo) was followed by a shallow SDE with the abrupt pocket implantation. After forming L-shaped spacer, N+S/D implantation was done with arsenic dose of 5x10^{15}/cm^2 at 40keV followed by phosphorus dose of 1-5x10^{13}/cm^2 at energies varying from 30 to 60keV. Similarly, boron P+S/D implantation was used with a dose of 3x10^{15}/cm^2 at 4keV and then boron was implanted with a dose of 1-5x10^{13}/cm^2 at energies varying from 10 to 15keV. After S/D activation of 1050°C spike rapid thermal annealing (RTA) with cover SiO_2, $CoSi_2$ was formed on S/D and gate electrode.

3. Results and discussion

The parasitic Cj and Ileak,j can be suppressed by the optimization of the channel, pocket, S/D and graded S/D doping profile. To find out the critical process factors for the Cj and Ileak,j suppression, simulation and implantation split experiment were done as well as process architecture analysis.

As shown in Fig.1, the simulation was done with the varying boron implantation energy in the n-channel region. It is observed that the lower boron energy profile meets N+S/D doping profile at the lower doping level. The junction with this lower level's doping gives a lower Cj and Ileak,j. N-channel boron energy of 10keV is feasible for the reduction of the area/periphery Cj and Ileak,j if the same threshold voltage is kept by adjusting the channel implantation dose. In addition, we need to optimize SDE and pocket implantation condition to minimize the channel adjustment effect needed.

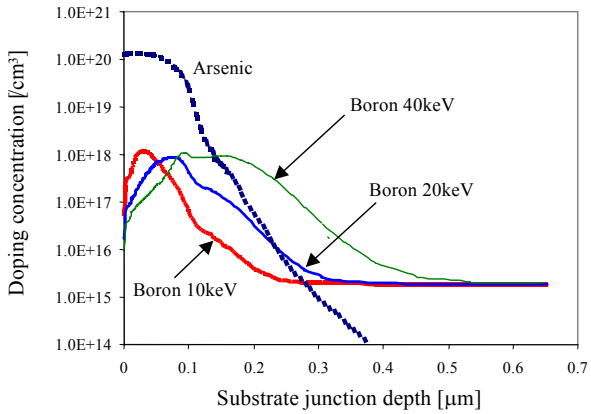


Figure 1. Simulation doping profile of boron n-channel region with varying implantation energy

Depending on the simulation results, we obtained the reduced parasitic Cj for both N+/PW and P+/NW diode structure. Fig. 2 shows the reduction of Cj as the channel implantation energy decreases. Channel energy condition of 10keV reduces N+/PW Cja by 70% compared to 40keV condition after junction side-wall capacitance (Cjsw) is decoupled separately. Fig. 3 shows the reduced P+/NW Cja as we optimized the doping profile with the lower channel implantation energy, the higher pocket tilt implantation and the additional P+S/D graded implantation. P+/NW Cja with optimum condition was decreased by 80% after Cjsw effect was decoupled separately.

Table 1. Parasitic junction capacitance

CMOS Logic	NMOS	PMOS
Cj [fF/μm^2]	0.8	0.7
Cjsw [fF/μm]	0.03	0.03
Cjswg [fF/μm]	0.4	0.3
Cgdo [fF/μm]	0.2	0.3

Low parasitic capacitances were obtained in this work as shown in Table 1. Cja and Cjsw for N+/PW and P+/NW is significantly reduced compared to relevant published data [1]. Furthermore, Cgdo and the side wall junction capacitance under gate electrode (Cjswg) are minimized to ensure high performance for 0.1um devices. For good control of Cjswg and Cgdo, SDE dose and pocket implantation was carefully executed. As SDE condition has a trade-off relation between Cgdo and transistor driving current, SDE junction profile has to be kept abrupt to meet both parameters. Besides, pocket condition should not only affect Cja but also improve the transistor performance.

In the same way as the parasitic capacitance reduction, N+/PW and P+/NW junction leakage current were also suppressed using the optimized process condition presented for Cj reduction. N+/PW Ileak,j was suppressed by the optimization of n-channel doping, N+S/D and S/D graded implantation as shown in Fig. 4.

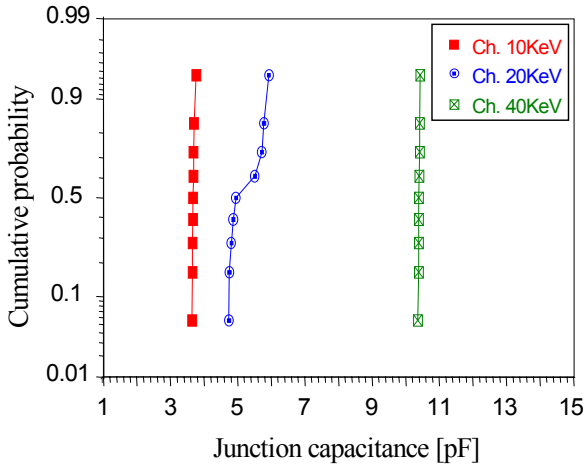


Figure 2. Cumulative probability of N+/PW area junction capacitance with varying energy of boron n-channel implantation

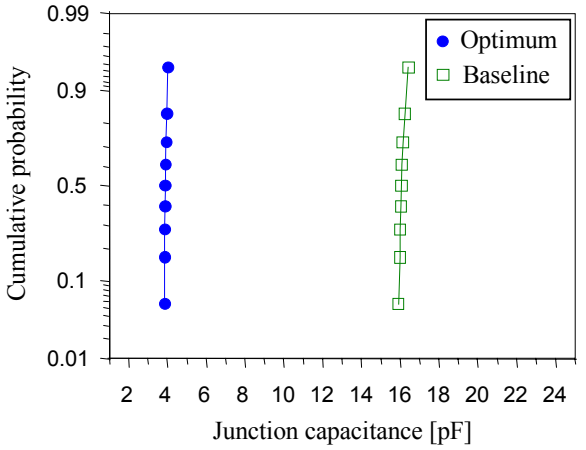


Figure 3. Cumulative probability of P+/NW area junction capacitance for optimum vs. baseline process condition

As decreasing channel implantation energy, Ileak,j is gradually reduced for both area type (area=6600μm^2, perimeter=460μm) and periphery type (area=12000μm^2, perimeter=64800μm) structure. Periphery type diode normally shows a larger Ileak,j than the area type diode due to the high perimeter leakage current along the shallow trench edge. Fig. 5 shows the significant P+/NW area and periphery junction leakage reduction with the optimized channel, pocket and S/D doping profile while baseline condition has a large variation in spite of the same process condition. To get optimum condition, S/D graded implantation with boron is added after P+S/D implantation. It can accelerate the short channel effect for higher implantation energy and PMOS pocket implantation has to be optimized to remove the effect of S/D graded implantation.

The optimized S/D graded implantation condition has a more significant impact on P+/NW leakage reduction than N+/PW diode because P+/NW junction has a larger spread of Ileak,j than N+/PW.

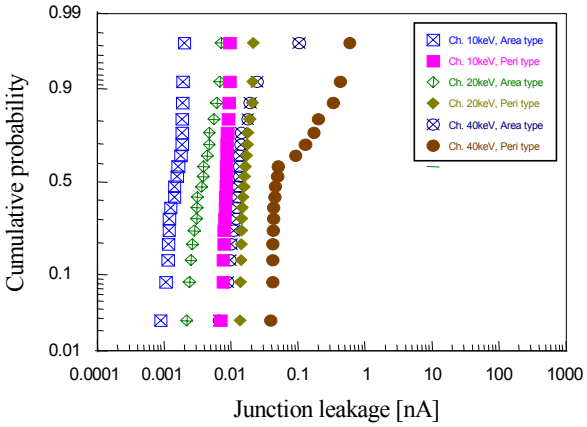


Figure 4. Cumulative probability of N+/PW area and periphery type junction leakage current according to different n-channel implantation

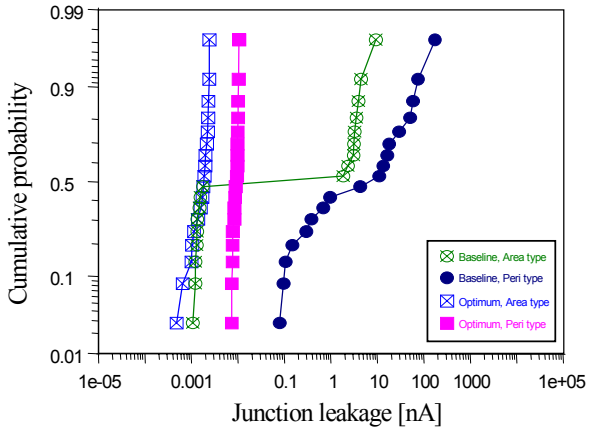
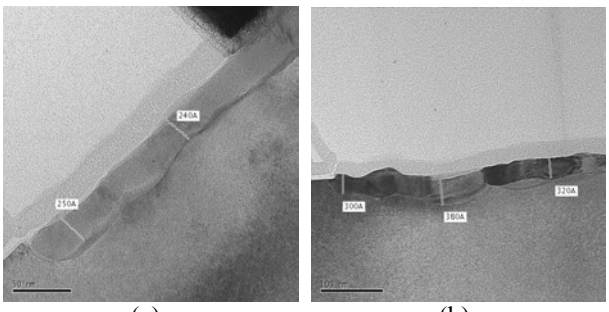


Figure 5. Cumulative probability of P+/NW area and periphery type junction leakage current for baseline vs. optimum process condition

As shown in Fig. 6, cobalt salicide thickness between N+/PW and P+/NW substrate is different due to the different species for S/D implantation which alter the silicide spike growth inside the deep S/D area [2]. Arsenic ion implantation makes a amorphous layer and suppress the abnormal salicide growth such as spikes while boron ion implantation without a amorphous layer partially causes the quick spike growth.



(a) (b)

Figure 6. TEM analysis for N+/PW(a) and P+/NW(b) cobalt salicide thickness after 2nd RTA 850°C formation

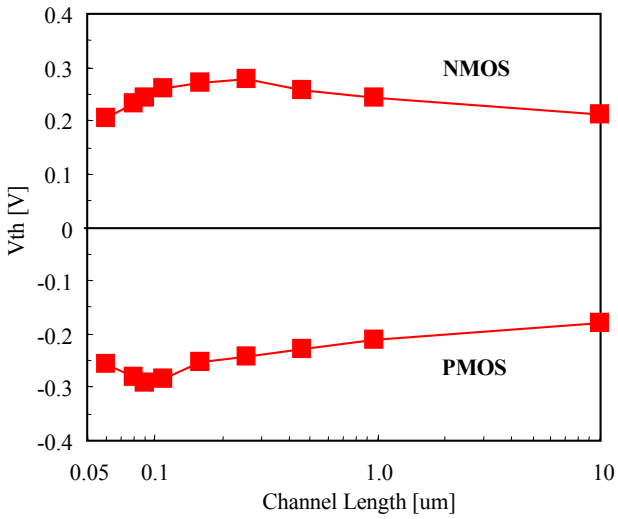


Figure 7. Threshold voltage as a function of the gate length for NMOS and PMOS

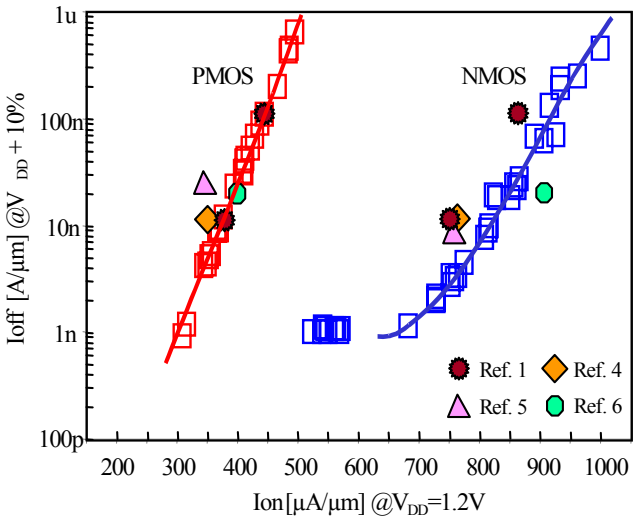


Figure 8. Off-state current vs. drive current for NMOS and PMOS device at Vdd=1.2V

Careful doping profile tailoring in channel, pocket and S/D region result in a reduction of N+/PW Cja to 0.8fF/μm^2 and P+/NW Cja to 0.7fF/μm^2. In addition, Ileak,j is also suppressed with Ileak,a <50nA/cm^2 and Ileak,p <0.1fA/μm [3].

With physical 70nm gate length and 1.7nm equivalent oxide thickness, NMOS drain saturation current (Idsat) and PMOS Idsat are 840μA/μm and 380μA/μm respectively, operating at 1.2V with an Ioff 15nA/μm. Fig. 7 and Fig. 8 show the well controlled short channel effect down to 60nm and the competitive device performance of Ioff versus the drive current (Ion) for both NMOS and PMOS device [1][4][5][6]. The high performance device was achieved by abrupt pocket profile, shallow SDE junction [7] and spike rapid thermal annealing. Optimized SDE structure not only reduced the parasitic series resistance to improve the

driving current but also Cgdo to decrease the parasitic loading capacitance [8].

The unloaded ring oscillator achieved 10.5ps/stage delay with the realized low parasitic capacitance and the high performance devices at 1.2V operation. Fig. 9 shows the propagation delay versus the normalized Idsat with respect to with or without S/D graded implantation condition. S/D graded implantation condition which gives lower Cj is about 8% faster than without S/D graded implantation condition.

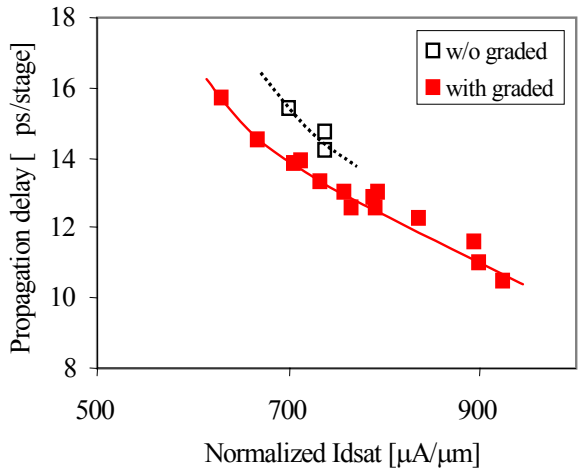


Figure 9. Propagation delay vs. normalized Idsat for with S/D graded or without S/D graded implantation

4. Conclusion

To realize the high performance devices beyond 0.1um technology regime, the consideration of a parasitic junction capacitance and a junction leakage current is as essential as a transistor driving current. In this work, the reduction of the parasitic junction capacitance and the junction leakage current was achieved by the optimization of doping profile through the careful tailoring of the implantation condition without any change of the transistor performance. With the high performance device, we demonstrated the unloading inverter delay of 10.5ps/stage for 0.1μm manufacturable process technology.

References

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