# Reliability and Retention Study of Nanocrystal Cell Arrays

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## Abstract

*We have studied nanocrystal memory arrays with 2.56 × $10^5$ cells (256kb) in which Si nanocrystals have been obtained by CVD deposition on a 4nm tunnel oxide. The cells in the array are programmed and erased by electron tunneling through the $SiO_2$ dielectric. We find that the threshold voltage distribution has little spread. In addition the arrays are also very robust with respect to drain stress and show good retention.*

## 1. Introduction

Nanocrystal memory cells are very attracting for application in low power and ultra-scaled devices [1,2]. With respect to new generation memories obtained with emerging technologies, nanocrystal memories have the advantage of being full compatible with standard CMOS technology.

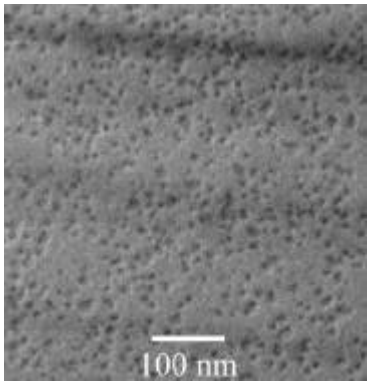


**Figure 1**. TEM plan view showing the nanocrystal distribution and size on the silicon dioxide.

In this work e have realized nanocrystal memory cells by depositing silicon islands on thin $SiO_2$ tunnel dielectric. The study has been focused on the electrical characterization of arrays consisting of 2.56 × $10^5$ memory cells (256kb) in which the all the cells can be programmed or erased at the same time by electron tunneling from the cell channels through the $SiO_2$ dielectric.

Si islands were obtained by CVD deposition of silicon on top of a thin silicon dioxide, thermally grown on a (100) silicon wafer. The deposition was carried out using $SiH_4$ and $H_2$, the temperature was in the range 500-600°C and the pressure was of 80 Torr. The memory cells were fabricated by using the technology process flow of state of the art Flash-EEPROMs that consists of scaled CMOS with shallow trench isolation. The continuous floating gate was replaced by the array of nano-crystalline silicon islands.

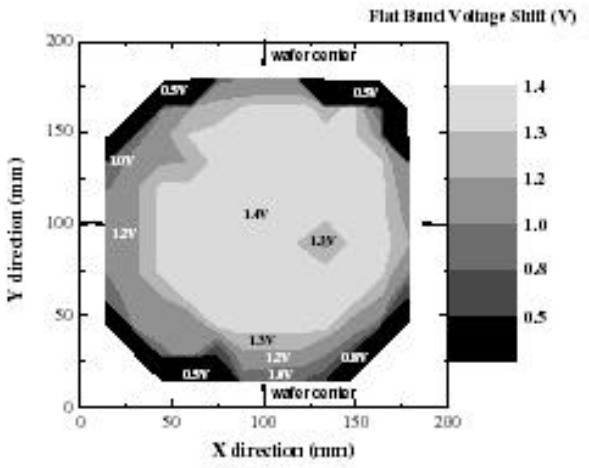


**Figure 2**. Flat band voltage shift distribution on an 8 inches silicon wafer. The shift is obtained by programming and erasing large area capacitors, which are uniformly distributed on the wafer.

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The memory tunnel dielectric was a thin silicon dioxide of 4 nm. The floating Si islands were coated with a control oxide formed by a CVD $SiO_2$ layer having a thickness of 8nm.

The elementary cell was characterized by having a channel length of 0.34 μm and a channel width of 0.2 μm.

## 2. Results

Fig. 1 is a typical example of the Si nanocrystal distribution on the oxidized surfaces as obtained by TEM plan view imaging. In Fig. 1 the size distribution is peaked at a radius of ~ 3 nm and the nanocrystal density is of ~ $3 \times 10^{11}$ $cm^{-2}$.

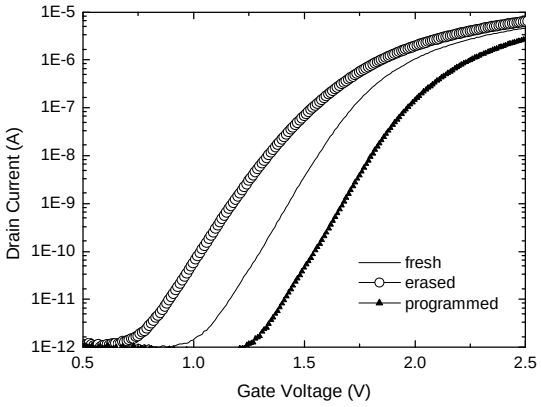


**Figure 3.** Programmed and erased Id-Vg characteristics of the single nanocrystal cell. The programming is obtained by applying +10 V for 1 ms to the control gate with the other terminals to ground. The erasing is achieved by applying – 10V for 1 ms to the gate with the other terminals to ground.

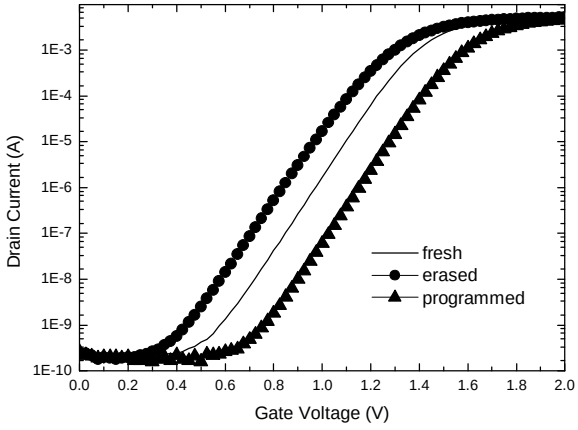


**Figure 4:** Fresh, erased and programmed Id-Vg characteristics for the 256kb cell array.

The uniformity of the nanocrystal distribution on the 8 inches wafer has been measured by monitoring the flat band voltage or threshold voltage shift between written and erased states in MOS capacitors and in MOSFETs. Fig. 2 shows an example of the distribution on the wafer of flat band voltage shift between written and erased state. Programming and erasing were obtained by applying +10 V and -10V, for 1 s to the MOS gate, respectively. One can observe that the shift is quite uniform on the large area wafer and this indicates a good uniformity of the gate stack in terms of thickness of the dielectrics and of the nanocrystal size and density. Typical Id-Vg characteristics for fresh, programmed and erased single cell are shown in Fig.3. The cell reading is obtained by applying 100 mV to the drain whereas source and substrate are grounded. Both programming and erasing are achieved by applying pulses of + 10 V or – 10 V, with a duration of 1 ms, to the control gate. The threshold voltage shift between written and erased levels, measured at a drain current of 1 nA, is of ~ 0.5 V. The subthreshold slope in the Id-Vg characteristics of the fresh cell is of 125 mV/dec. Typical drive current at Vd=100 mV is of 10 nA.

Programming and erasing are achieved by tunneling through the 4 nm oxide, even though channel hot electron programming is a possible option.

Fig. 4 shows the Id-Vg characteristics in the fresh, programmed and erased states of the 256kb array, programming and erasing conditions are the same used for the single cell (Fig.3). Fig.4 shows that no significant threshold voltage spread is observed, neither in the fresh nor in the written and in the erased state. The sub-threshold slope, in fact, remains practically unchanged and it is the same of that of the single cell of Fig.3.

Figures 5 (a), (b) and (c), show the Id-Vg characteristics of the 256kb cell array in the programmed state after 1, $10^3$ and $10^5$ write/erase (W/E) cycles. It can be observed that after cycling the subthreshold slope of the programmed Id-Vg characteristic remains unchanged. Note that after $10^5$ cycles the characteristic is shifted towards higher voltage values of about 0.05 V, this is due to charge trapping in the oxide that causes a rigid shift towards higher values but it does not induce a closure of the W/E window.

Furthermore we have applied a drain stress to the array by programming the cells and measuring the variations in the Id-Vg curve as a consequence of the application of 5 V to the drain for a time up to 10 s, the other terminals were grounded. Usually Flash memory cells are subjected to drain stress when a cell is in the programmed state and the bit line is biased to high voltage of ~ 4.5 V to allow programming of other cells [3]. This type of stressing test is critical for standard Flash cell arrays and it is used to monitor the presence

of tails in the threshold voltages distributions. Typically tails can be observed after long stress times ( >100 ms). Fig.6 shows that the characteristic in the programmed state is not influenced by the drain stress, as it remains overlapped to that obtained without the stress. Some distortions begin to be observed when the drain voltage is increased to 10V, as it is depicted in Fig.7.

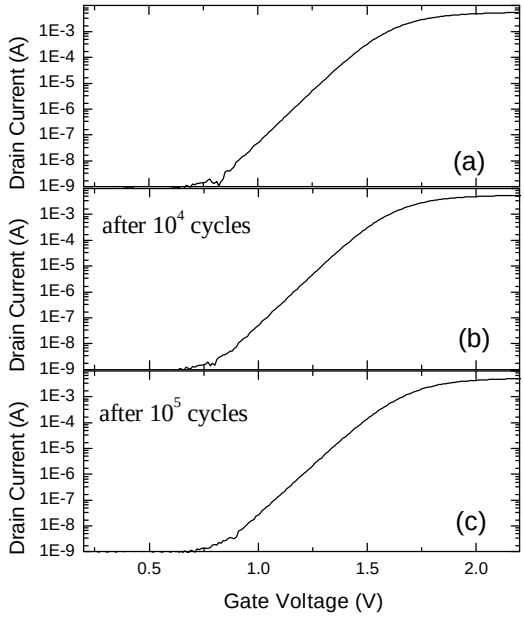


**Figure 5:** Id-Vg characteristics of the cell array in the programmed state:(a) after 1 cycle of W/E; (b) after $10^4$ cycles of W/E and (c) after $10^5$ cycles.

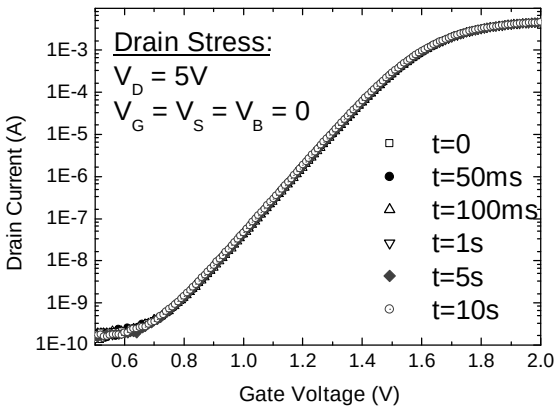


**Figure 6:** Id-Vg characteristics of the cell array in the programmed state after drain stress obtained applying 5V to the drain for different times, up to 10 s.

The retention characteristic of the cell arrays has been then investigated for long times and at high temperature.

Fig.8 shows the time evolution at a temperature of 250°C of the programmed and erased threshold voltages, respectively, measured at 1 μA. The monitoring has been carried out for more than 300 hours. Programmed and erased logic states remain well separated, with a difference higher than 0.45 V for all the duration of the measurement.

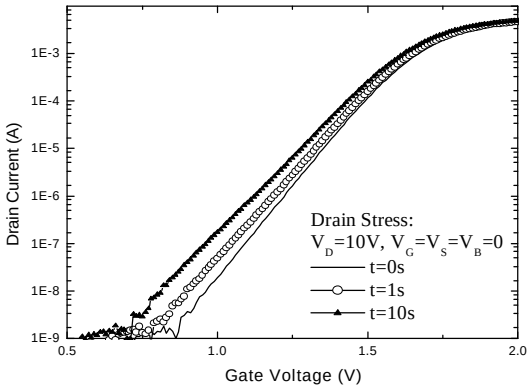


**Figure 7.** Drain stress obtained by applying 10 V to the drain of the cell array, with the other terminals to ground.

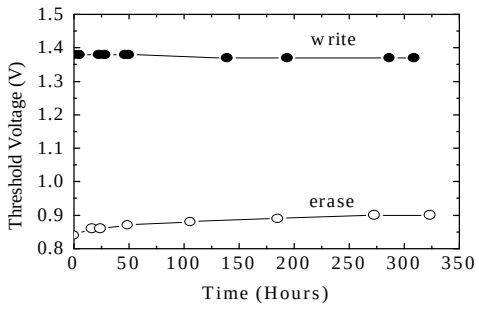


**Figure 8**. Written and erased threshold voltage measured at 1 μA as a function of the time at 250 °C.

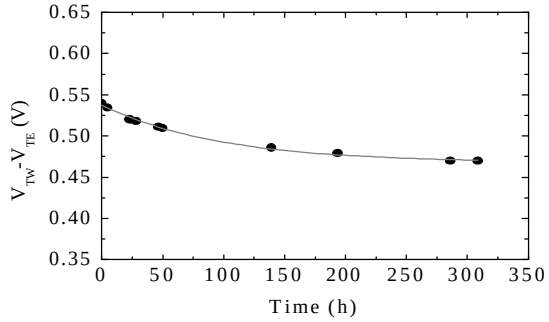


**Figure 9.** Behaviour of the threshold voltage shift between written and erased state ($V_{TW}$-$V_{TE}$) measured at 250°C as a function of the time.

Fig.9 displays the window ($V_{TW}$-$V_{TE}$) closure as a function of time, it can be observed that the shift follows an exponential decay down to a constant value. The Initial window is 0.54 V than it reduces of 5% after 50 h, 9% after 100 h, 11% after 200 h and 13% after 300 h.

## 4. Conclusion

We have realized arrays of $2.56 \times 10^5$ nanocrystal memory cells by depositing Si islands with radius of few nm on top of 4 nm tunnel oxide. The cells in the array are programmed and erased by electron tunneling through the $SiO_2$ dielectric. The distribution of cell threshold voltages has little spread both in the programmed and erased states and is poorly influenced by high cycling. The arrays are also very robust with respect to drain stress and show good retention characteristics.

## 5. References

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[2] H.Hanafi et al., IEEE Trans. Electron Devices **43**, 1553 (1996).
[3]P.Pavan et al., Proceedings of the IEEE **85**, 1248 (1997).