Off-Leakage and Drive Current Characteristics of Sub-100-nm SOI MOSFETs and Impact of Quantum Tunnel Current

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Abstract

This paper estimates the off-leakage current (I_{off}) and drive current (I_{on}) of various silicon-on-insulator (SOI) MOSFETs by simulations based on the hydrodynamic-transport model. It is shown that the double-gate SOI MOSFET doesn't always offer better drivability than other SOI MOSFETs, and that a single-gate SOI MOSFET with carefully selected parameters exhibits superior performance to double-gate SOI MOSFETs.

It is also demonstrated that the quantum tunnel current is not significant, even in 20-nm-channel SOI MOSFETs.

1. Introduction

The double-gate (DG) SOI MOSFET has been receiving attention as a device for the nano-scale regime [1] because the DG SOI MOSFET continues to be considered as the ultimate device structure for suppressing the short-channel effects (SCEs) with drivability superior to those of other devices. In particular, performances of symmetric double-gate (SDG) SOI devices [2] having poly-Si gates with the same conduction type, and asymmetric double-gate (ADG) SOI devices [3] having n^+ and p^+ poly-Si gates have been widely discussed [4,5].

In the sub-100-nm channel regime, the simulations must take account of many physical phenomena, such as hydrodynamic transport, band-to-band tunneling (BBT) at the drain [6] and quantum tunneling between source and drain. Recently, we discussed the influence of BBT on off-leakage current in [7], where it is clearly shown that the BBT enhances the off-leakage current. However, it's still controversial whether a small DG SOI device can really achieve the desired characteristics.

In this paper, we estimate the off-leakage current (I_{off}) and drive current (I_{on}) of single-gate (SG), SDG, and ADG SOI devices by simulations that use the hydrodynamic-transport model. First, the drive currents of various SOI devices are simulated and intrinsic performances are compared. Second, the influence of technological advances on device performance is discussed. Finally, the quantum tunnel (QT) between source and drain is numerically simulated using an original model, and its impact on I_{off} is evaluated for various SOI devices.

2. Device structures simulated

The parameters are selected on the basis of the conventional scaling method and the technology road map; in other words, basically we employed the technology level of 100-nm channel devices independent of channel length (L). The gate oxide thickness and the silicon layer thickness of the simulated SOI nMOSFET devices were 3 nm and 5 nm, respectively. The silicon layer thickness was chosen to avoid quantum mechanical influences perpendicular to the gate oxide/silicon layer interface because it is anticipated that a sub-5-nm thick silicon layer would manifest many quantum mechanical effects to the detriment of the transport characteristics [8]. The buried oxide thickness of SG device was 10 nm, and that of SDG and ADG SOI devices was 50 nm. Except for DG SOI devices, the buried oxide layer thickness was designed to suppress SCEs by increasing the SOI-to-substrate electric field [9]. Doping levels of p-type SOI layer and p-type substrate were $3x10^{17}$ cm^{-3} and $3x10^{17}$ cm^{-3}, respectively. The gate overlap length (L_{ov}) was assumed to be 20 nm; this represents a current technology limit. Drain voltage (V_d) was 1V. Here, we used a commercial two-dimensional (2-D) device simulator [10], and the hydrodynamic transport model was implemented. We chose the mobility model proposed by Caughey-Thomas [10]. Quantum tunneling (QT) current was evaluated using original simulations; the tunneling probability was calculated by the transfer-matrix method. 2-D potential barrier profile between the source and the drain was calculated by a device simulator [10]. QT current was not considered in deriving the results in Figs. 1-4.

3. Results and discussion

3.1. Drive current and intrinsic performance of various SOI devices

In order to compare the drivability of various SOI devices, the dependence of intrinsic performance (C_gV_g / I_{on}) on I_{off} is shown in Fig. 1, where C_g is the total gate capacitance and V_g is the gate voltage. Simulation results for L of 100, 50, 40, 30 and 20 nm are plotted for each device. The ADG SOI device shows the largest I_{off} and the worst drivability. It should be noted that the SDG SOI device doesn't always show better drivability than the SG device.

In these simulations, all the devices have a very thin gate oxide layer. The gate-induced electric field at $V_g = V_{th}$ + 1V is about $3x10^6$ V/cm at the gate oxide/SOI layer interface; surface roughness scattering is dominant in this range of electric field. The SOI layer is at most several times as thick as the inversion layer. Surface roughness scattering influences the transport of most electrons in the DG SOI MOSFET because the inversion layer covers almost the whole SOI layer.

Since the electric field along the channel exceeds $1x10^6$ V/cm in sub-100-nm channel devices, the electron drift velocity should exceed its saturation velocity. However, the DG devices have lower longitudinal electric fields in the channel at $V_g = V_{th}$ + 1V (not shown here), which results in less acceleration of electrons. Consequently, the DG devices have comparable or slightly less drivability.

Next we discuss radio-frequency performance. Cut-off frequency, f_t, dependence on L is shown for various devices in Fig. 2. It should be noted that SG SOI devices show the best performance even when the SG SOI device has the thinnest buried oxide layer. Two-different DG SOI devices show an f_t value that is half that of the SG SOI device. The degradation of f_t values in DG SOI devices originates from the bottom gate electrode, which has extra parasitic capacitance around the electrode.

The above-described simulation results demonstrate that current drivability and analog performance depend strongly on device structure, and that SG SOI devices show better performance than DG SOI devices.

3.2. Influence of technological advance on off-leakage and drive current

In the foregoing section, we fixed the device parameters except for L. However, in 20-nm-channel SOI devices, the present value of gate overlap, L_{ov}, (20 nm) is not compatible with enhanced device performance. Accordingly, we considered the influence of technological advances on I_{off} and I_{on}. Since it can be easily anticipated that L_{ov} rules the drivability of devices with sub-100-nm channel lengths, we considered the scaling effect of L_{ov} on I_{on} and I_{off}. We assumed that L_{ov} was scaled down in proportion to L; the initial value of L_{ov} is 20 nm for L=100 nm and 4 nm for L=20 nm.

In order to compare the drivability of various SOI devices, the dependence of C_gV_g / I_{on} on I_{off} is shown in Fig. 3. Simulation results for L of 100, 50, 40, 30 and 20 nm are plotted for each device. C_gV_g/I_{on} decreases as L is reduced. C_gV_g/I_{on} value of the 20-nm channel SG SOI MOSFET in Fig. 3 is smaller than that in Fig. 1. This is because the parasitic resistance of the overlap region is reduced as L_{ov} decreases, and because the deceleration of electron velocity is suppressed as L_{ov} decreases. On the other hand, I_{off} increases as L is reduced. I_{off} value of the 20-nm channel SG SOI MOSFET in Fig. 3 is much larger than that in Fig. 1. This is because the local longitudinal electric field of the gate-drain overlap region increases; this results in the increase in BBT current. For ADG SOI devices, some simulation results (L=30 nm and 20 nm) are not plotted because those devices exhibit normally-on operation; the normally-on operation results from the BBT current. In addition, the reduction of L_{ov} leads to an enhancement of the SCEs. It should be noted again that the SDG SOI device does not always show the best performance even in Fig. 3.

The above results suggest that the abrupt lateral distribution of source and drain diffusions seen suppresses the degradation in I_{on}, while it yields the increase in I_{off} through the increase in BBT current. In addition, SCEs become prominent. Reducing the supply voltage is just one way to suppress I_{off} and SCEs. According to present simulations, we have to set $V_d < 0.5$ V in the 20-nm-channel SDG SOI MOSFET so that the BBT current at $V_g = V_{th}$-0.3V becomes negligibly small. However, this condition does not match the SDG SOI device design that yields acceptable performance. We have to set $V_d \sim 0.1$ V in the 20-nm-channel ADG SOI MOSFET.

Finally, simulated radio-frequency performance of the devices is shown in Fig. 4. Values of f_t are quite improved compared to those shown in Fig. 2 because L_{ov} has been scaled down and the deceleration of the longitudinal field near the source is suppressed. Past papers demonstrated (by simulations) that DG SOI devices show the highest digital switching speed [11]. In the present simulation, however, they don't achieve such outstanding analog performance. This is because the DG SOI devices have extra large parasitic capacitance around the bottom gate.

3.3. Influence of quantum tunnel current between source and drain

Kawaura *et al*. investigated the impact of the quantum tunnel current (QTC) component between source and drain in estimating I_{off} of a bulk MOSFET having an 8-nm channel [12]. They mentioned that the QTC component did not affect overall I_{off} characteristics at room temperature. In order to examine the impact of the QTC between source and drain in SOI MOSFETs, we numerically simulated the QTC component by the transfer-matrix method. Simulations were performed with the potential distribution obtained by a 2-D device simulator [10].

The ratios of quantum-mechanically simulated current

to classically-simulated current for SG, SDG, and ADG SOI devices at $V_g=V_{th}$ or $V_g=V_{th}$-0.5V are shown in Figs. 5(a), 5(b), and 5(c), respectively. Some simulation results include numerical errors of about 5 % because of differences in the mesh assignments. It can be seen in Fig. 5 that the QTC component alters the I_{off} characteristics to some extent for all device structures with sub-50-nm long channels. In SG SOI devices, a 10 or 15 % increment in I_{off} is anticipated in 5-nm-channel devices. The increment in the I_{off} of ADG SOI devices is identical to that in SG SOI devices. However, the increment in the I_{off} of SDG SOI devices is larger than that in SG SOI devices. The impact of the simulated QTC, however, is weaker, even in SDG SOI devices, than expected. Therefore, we can still employ the conventional semi-classical method to estimate the off-leakage current for sub-50-nm channel low-power SOI MOSFET applications.

4. Conclusion

In this paper, we estimated the off-leakage current and drive current of various SOI MOSFETs by simulations based on the hydrodynamic-transport model with the BBT effect. It has also been shown that the double-gate SOI device doesn't always show better drivability than other SOI devices, and that a single-gate SOI device offers better performance than double-gate SOI devices. Therefore, it can be suggested that the single-gate SOI device is more suitable for low-power SOI device applications than previously proposed double-gate SOI devices. It has been also demonstrated numerically that the quantum tunnel current is not significant, even in 20-nm-channel SOI MOSFETs. Therefore, we can still employ the conventional semi-classical method to estimate the off-leakage current of sub-50-nm channel low-power SOI MOSFETs.

Acknowledgement

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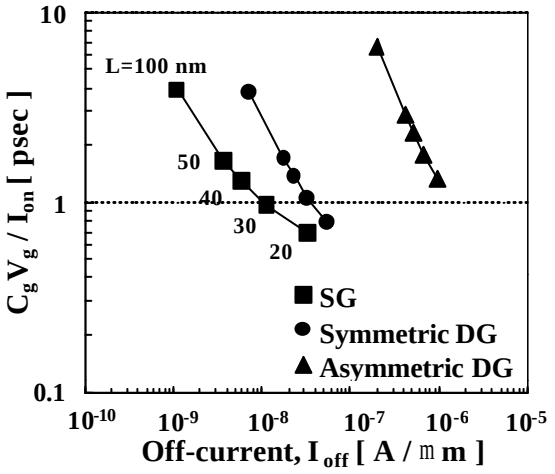


Figure 1. C_gV_g/I_{on} performances of SG, symmetric DG and asymmetric DG SOI MOSFETs. V_d = 1.0 V.

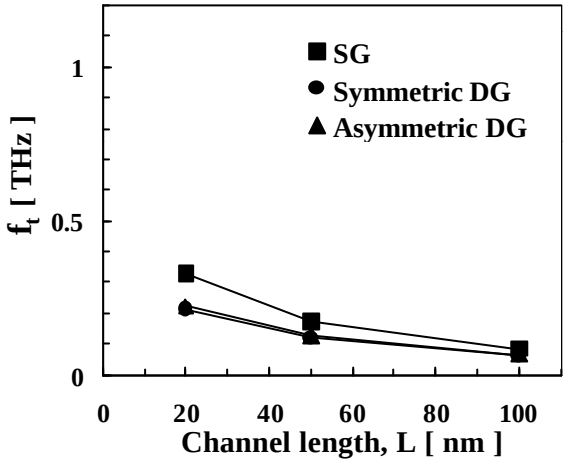


Figure 2. f_t versus channel length for various devices. All devices have the identical value of L_{ov} (20 nm). V_d = 1.0 V.

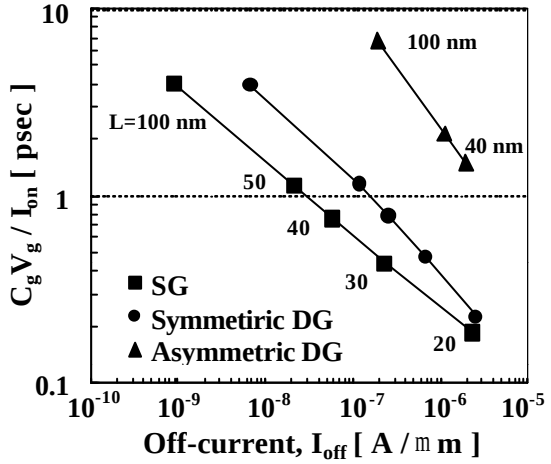


Figure 3. C_gV_g/I_{on} performances of SG, symmetric DG and asymmetric DG SOI MOSFETs. V_d = 1.0 V. Here, L_{ov} is linearly scaled down as L is reduced.

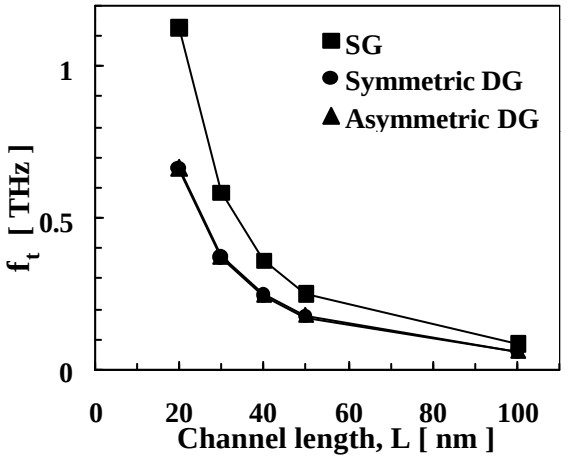
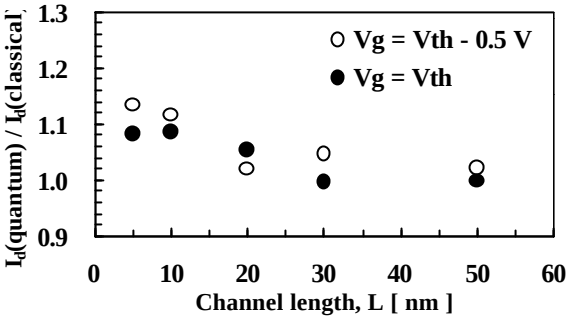
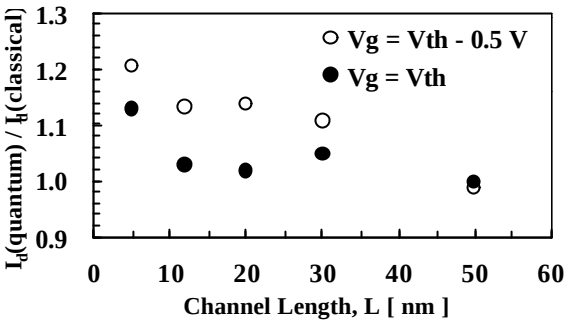


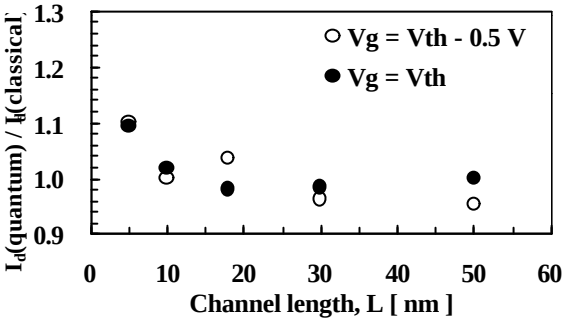
Figure 4. f_t versus channel length for various devices. Here, L_{ov} is linearly scaled down as L is reduced. V_d = 1.0 V.



(a) SG SOI device.



(b) Symmetric DG SOI device.



(c) Asymmetric double gate

Figure 5. The ratios of quantum-mechanically simulated current to semi-classically simulated current. V_d = 1.0 V. I_d is calculated at $V_g=V_{th}$ or $V_g=V_{th}$-0.3V.