50nm Schottky Barrier CMOS with Conventional Silicide

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Abstract

A novel structure of Schottky Barrier MOSFET is demonstrated. The devices are designed upon the concept utilizing quantum mechanical tunnelling through the Schottky barrier. An effective and state of art CMOS compatible process flow is used. 50nm N-type and P-type Schottky Barrier MOSFET with two conventional metal silicide are presented and excellent device performance is achieved in comparison with other Schottky Barrier devices.

1. Introduction

As MOSFET scales down to sub-100nm regime, source/drain engineering becomes crucial in device design. Performance degradation is a major trade-off for traditional approaches, such as shallow source/drain extension junction and 60mv/decase sub-threshold swing has been serving as a thermodynamic barrier for MOS devices that the transport is governed by drift and diffusion. Studies have shown source/drain parasitic resistance[1] would become more substantial as the devices continue scaling down. To conquer those physical challenges, device incorporating transport other than drift and diffusion and novel structures of source/drain must be explored. Schottky Barrier MOSFET has been an active candidate to solve source/drain resistance problem. Previous studies of Schottky Barrier devices [2,3,4,5,6] are primarily focused on the reduction of specific contact resistance using low barrier-height metal silicide, such as Platinum and Erbium. Also, the device is fabricated on an intrinsic substrate without using any source/drain or S/D extensions. However, such design proposes high degrees of complexity and challenges for fabrication and integration with current CMOS. Meanwhile, the SBMOSFET suffers from the deterioration of sub-threshold characteristic due to the substantial off leakge current. In this paper, a novel Schottky Barrier MOSFETs structure using conventional silicide and lightly doped source/drain extensions are presented. In this novel structure, the source/drain resistance is simply replaced by a gate bias modulated barrier. Quantum mechanical tunnelling is then incorporated with the device operation. By using conventional silicide, both N and P FET can be fabricated simultaneously without dealing with highly unbalanced barrier height. By adding the lightly doped source/drain extension, thin and controllable barrier width can be achieved. It will enhance the driving current of SB MOSFET and provide strong immunity of Short-channel Effect. It is noticeable that such lightly doped source/drain extensions also serve as the isolation of metal-semiconductor Schottky junction and therefore eliminate the anomalous junction leakage current.

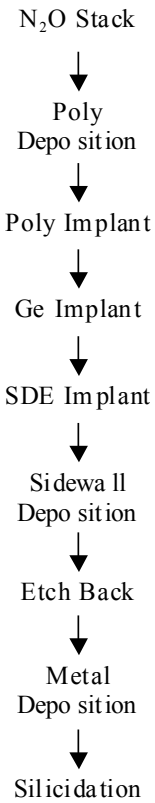

Figure 1. Process Flow

2. Device Fabrication

Upon standard CMOS process flow, several minor adjustments are applied A process flow with essential process steps is described in Fig-1. For conventional MOSFET, source/drain regions are often composed of both lightly doped SDE, deep source/drain regions that are the major contributors of SCE and metal silicide. Additional pocket implant is generally used to control SCE. However, for this SB MOSFET, Ge Pre-amorphous implantation and lightly doped extension are the only implantation process steps involved in the source/drain region. 20KeV Ge PAI serves the purpose of controlling both the SDE and silicide depth. The implantation steps are done sequentially and are followed by ultra-thin oxide deposition and etch back. The source/drain for NMOS and PMOS are implanted with As and BF_2 with energy 10KeV and 5KeV respectively. Since the Schottky barrier width is mainly modulated by the fringe electrical field from gate electrode, it is essential to minimize the distance from interface of Schottky junction to the gate electrode to achieve strong modulation. Thicknesses of thin sidewall oxide used in this work are 5 and 10nm as deposited. After etching back, the actual sidewall is thinner than 50% of the thickness as deposited to enhance the barrier modulation from gate bias (See in SEM figures in Fig-8 and Fig-9). Nevertheless, it also results in the critical challenge of the silicide formation to prevent the bridging from source/drain to gate. Metal silicide is chosen from the ones with metal-semiconductor barrier height close to mid-Silicon energy bandgap. Therefore, silicidation process can be done concurrently for both NMOS and PMOS. Co and Ni are selected and deposited. Two-time RTA are to complete silicide and form the SB source/drain structures. The final silicide thickness are about 100Å for $CoSi_2$ and 170Å for NiSi. The barrier heights of $CoSi_2$ and NiSi are 0.64eV[7] and 0.65eV[8] respectively. A schematic of Schottky source/drain structure is illustrated in Fig-2.

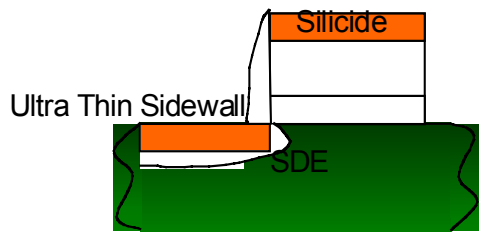

Figure 2. Schematics of source/drain structure of SB MOSFET

3. Result and Discussion

I-V characteristic of 50nm SB NMOS with NiSi source/drain is depicted in Fig-3. Driving current is greatly enhanced by the increment of SDE doping. It is not only due to the resistance reduction but also the thinner Schottky barrier width. It suggests that for this novel structure, the Schottky barrier width certainly play a important role determining the current flowing through the barrier. Therefore, it is clear that even though the barrier height determines the specific contact resistance, with proper control of the barrier width, it is achievable to increase the tunnelling current as well as the overall performance improvement of the MOS devices. There is an abnormal characteristic observed in both long channel and short channel devices shown in Fig-6 and Fig-7. As the reverse gate bias is applied, characteristic similar to as the device is bias at normal working condition is shown. Such phenomenon is also reported in TFT devices [9]. The possible reason for ambipolar characteristic for SB devices is that the majority carriers are accumulated at the channel as the gate bias reversed. While enough energy is supplied from drain bias, the carriers become capable to surmount the barrier or directly tunnel through the Schottky barrier at source. Therefore, if the source/drain are made of the metal-semiconductor system with mid-gap (~0.56eV) barrier height, such abnormal characteristic is anticipated. However, it is understandable that ambipolar characteristic can be substantially suppressed if the substrate is fully depleted. Nevertheless, in addition to the ambipolar phenomenon, excellent electrical performance for both long and short channel SB PMOS with $CoSi_2$ are illustrated in Fig-4~Fig-6. Good I_{on}/I_{off} ratio and substantial DIBL suppression are achieved in the first experiment of his novel SB MOSFET. With further adjustment of the threshold voltage, the off leakage current can be minimized and therefore the I_{on}/I_{off} ratio will be improved. Meanwhile, instead of penetrating deeply into channel, electrical field flux from source/drain extensions are favourably terminated by metal silicide junction and therefore, short-channel effect is therefore improved with the SB structure with addition of lightly doped SDE. Fig-8 and Fig-9 show both NMOS and PMOS with final gate length around 47nm and 55nm respectively measured in cross section SEM.

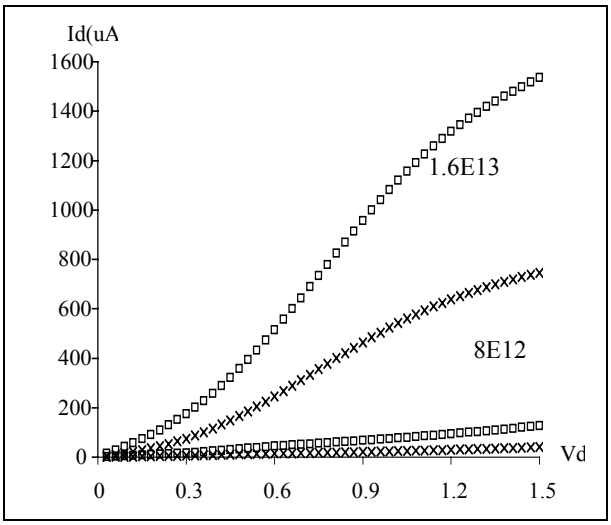

Figure 3. 50nm NiSi NMOS with different SDE doping

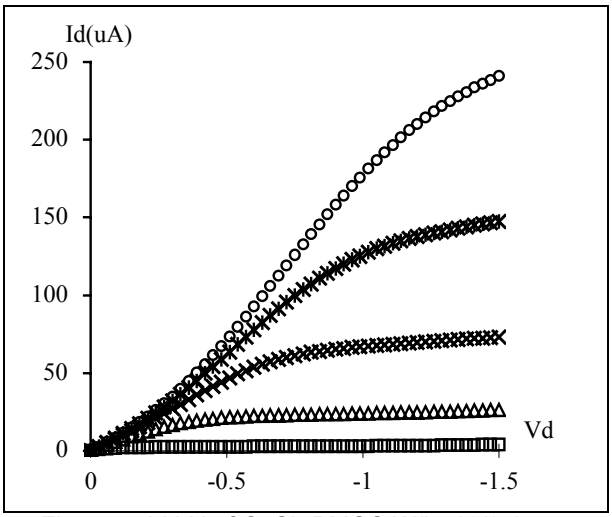

Figure 4. Id-Vd of $CoSi_2$ PMOS W/L=10/0.15um

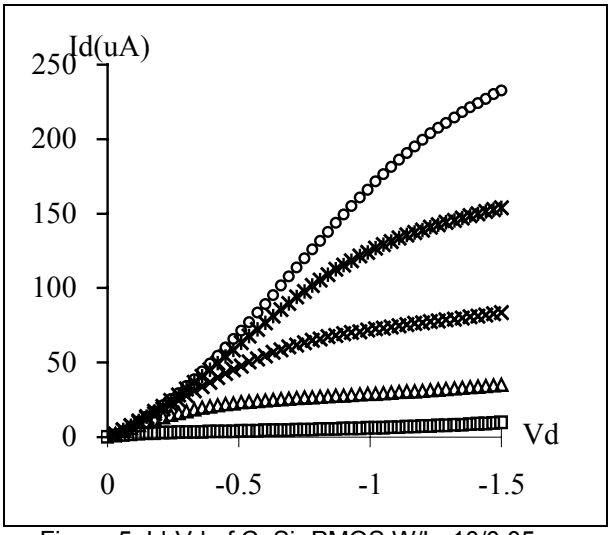

Figure 5. Id-Vd of $CoSi_2$ PMOS W/L=10/0.05um

4. Conclusions

In this paper, novel SB MOSFETs with convention nickel and cobalt silicide, low dose SDE and ultra-thin sidewall are presented. SB MOSFET clearly demonstrates the promising electrical characteristics such as good I_{on}/I_{off} ratio, gate-governed transport and the capability to suppressed SCE and DIBL in sub-100nm regime. It suggests that controllable tunnelling barrier of SB MOSFET is not only the merit of this structure, but also propose further scaling potential. Also, it can be anticipated that the device performance will be improved by using fully-depleted substrate and strengthen the feasibility on both digital and analog applications. Furthermore, this novel SB MOSFET structure is fully capable for process integration and compatible with state of art CMOS process technology.

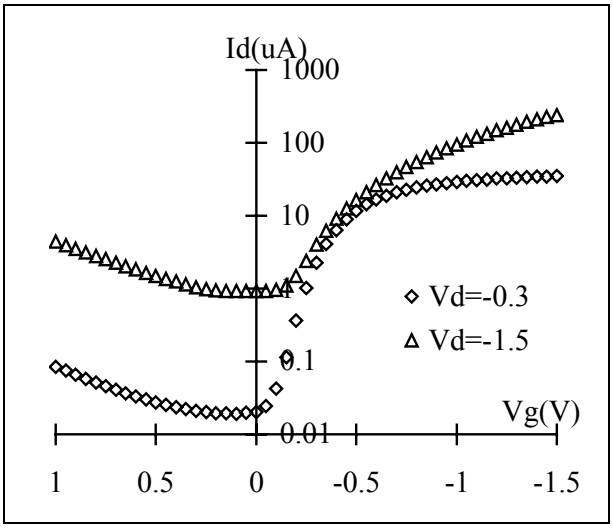

Figure 6. Id-Vg of $CoSi_2$ PMOS W/L=10/0.15um

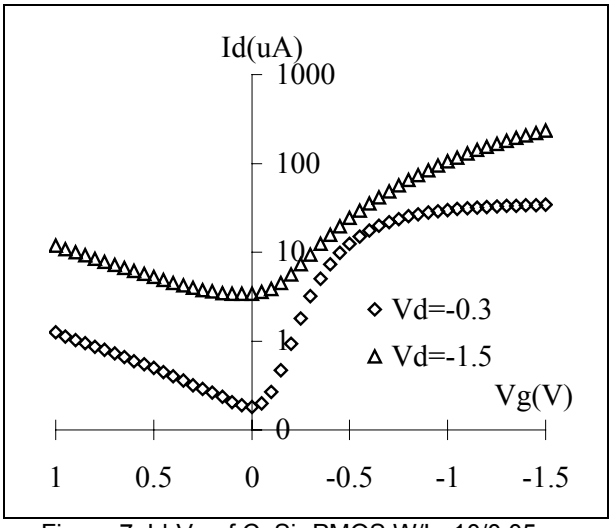

Figure 7. Id-Vg of $CoSi_2$ PMOS W/L=10/0.05um

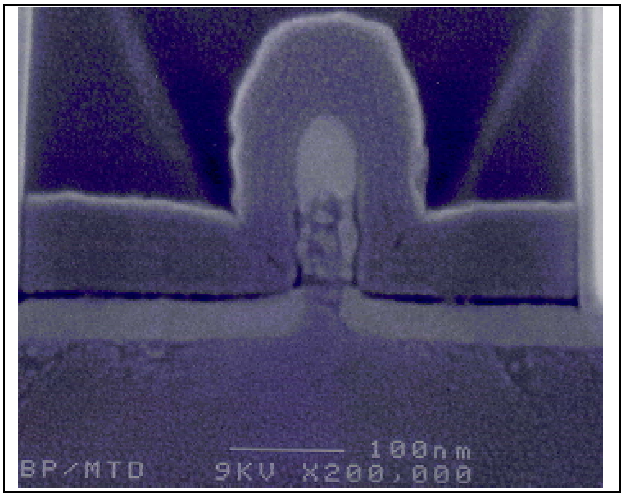

Figure 8. Cross Section SEM of 50nm SB NMOS with 10nm sidewall

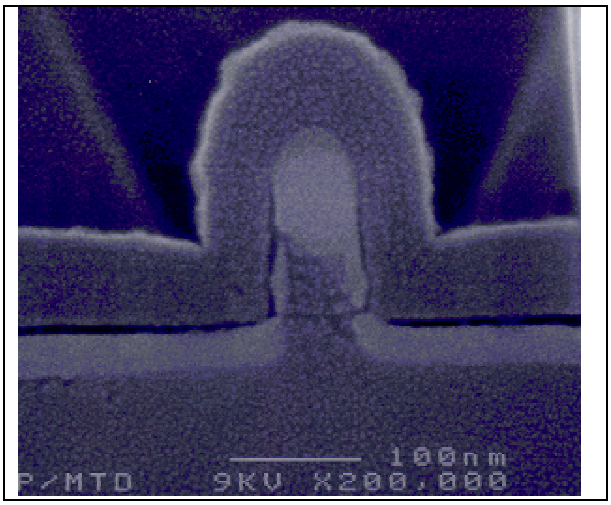

Figure 9. Cross Section SEM of 50nm SB PMOS with 10nm sidewall

5. Acknowledgement

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