Scaling Behaviour of Large-grain Polysilicon MOSFETs

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Abstract

The scaling properties of the large-grain polysilicon on insulator (LPSOI) MOSFETs are investigated. In conventional small grain polysilicon TFT, the defect related field emission at the drain end is the main source of device failure. With the device width scaling of LPSOI MOSFETs such effects reduces significantly. Therefore, a deeper scaling of the channel length of narrow LPSOI MOSFETs is possible, and lead to a significantly improved device performance. However, the short channel effects like DIBL start appearing after a certain channel length. A study of these effects can be used to optimize device and process design for high performance on MOSFETs on the LPSOI substrate.

1. Introduction

The polysilicon Thin-Film Transistor (TFT) technology has been emerging as a viable technology in the applications such as Active Matrix Liquid Crystal Displays (AMLCDs)[1] and three-dimensional (3-D) integrated circuits [2]. To meet the increasing demand of high performance and high density of polysilicon (p-Si) TFT circuits in such applications, a scaling of device dimensions is essential. Channel length scaling offers higher speed and lower supply voltage, while channel width scaling allows higher density and low power consumption.

Recently, MOSFETs fabricated using the LPSOI technology has demonstrated SOI like device performance [3]. In addition, the realization of 3-D circuits [4] as well as various novel device structure such as self aligned double and bottom gate structure [4,5] using the LPSOI technology, has motivated to enhance the device performance further. The common way to enhance the performance is the device scaling which leads to high mobility, low threshold voltage, and steep subthreshold slope. However, an increase of the off-state leakage current I_{off}. limits the further scaling, which is due to the presence of grain boundaries(GBs) and defects in the channel region especially at the drain end [6]. Such effects are more pronounced at large device width, since it has higher probability to cover the longitudinal GBs as well material defects. A significant improved performance of the device is expected when the device size reduced to the average grain size as probability to cover a GB reduces. Moreover, it has been reported that threshold voltage of the p-Si TFT's of sub-grain size decreases drastically when the device size reaches to average grain size [7-9].

In this paper, we have investigated scaling properties including the narrow width effects as well short channel effects of LPSOI MOSFETs. It was found that a rigorous scaling of narrow width device was possible. Meanwhile, the working devices size has been entered in the submicron regime, where the short channel effects as that of a *c*-Si MOSFET starts to appear. A proper understanding of the short channel effects on the LPSOI substrate can be instrumental in developing the high performance LPSOI MOSFETs circuits. However, the study of short channel and narrow width effects has been extensively performed on the conventional small grains p-Si TFTs [7-10]. So far, the large grain p-Si TFT has received limited attention. A better understanding of the small dimensions effects would facilitate the better device designs and process optimization and, hence, true 3-D circuits can be realized.

2. Experimental

The LPSOI MOSFETs were fabricated with standard SOI CMOS process on the LPSOI film, which was prepared by the metal induced lateral crystallization (MILC) and subsequent high temperature annealing process. The channel regions of the n-channel and p-channel LPSOI MOSFETs were doped with boron ($2\times10^{12}cm^{-2}$) and phosphorous ($8\times10^{12}cm^{-2}$), respectively. The gate oxide thickness was 110Å. The detail of fabrication procedure can be found in [3, 13]. A summary of general grain structural related parameters of LPSOI film for two types of devices is given below in Table. 1.

Table 1

	Physical grain size along channel length	Physical grain size along channel width	Si film thickness
Type-A	up to 100μm	up to 10μm	1000Å
Type-B	up to 10μm	up to 100μm	1000Å

3. Off-state Behaviour

It is well known that the scaling of the TFT was restricted by the defects related field emission at the drain end [11]. As the channel length of device is reduced, the gate controlled over the channel region becomes less effective, and effects like high I_{off} start dominating. The anomalous leakage current phenomenon is linked to defect related field emission at GB as well the drain end [11]. The phenomenon starts occurring well before the channel length entered in the submicron regime. This can be so significant that most of devices fail to function properly. However, in LPSOI MOSFETs, the I_{off} reduces with the width scaling as shown in Fig. 1. Therefore, channel length scaling of narrow devices can be achieved. The leakage current increases sharply when W_{eff} reaches a particular point, depending on the average grain size of the LPSOI film. This implies that the type-A structure can be used to obtain high performance short channel transistors only when the device widths are small. On the other hand, type-B devices allow the channel length to scale beyond that of type-A devices, due to larger grain size along the channel width. Therefore, the type-B layout should be used when the channel length of a transistor is smaller than a certain critical value.

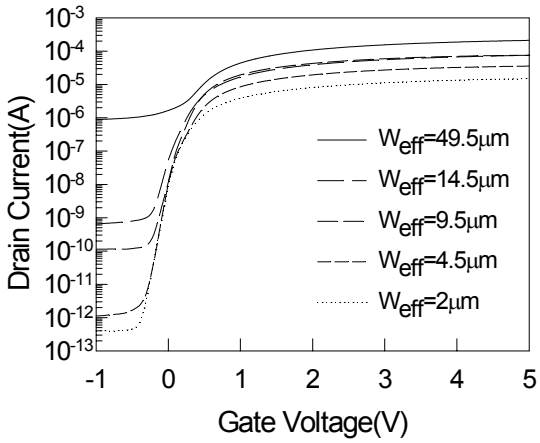

Figure 1: The typical subthreshold behaviour of the n-channel type-A LPSOI MOSFETs (L_{eff} =2.5μm) at different W_{eff} to illustrate the increasing level of I_{off}.

Fig. 2 provides a guideline for selecting type-A or type-B devices at a given channel length and width. The boundaries are determined by the channel length when the average leakage current exceeds a value of 10^{-6} μA/μm. Each data point was averaged over 35 devices. For the three regions shown in Fig. 2, both type-A and type-B devices function in region A while only type-B device functions in region B. In region C, both type-A and type-B devices fail to function with the present technology. These results also indicate that a low leakage current can be maintained for very narrow devices with both type-A and type-B layouts. So, more vigorous channel length scaling is possible for extremely narrow devices on the LPSOI films.

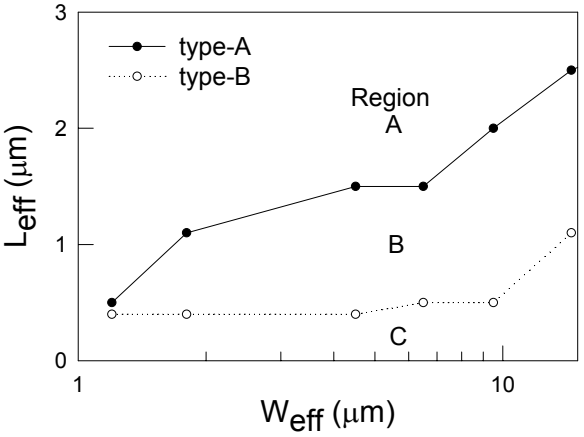

Figure 2: The minimum function effective channel length (L_{eff}) as function of effective channel width (W_{eff})for n-channel type-A and type-B LPSOI MOSFETs.

4. Narrow Width Effects

From the previous section it was learn that device found to working at narrow device width. To investigate the narrow device narrow width effect, the parameter threshold voltage V_t was chosen. Fig. 3 shows the effect of width scaling of LPSOI MOSFETs on the average V_t. The V_t of MOSFETs were defined at a fixed normalized drain (100nA) current with V_{ds} = 0.05V. The effect of width scaling is nearly same for both n-channel and p-channel LPSOI MOSFET. A significant decrease in V_t of both n-channel and p-channel devices is observed when W_{eff} is lower than 2μm. When channel width becomes smaller than the average grain width, the concentration of defects decreases in the channel region decreases. To investigate the decrease in V_t, the trap density in the channel region was calculated using the method described by Levinson [12]. According to this method the trap density can be obtained from the slope of the $ln(I_d/V_g)$ versus $1/V_g$ curve. The calculated value of trap densities for different W is shown in Fig. 4.

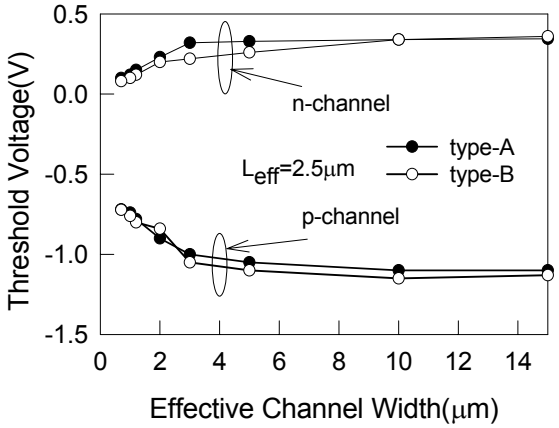

Figure 3: The average V_t of n-channel and p-channel type-A and type-B device as a function of W_{eff} .Each data point was averaged from 20 devices.

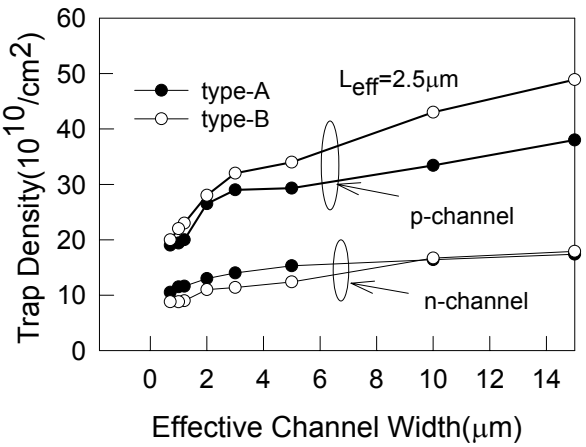

Figure 4: The average trap density of n-channel and p-channel type-A and type-B device as a function of W_{eff}.Each data point was averaged from 20 devices.

The trap density has shown a sensitivity similar to that of V_t at different channel widths. This study suggests that small sized devices have a small amount of the trap density. A low value of V_t as well as trap density at smaller width can also be related to the small geometry of the islands. Possibly the small islands size has assisted the formation of single grain Si island according to theory of secondary crystallization proposed in [13]. Due to the single *c*-Si properties at small size, the well-developed and advanced process and engineering techniques of Si MOSFET can be applied to smaller sized LPSOI MOSFETs in order to counter short channel effects as well to obtain the high device performance.

5 Short Channel Effects of Narrow Width Devices

As we observed from the previous section that the channel length scaling of the device can be performed successfully at narrow width. Fig. 5 illustrates the V_t dependency of n-channel and p-channel LPSOI MOSFETs over the channel length.

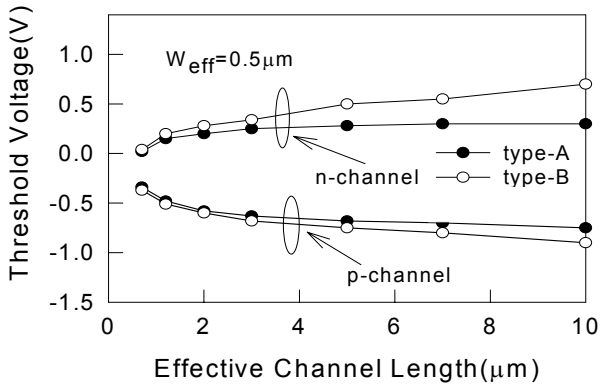

Figure 5: The average V_t of n-channel and p-channel type-A and type-B device as a function of L_{eff}. Each data point was averaged over 20 devices.

The V_t of all types of devices decreases with the channel length scaling in a nearly similar manner. A significant decrease in V_t was observed at short channel lengths. This decrease in V_t can be due to the short channel effects. In order to understand these effects, the LPSOI device characteristics were investigated at different dimensions and V_{ds}. These effects set the limits of the device scaling.

Fig. 6 and 7 show the subthreshold characteristics of short n-channel and p-channel type-A LPSOI MOSFET, respectively. A serious punchthrough like phenomenon is observed in devices when the W_{eff} is equal to 0.7μm. However, this phenomena is suppressed when the W_{eff} is reduce to 0.5μm even though a considerable drain induced barrier lowering (DIBL) is observed. The suppression of short channel effects can be due to both lower density of the trap states and better gate control over the channel region at the narrow width according to explanation proposed in [14]. Therefore, the narrow width device can be scaled down further. It can be seen from Figs. 6 and 7 that the DIBL can be the one of the major problem for the scaling. The DIBL at W_{eff} = 0.5 and 0.7μm was investigated in terms of the ΔV_t at two different V_{ds}, 0.05V and 1.05V as shown in Fig. 8. The p-channel and n-channel LPSOI MOSFETs are having nearly same amount of DIBL. An increase in DIBL can be observed with an increase in width, which can be due to the weak control of gate over the channel region. An extensive research on the DIBL effect of narrow width Si-MOSFET has been provided in [14,15].

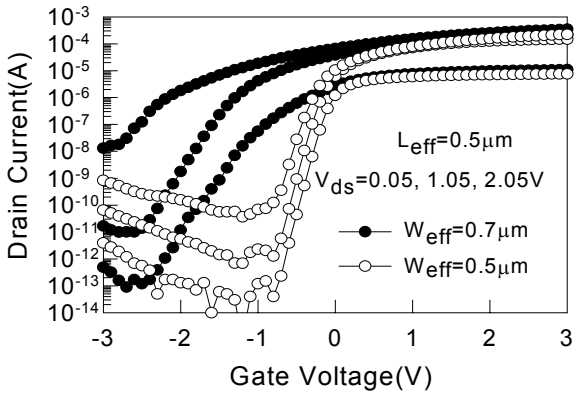

Figure 6: Subthreshold characteristics of short n-channel LPSOI MOSFETs at different V_{ds} and W_{eff}.

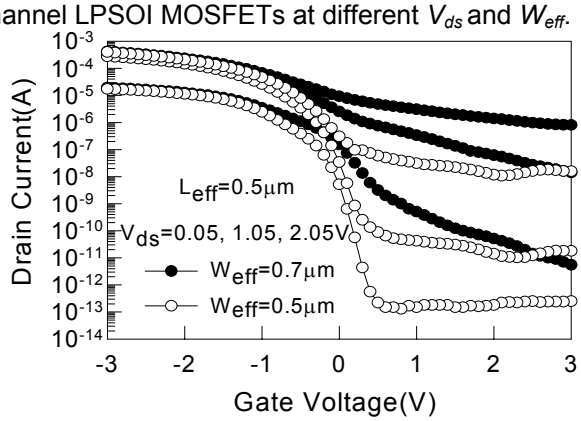

Figure 7: Subthreshold characteristics of short p-channel LPSOI MOSFETs at different V_{ds} and W_{eff}.

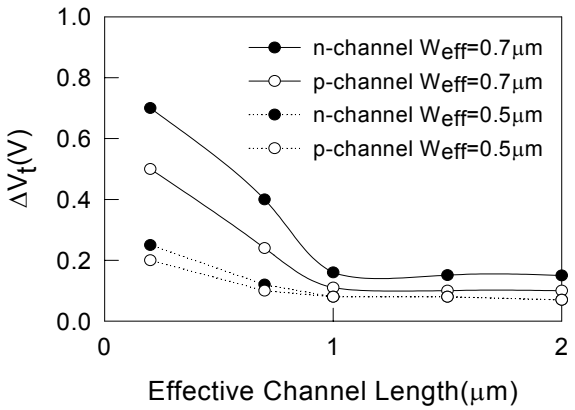

Figure 8: Shows the averaged value of the ΔV_t for n-channel and p-channel type-A LPSOI MOSFET as function of L_{eff}. The each data point was averaged over 20 devices. The ΔV_t measured from V_{ds} = 0.05V and V_{ds} =1.05V subthreshold curve.

6 Discussion

Interestingly, the behavior of the LPSOI MOSFETs at narrow widths appears to be the same as that of SOI MOSFET [14]. The studied LPSOI MOSFETs were using the MESA isolation technique. So far in LPSOI MOSFET technology no techniques such as LDD (lightly doped drain) and doping profile tailoring of channel region has been applied to counter the short channel effects. Probably, further scaling can be possible with the application of an appropriate channel doping profile and device design. The reduction of the Si film thickness can lead to much improved device performance as well better control of short channel effects [16].

7 Conclusion

The narrow width and short channel effect on both n-channel and p-channel LPSOI MOSFETs has been investigated. At wide device size, the grain boundaries and material defects are dominant, the threshold voltage starts decreasing when channel width becomes comparable to average grain size. This decrease becomes more significant when the width approaches to 2 μm. The finding of trap density supports the decrease threshold voltage and off-state leakage current. The short channel effects such as DIBL and punchthrough-like phenomena appears to reduce with the width scaling. The narrow width device exhibits a better channel scaling properties compared to wide devices. An enhanced performance of the LPSOI MOSFETs can lead to the better realization of true 3-D circuits.

Acknowledgement

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