Si Nanocrystal Based Memory Structures by Ultra Low Energy Implantation for Low Voltage/Low Power Applications

P.Dimitrakis, E.Kapetanakis, P.Normand, D.Tsoukalas
NCSR "Demokritos", IMEL, P.O.Box 60228, Ag.Paraskevi, 153 10, GREECE
pdimit@imel.demokritos.gr

Ben Assayag, C. Bonafos, M. Carrada, D.Chassaing, A. Claverie,V.Soncini[1]
CEMES/CNRS, Toulouse, France
[1] *STMicroelectronics Agrate Italy*

Abstract

Metal-Oxide-Semiconductor structures exhibiting significant charge storage due to the presence of Si nanocrystals into the amorphous oxide matrix have been fabricated by 1keV Si ion implantation into 10nm SiO_2 gate oxide layer. The effect of the implanted dose and annealing temperature on the memory window is reported. Large shifts of flat-band voltage are achieved at very low programming electric fields (4V at 2MV/cm).

1. Introduction

Memory cells consisting of a MOSFET with a charge storage medium made of nanocrystals are promising candidates for high storage density low power applications. Nanocrystal memories obtained by ultra-low energy silicon implantation and subsequent annealing have been recently reported [1]. This work gave attractive results but also revealed the need for reliable and systematic experimental studies that will offer a global exploration of the potential of the ion beam synthesis technique. In this work, charge storage effects of Si-implanted SiO_2 as a function of the implantation dose and annealing temperature are investigated through capacitance and current voltage measurements of MOS capacitors.

2. Experimental Procedure

10nm thick SiO_2 layers were thermally grown on 8 inch p-type (100) Si wafer. The average substrate doping was at the $6\times10^{15}cm^{-3}$ level. These layers were subsequently implanted with ^{28}Si atoms with an energy of 1keV at doses varying from 2×10^{15} to 1.5×10^{16} Si/cm^2. The projected range of the implanted Si atoms was estimated by LSS theory to be about 3.5nm. This simulation allows us to calculate the concentration of excess Si atoms into the oxide matrix and thus the supersaturation of Si. A SiO_2 layer of 16nm was then deposited onto the initial implanted oxide layer, increasing the control oxide thickness and hence the asymmetry of barrier heights for carrier injection. In order to create Si nanocrystals (ncs) thermal annealing was subsequently performed at two different temperatures, 950°C or 1050°C, in inert ambient for 30min. Finally, Al was evaporated on both sides of the structures and used as top-bottom capacitor's electrodes (see Fig.1). Sample reference code numbers are presented in Table 1. A comprehensive electrical characterization of the final devices was followed. C, G, I-V measurements were utilized in order to evaluate the memory behaviour of the implanted SiO_2 layers. The evaluation parameter was the flat-band shift after the application of different polarity electric fields.

Table 1. Sample reference code numbers

Code Number	Annealing Temperature (°C)	Implantation Dose (Si/cm^2)
102A , B	950, 1050	2×10^{15}
105A , B	950, 1050	5×10^{15}
108A , B	950, 1050	8×10^{15}
110A , B	950, 1050	1×10^{16}
115A , B	950, 1050	1.5×10^{16}

3. Results and Discussion

3.1. TEM Analysis

Transmission electron microscopy performed on oxides without additional SiO_2 deposition reveals the presence of a single layer of Si nanocrystals into the gate oxide for doses of 8×10^{15} cm^{-2} and above [2]. A typical HREM image of a Si nc embedded into the SiO_2 matrix is presented in figure 2. The thickness of the ncs band is in the 2.4 nm range for the 8.10^{15} and 1.10^{16} cm^{-2} doses and reaches 3.4 nm for the 1.5×10^{16} cm^{-2} dose. For all samples the ncs band starts at 3.5nm from the surface. The above dimensions are relatively insensitive to annealing temperature variations.

3.2. Electrical Characterization

High Frequency (1MHz) Capacitance – Voltage measurements are used to estimate the net oxide charge concentration and the flat-band voltage, V_{FB}, of each sample. Capacitance-voltage measurements are carried out with a step delay time of 1s and a sweep rate of 0.1V/s. The voltage sweep starts from inversion to accumulation and back to inversion. The indication for the memory effect is the hysteresis in the C-V curves. Hysteresis would be observed between the two characteristics with opposite sweep rates. This happens because there is an appreciable density of states deep in the oxide having time constants longer than the bias time necessary to sweep the voltage [3]. The magnitude of the flat-band voltage shift is proportional to the trapped charges Q_{ot} into electronic states (traps) that are present in the SiO_2 matrix and/or in the Si ncs. A significant "memory effect" is observed for doses larger than 5×10^{15} cm^{-2}. The application of a positive voltage results in electron injection into SiO_2 trapping centres originating from the interface, deep traps in the ncs and unsaturated Si bonds due to the excess Si atoms into the oxide (oxide bulk traps) [4,5]. The annealing process in the range of 950-1050°C removed most of the implantation damage. The application of a negative voltage results in holes injection from Si substrate and/or electron injection from the gate into the SiO_2.

From a device point of view, a voltage sweep from inversion to accumulation results in a positive shift of the C-V curve with a flat-band voltage V_{FB}^{+}, while the voltage sweep in the opposite direction results in a negative shift of the C-V curve with a flat-band voltage V_{FB}^{-}. The value of V_{FB}^{+} or V_{FB}^{-} depends on the starting bias voltage, i.e. on the starting applying electric field (fig. 3).

In figure 4(a), the experimental values of V_{FB}^{+} and V_{FB}^{-} are presented. In the case of MOS transistor, these quantities are related to the threshold voltage and hence govern its operation status (on/off with respect to V_{FB}^{+}/V_{FB}^{-}). It is obvious that these quantities change almost symmetrically with respect to their initial values, except for the case of capacitors implanted with $1.5x10^{16}$ Si cm^{-2}. For these MOS devices, we find that as the electric field increases V_{FB}^{+} changes very little while V_{FB}^{-} saturates very quickly. In other words, more holes are trapped into the SiO_2 matrix than electrons. Similar results have been reported in the literature [4, 6, 7]. This difference in the stored charge would indicate that the number of injected holes is greater than the number of injected electrons. However, the same phenomenon would be observed if the injected holes are equal to the injected electrons but the electrons are tunnel back faster than holes, as reported by Shi et al [5].

The flat-band voltage shift, $\Delta V_{FB}=V_{FB}^{+}-V_{FB}^{-}$, as a function of the electric field is shown in figure 4(b) for *different implantation doses*. ΔV_{FB} is a figure of merit of the programming voltage window, i.e. the lower and the highest gate bias necessary to be applied in order to switch between states "0" and "1". It is obvious that as the implantation dose increases, the electric field needed to obtain a given flat-band voltage shift decreases. For 1.5×10^{16} Si cm^2 implanted devices, both V_{FB}^{+} and V_{FB}^{-} and hence ΔV_{FB} saturate. A fully charged memory window of 4V is achieved for a programming electric field of about 2MV/cm. According to [8,9], silicon doses larger than $1x10^{16}$ Si cm^{-2} implanted at 1keV are suitable for the fabrication of well-crystallized Si islands after annealing temperature as low as 900°C. For lower doses the nc formation strongly depends on the annealing temperature. We attribute the rather abrupt flat-band voltage saturation observed for the 1.5×10^{16} Si cm^2 implanted devices to the near complete saturation of the traps associated with the presence of ncs. On the other hand the absence of abrupt-saturation found for the other doses is viewed as a reflection of the saturation behaviour of small ncs and a substantial population of isolated Si atoms present simultaneously. These arguments become stronger considering the experimental results for the different annealing temperatures described in the following paragraphs.

Table 2. The effect of Si supersaturation on device performance characteristics

Code Number	Super-saturation (%)	E_{cr} (MV/cm)
102A , B	10	>4
105A , B	25	>4
108A , B	39	>3.5, >4
110A , B	49	2.97, 2.38
115A , B	74	1.91

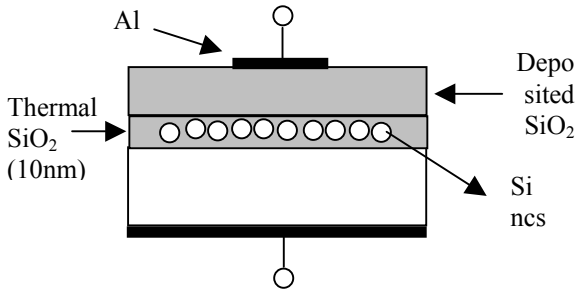

Figure 1. The tested memory structure.

The *effect of the annealing temperature* is shown in figures 5(a) and 5(b). The onset of charge storage is enhanced for higher annealing temperature. Oxides implanted with 8×10^{15} Si/cm^2 can store more charges at low electric fields when the annealing is performed at 950°C. This is because at higher annealing temperatures, the oxide trap concentration is reduced and the excess Si

atoms form small clusters at a longer distance from the Si/SiO_2 interface.

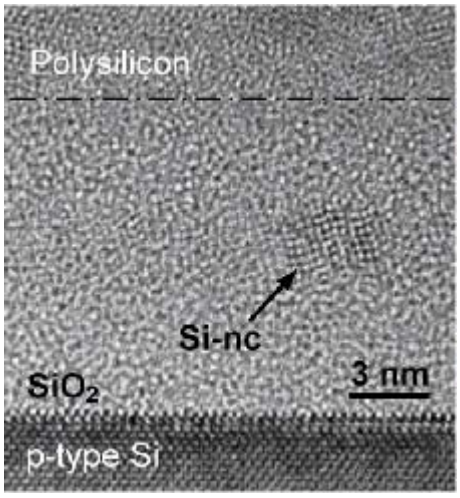

Figure 2.High Resolution TEM image of Si nc observed in a 10 nm-thick, $1x10^{16}$ Si cm^{-2} implanted oxide annealed at 1050°C for 30min. Polysilicon was deposited for TEM observation after the post implantation annealing

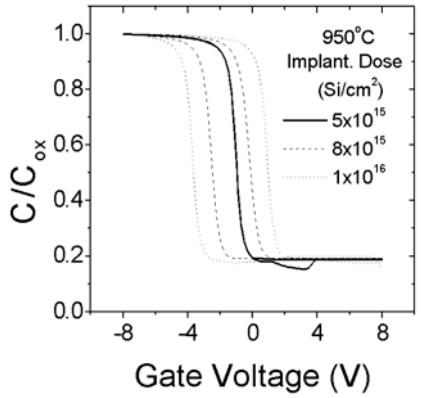

Figure 3. The influence of implantation dose on charge storage into Si ncs embedded in SiO_2 matrix. The annealing temperature is 950°C

For oxides implanted with 1×10^{16} Si/cm^2 formation of nanocrystals occurs at both temperatures; with increasing temperature crystallite lateral size increases (not shown here) and the density of oxide traps is substantially reduced. Consequently, the charge storage for samples annealed at 1050°C takes place principally at the energy states located within or at the interface of nanocrystals. Hence, the flat-band voltage shift changes more rapidly and saturates near 3MV/cm.

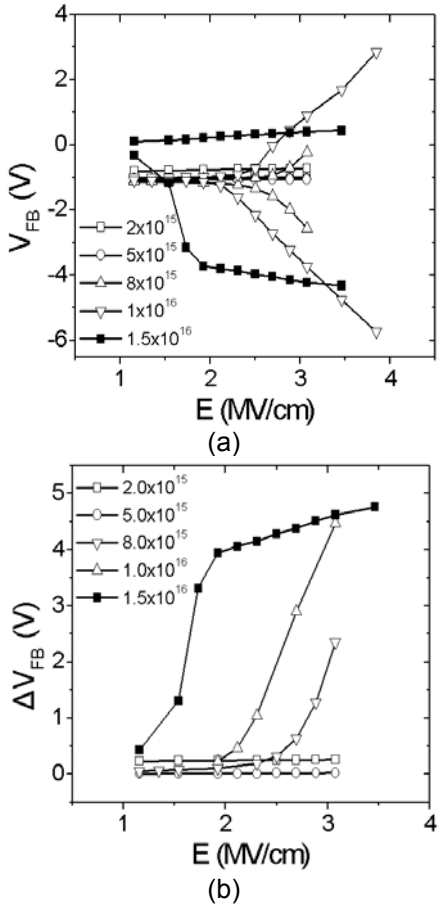

Figure 4. (a) The dependence of the flat-band voltage on the electric field and (b) flat-band voltage shift vs the applied electric field. The annealing temperature is 950°C.

Regarding the accumulation condition under negative gate bias voltage, all samples show J_G-V *curves* with one or two humps (fig. 5(b)). J_G-V curves were obtained with a sweep rate of 0.4V/s, starting from zero bias until breakdown occurs. Similar humps have been reported before [10], but no satisfactory interpretation has been offered. The humps may be closely related to a mechanism of current flow towards the implanted Si-sites at the corresponding bias voltage. Additionally, our samples show clear negative dynamic resistance in the region below –10V. It is believed that the presence of negative dynamic resistance is due to the lowering of the neutral trap level with increasing gate bias. The neutral traps generated by Si-implantation are 3eV below the SiO_2 conduction band [10]. The gate currents measured under accumulation conditions are mainly determined by electron injection into SiO_2 from the metal gate and/or hole injection from the accumulated Si substrate.

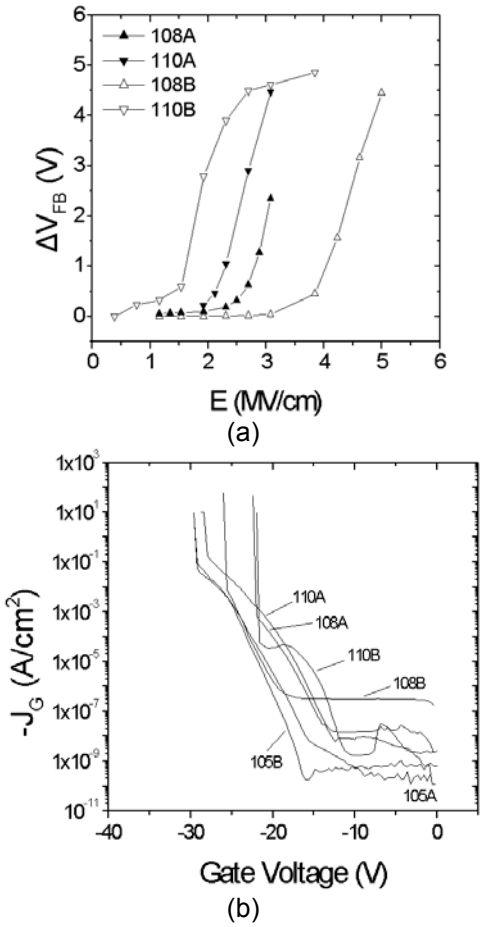

Figure 5. The influence of annealing temperature (a) on charge storage into Si ncs embedded in SiO_2 matrix and (b) on the J_G-V characteristics in accumulation.

In general, the higher is the implantation dose or the annealing temperature the lower the breakdown voltage.

4. Conclusions

Low-energy Si implantation into thin SiO_2 can be used to form two-dimensional Si nanocrystal arrays capable of substantial charge storage. As a consequence, flat-band voltage shifts as large as 4V can be achieved by applying an electric field less than 2MV/cm. By changing the implantation dose and the annealing temperature the programming electric field can be tuned.

5. References

[1] E.Kapetanakis, P. Normand, D. Tsoukalas, K. Beltsios "Room-temperature single-electron charging phenomena in large area nanocrystal memory obtained by low-energy ion beam synthesis." *Appl. Phys. Lett.* **80**, 2002, pp. 2794-2796

[2] G. Ben Assayag, C. Bonafos, M. Carrada, D. Chassaing, A. Claverie, P. Normand, D. Tsoukalas, P. Dimitrakis, E. Kapetanakis, V. Soncini, M. Fanciulli, M. Perrego, "Effect of Ion Implantation Energy and Dose on the positioning of Silicon nanoparticles embedded in Ultrathin SiO_2", Ion Implantation Technology, IIT 2002, Taos, New Mexico, USA, September 22-27 2002, accepted for presentation.

[3] E.H.Nicollian, A.Goetzberger, "The Si-SiO_2 interface-Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique", *Bell Syst. Tech. Journal* **XLVI**, 1966, p.1055

[4] Y.Shi, K.Saito, H.Ishikuro, T.Hiramoto, "Effects of Interface traps on charge retention time characteristics in Silicon – quantum – dot – based metal – oxide - semiconductor diodes", *Jpn.J.Appl.Phys.* **38**, 1999, p.425

[5] A.Kalnitsky, A.R.Boothroyd, J.P.Ellul, E.H.Poindexter, P.J.Caplan, "Electronic states at Si-SiO_2 interface introduced by implantation of Si in thermal SiO_2", *Solid State Electron.* **33**, p.523

[6] A.Kalnitsky, J.P. Ellul, E.H.Poindexter, P.J.Caplan, R.A. Lux, A.R. Boothroyd, "Rechargeable E′ centers in silicon-implanted SiO_2 films", *J.Appl.Phys.* **67**, 1990, pp.7359-7367

[7] Y.Shi, K.Saito, H.Ishikuro, T.Hiramoto, "Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals.", *J.Appl.Phys.* **84**, 1998, p.2358-2360

[8] S.Coffa, E.Castagna, C.Bongiorno, "Optical and structural properties of Si nanocrystals arrays formed by ultra low energy Si implants into thin gate oxides", *E-MRS*, Strasbourg, 2000, R-II2.

[9] P.Normand, K.Beltsios, E.Kapetanakis, D.Tsoukalas, T. Travlos, J. Stoemenos, J.Van Den Berg, S.Zhang, C.Vieu, H.Launois, J.Gautier, F.Jourdan, L.Palun, "Formation of 2-D arrays of semiconductor nanocrystals or semiconductor-rich nanolayers by very low energy Si or Ge ion implantation in silicon oxide films", *NIMB* 178/1-4, 74-77, 2001

[10] T.Matsuda, T.Ohzone, T.Hori, "Time dependent dielectric breakdown characteristics of MOS capacitors with Si-implanted SiO_2.", *Solid-State Electron*. 39, 1996, pp.1427-1434.

6. Acknowledgements

This work was financially supported by the NEON/GROWTH EU project under contract GRD1-2000-25619.