

A Novel Dynamic Threshold Operation Using the Electrically Induced Junction MOSFET in the Deep Sub-micrometer CMOS Regime

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Abstract

With CMOS scaling into the Sub-100nm regime, the supply and the threshold voltages need to be scaled proportionately. This necessitates addressing of low power CMOS device design issues. The idea of a Dynamic Threshold MOSFET (DTMOS), without the associated substrate loading effects, is a key to addressing the problems associated with device scaling for low power CMOS.

This work focuses on the device optimisation for such low power ULSI circuits using a novel Electrically induced junction (EJ)-MOSFET as a DTMOS. Such an implementation can be used without the additional substrate loading effects and the supply voltage limitations, commonly associated with conventional DTMOS operation. Our detailed dc as well as transient simulations bring out the advantages of this novel structure.

1. Introduction

The dynamic threshold MOSFET (DTMOS) operation has attracted lot of interest in CMOS community in the last few years [1]. The need for such a device arises for low power, high performance applications. There are many ways a DTMOS can be implemented in Very Large Scale Integrated (VLSI) circuits. One and foremost of those is by tying substrate of the transistor to its gate. As the substrate bias increases (V_{SUB}), along with the gate bias (V_{GS}), bulk charge in silicon is compensated. This reduction in bulk charge lowers V_T of the device and consequently leads to a higher drive current (I_{ON}) due to increased available gate overdrive V_{GT} ($=V_{GS}-V_T$). However, such an implementation cannot be used for supply voltages above the cut-in voltages of the S/D junctions. More importantly, the bulk capacitance of transistor adds to

total parasitic capacitance at the input (C_{IN}), which must be charged by the input signal. Thus, this simple DTMOS implementation achieves higher I_{ON} while increasing the C_{IN} , with the overall result that there is degradation in the circuit speed.

In this work, we propose a novel implementation of DTMOS using Electrically Induced Junction (EJ) MOSFET. The performance of both the implementations has been evaluated using dc as well as transient simulations.

2. EJ-MOSFET

An EJ-MOSFET device has been shown to improve the device performance by a few researchers [2]. An alternative and better scheme to implement the EJ-MOSFET has been recently reported [3]. The latter achieves superior device characteristics due to replacement of its shallow n^+ extensions with shallow p^- extensions.

In such a device, as shown in Fig. 1, the effective channel length (L_{CH}) is lower, compared to a conventional MOSFET, as longer and inverted p^- regions act as shallow extensions in the presence of V_{GS} , i.e. $L_{ON} < L_{CH}$. Whereas, at $V_G=0$, the effective channel length is equivalent to L_{OFF} , as shown in the schematic in Fig. 1. Since V_T of the EJ-MOSFET depends on the effective channel length, there is a modulation of V_T with the gate bias, which is beneficial for the DTMOS operation.

3. Simulation

ISETCAD [4] process simulator DIOS, device simulator DESSIS, and mesh generator MDRAW have been used for all the energy balance and mixed-mode simulations reported in this work. Here we compare the performance of three devices, namely, the conventional

device, a DTMOS device that has its substrate tied to gate, and EJ-MOSFET that has been simulated with a few modifications in conventional CMOS process flow. The conventional device has a gate length of 120nm and all other technology parameters conform to SIA projections [5]-[6] for this technology node.

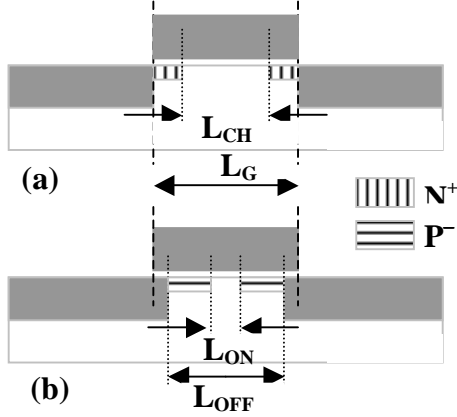


Figure 1. Device structures: (a) conventional device (b) EJ-MOSFET

4. Results and discussion

The p^- regions have first been superimposed by mesh-generation tool on a conventional device structure, simulated using process simulation. In order to optimise the EJ-MOSFET, I_{ON} and I_{OFF} have been plotted as a function of the length of p^- region with doping concentration as a parameter, shown in figures 2 and 3.

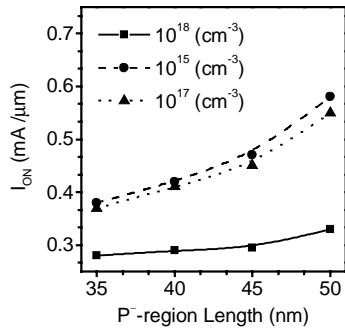


Figure 2. I_{ON} as a function of p^- region length

As can be seen from Fig. 2, I_{ON} increases with length of the p^- regions. This is because L_{ON} decreases for $V_G > V_T$ as length of p^- regions increases. I_{ON} also increases with decrease in the doping of p^- regions as lower the doping, higher will be the inversion layer charge in the p^- regions, decreasing the series resistance. Fig.3 shows that longer p^- regions result in higher I_{OFF} . This is because of a reduction in L_{ON} with increasing p^- length. Higher doping in the p^- regions lowers I_{OFF} , at the same time reducing I_{ON} .

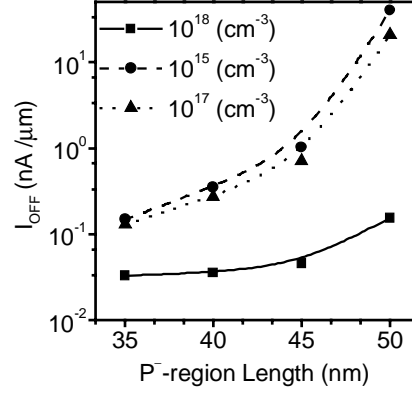


Figure 3. I_{OFF} as a function of p^- region length

To optimise the device performance, length and doping concentration of p^- regions is chosen to be 45nm and 10^{15} cm^{-3} respectively. Further, I_D-V_{GS} characteristics of the three devices have been compared in Fig. 4. Here, V_{DS} has been kept at a low value ($=0.05V$) and V_{GS} is ramped from 0 to 1.0V for conventional and EJ-MOSFET devices. V_{GS} for DTMOS device has been ramped only up to 0.8V in order to prevent turn-on of the substrate-source/drain (S/D) diodes.

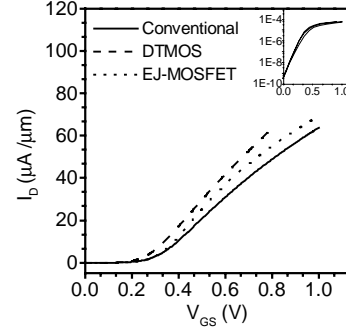


Figure 4. I_D-V_{GS} , inset shows the semi-log plot

It is seen from Fig. 4 that DTMOS achieves higher drive currents compared to the EJ-MOSFET and conventional devices. The improvement of EJ-MOSFET over conventional device can also be clearly seen in this figure. Inset in Fig. 4 shows the same I_D-V_{GS} plot on the semi-log scale, which shows that sub-threshold currents are nearly identical for all three devices. Figure 5 shows I_D-V_{DS} characteristics for three devices at V_{GS} values of 0.3V, 0.6V, and 0.8V. In this simulation, V_{DS} has been ramped from 0 to 1.0V. As expected from Fig. 4, I_D in Fig. 5 is highest for DTMOS device and lowest for conventional device, for all the three V_{GS} values. Whereas, a close examination of Fig. 5 reveals that EJ-MOSFET also shows improved saturation behaviour

which could be beneficial for analog applications. The improvement is expected because of the induced shallow inversion layer acting as source-drain extensions.

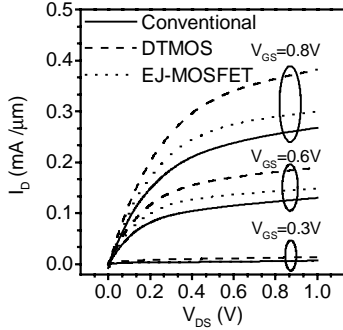


Figure 5. I_D - V_{DS} characteristics

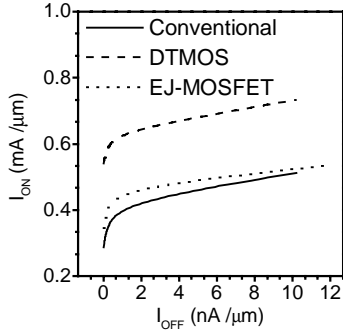


Figure 6. I_{ON} at various I_{OFF} values

In order to estimate the maximum I_{ON} that can be achieved for a given I_{OFF} value, the three structures are compared for their drive currents at identical I_{OFF} values in Fig. 6. As can be seen, EJ-MOSFET scores over the conventional MOSFET in terms of better I_{ON} - I_{OFF} performance. This suggests that the on current can be optimised in the case of EJ-MOSFET by a proper design of p^- length and doping concentrations.

In order to evaluate the transient performance of these devices, the DESSIS-SPICE interface of ISETCAD [4] has been used for mixed-mode simulations. Firstly, p-channel MOSFETs with identical V_T values have been simulated for the three structures. Then circuit schematic shown in Fig. 7 is used to extract the input capacitance of the three CMOS inverters. The n-channel MOSFETs in the inverter have a width (W_N) to length ratio (W_N/L) of 10, whereas width of p-channel transistors (W_P) has been adjusted to make the rise and fall delay values equal ($W_P/W_N=1.5$, for all three devices).

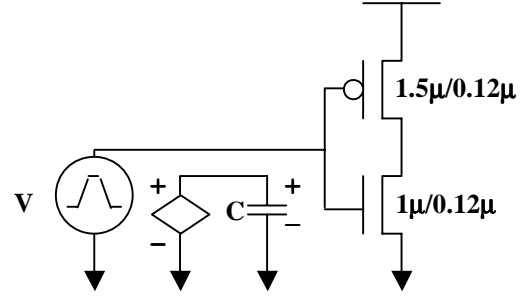


Figure 7. Circuit diagram for capacitance extraction

In Fig. 7, a voltage pulse (0-VDD) drives input of the inverter. The unity gain current-controlled-current-source (CCCS) "I" is controlled by current flowing through the voltage source "V". This current integrated over the rise time of input pulse using a 100fF capacitor "C", gives C_{IN} of the inverter. C_{IN} values extracted by this method come out to be 5fF, 7.33fF and 4.9fF for conventional, DTMOS (gate-tied-to-body) and EJ-MOSFET devices, respectively. The higher C_{IN} value for DTMOS inverter, as compared to a conventional inverter, is due to additional substrate capacitance that comes in parallel with C_{IN} of a conventional inverter.

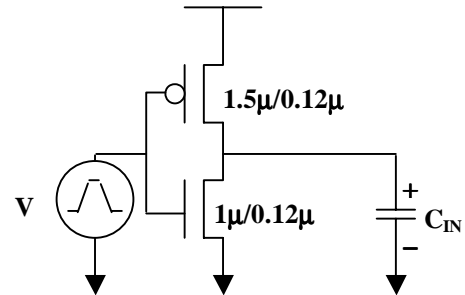


Figure 8. Circuit diagram for delay extraction

Figure 8 shows the CMOS inverter used to extract propagation delay for the three cases. This circuit has been designed to operate at an electrical effort ($H=C_{OUT}/C_{IN}$) equal to 1, i.e. the inverter drives a capacitive load equal to its own C_{IN} value. Further, Fig. 9 shows the propagation delay (τ) as a function of supply voltage (V_{DD}). As can be seen from Fig. 9, higher C_{IN} value of DTMOS inverter degrades its transient performance offsetting any improvement that is expected due to improved transistor drive current. On the other hand, EJ-MOSFET inverter achieves lowest delay values amongst the three inverters at all V_{DD} values. Also, as can be seen from Fig. 9, the delay advantage with EJ-MOSFET inverter improves with supply voltage scaling.

This suggests that EJ-MOSFET can play a vital role in optimising performance of deep sub-micrometer CMOS for low power applications.

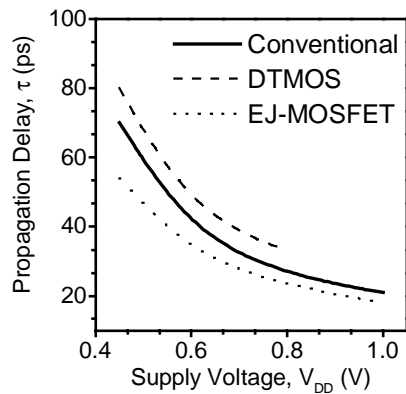


Figure 9. Propagation delay as a function of V_{DD}

5. Conclusions

Both dc and transient performance of EJ-MOSFET device has been compared with conventional and DTMOS devices. The EJ-MOSFET device shows moderate improvement in the dc characteristics (as compared to DTMOS) over the conventional MOSFET structures, and superior transient characteristics amongst all the three devices. It is also clear from these simulations that with proper optimisation of EJ-MOSFET parameters (p^- doping and length), it is possible to modulate its threshold voltage without the associated substrate loading effects.

12. References

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