SiGe pMOSFETs Fabricated on Novel SiGe Virtual Substrates Grown on 10µm x 10µm Pillars.

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Abstract

Silicon germanium pMOSFETs have been fabricated on novel silicon germanium virtual substrates. The SiGe virtual substrates were grown by MBE on 10µmx10µm silicon pillars fabricated by dry etching trenches into the original silicon substrate. The pillars promote relaxation of the SiGe virtual substrate and reduce cross hatch on the wafer surface.

The devices have 5nm silicon germanium active layer with a germanium content of 70% grown on top of a relaxed virtual substrate with a germanium content of 30%. A 2nm silicon cap separates the SiGe channel from the gate oxide.

Device characteristics show a improvement in on state drive current in these SiGe devices of 40% over their conventional silicon counterparts.

1. Introduction

The use of high mobility strained layers grown on top of relaxed silicon germanium virtual substrates has been shown by a number of authors to increase channel carrier mobility and device current drive [1-5]. However, the use of such a technique is limited by the formation of cross hatch patterns on the surface of the relaxed SiGe virtual substrates, formed by the stress fields associated with the SiGe buffer layer as it adapts to the different lattice constant of the silicon substrate wafer [6].

Reducing the lateral dimensions of the growth zone has been shown to reduce or eliminate cross hatch. This is achieved by growing such layers on top of microscopic pillars [6-7], as shown in figure 1. The edges of the pillars are suitable sites for the nucleation of dislocations. This reduces the amount of cross-hatch and improves wafer surface planarity [6].

In this paper we present a novel SiGe pMOSFET device fabricated on top of such pillars.

2. Device Fabrication

Device fabrication started with fabrication of the pillars. This was done by etching 2.5µm deep trenches into the silicon substrate wafer around the perimeter of 10µm x 10µm silicon pillars.

After pillar creation the wafers were implanted with phosphorus, at 2e13cm^{-2}, 160keV and 4e12cm^{-2} , 70keV. This dopant was activated by RTP at 1100C for 10s.

Silicon germanium layers were then grown on top of these pillars by undoped solid source MBE. The layer structure started with a 1µm thick linearly graded buffer layer, graded between 0% and 30% Ge. On top of this layer a 250nm relaxed 30%Ge SiGe buffer layer was

grown, followed by a 5nm 70% Ge SiGe channel and a 2nm 30% Ge SiGe cap. The layer structure was completed with a Si cap, some of which was consumed during gate oxidation. The final thickness of this silicon cap was 2nm. A diagram of the finished layer structure is shown in figure 2.

After MBE layer growth the trenches around the pillars were filled by deposition of 100nm of low temperature oxide (LTO) silicon dioxide and 900nm of polysilicon. Polysilicon was used as, unlike LTO, it filled the trenches with out leaving voids. The polysilicon was removed from the top of the pillars by dry etch and a 500nm layer of LTO was deposited on the wafer to form the field oxide. Active area windows were wet etched in this oxide to expose the tops of the pillars so that devices could be fabricated on top of the pillars.

The gate oxide was grown in dry oxygen and was 5nm thick. The polysilicon gate electrode was 200nm thick and insitu doped with boron. Gates were defined by e-beam lithography. Source/ drain extension implants were made with 1e14cm^{-2}, 33keV BF_2 implant. Sidewall spacers were made of LTO, and the HDD implanted with of 5e15cm^{-2}, 45keV BF_2. Implants were activated by anneal at 800C for 30 minutes. Devices were completed with a conventional back end of BPSG ILD and Ti/Al metallisation.

A cross sectional TEM picture of a completed device like structure is shown in figure 3, and a picture of a trench structure shown in figure 4.

Conventional silicon reference devices were also fabricated with a substrate consisting of a MBE grown layer of undoped silicon grown on top of pillars.

3. Electrical Results

DC characterisation of the devices was made with a HP4155 Semiconductor Parameter Analyser.

The threshold voltage (V_t) for 2μm SiGe devices is +0.38V, compared to 0.05V for the silicon device. This change in threshold voltage is caused by valance band offset of the silicon germanium buried channel.

Gate Voltage vs. Drain Current curves for the same 2μm devices are shown in figure 5. The gate voltage for this graph ranges from the threshold voltage to -2.5V+V_t. The drain current for a 2μm silicon germanium device at Vd=-2.5V and Vg=-2.5V+V_t is -114μA/μm width. This is 40% higher than the -69μA/μm width measured for the conventional silicon device.

Vg vs. Id curves are shown in figure 6. From these curves transconductance and effective mobility can be extracted [8]. The effective mobility as a function of gate voltage is shown in figure 7 and the transconductance shown in figure 8.

The maximum hole effective mobility of the silicon germanium devices is 156cm^{2}V^{-1}s^{-1}, which is 39% higher than the maximum mobility of the silicon reference device of 94.6 cm^{2}V^{-1}s^{-1}.

Transconductance was measured at a drain voltage of -100mV. The maximum transconductance was 5.40μS/μm for the SiGe devices and 3.26μS/μm for the silicon reference device.

4. Discussion

The new SiGe devices show a considerable improvement in current drive, transconductance and effective mobility over their conventional counterparts.

The improvement in maximum effective hole mobility and transconductance of these new devices is due to the presence of the high germanium content SiGe buried layer.

The improvement in drain current of the new devices may also be due to this layer or the formation of a parasitic channel in the silicon cap layer. Current drive improvements in strained silicon layers formed on SiGe virtual substrates have been shown by a number of authors [1-5].

5. Conclusion

SiGe MOSFETs have been presented grown on novel SiGe virtual substrates.

The silicon germanium virtual substrate is grown on top of 10µm x 10µm pillars which promotes the relaxation of the virtual substrate and reduces cross hatch.

A 70% germanium strained channel has been grown on top of this substrate.

Device characteristics show a 40% increase in device drive current compared to silicon counterparts. An improvement in channel carrier mobility and device transconductance which has been attributed to the presence of the high germanium (70%) content SiGe channel.

6. References

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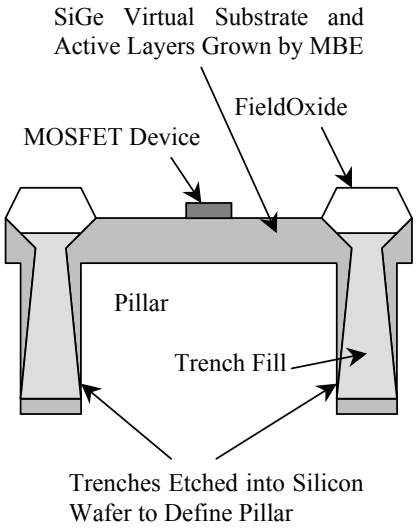

Figure 1, Cross setional diagram of a silicon pillar with SiGe MBE layer grown on top of it. The SiGe material also grows inside the trench structure.

2nm Si Cap
2nm 30%Ge SiGe Cap
5nm 70%Ge SiGe Channel
250nm 30%Ge SiGe buffer Layer
1um 0% to 30%Ge SiGe Graded Buffer Layer
Si Substrate

Figure 2, Device layer structure.

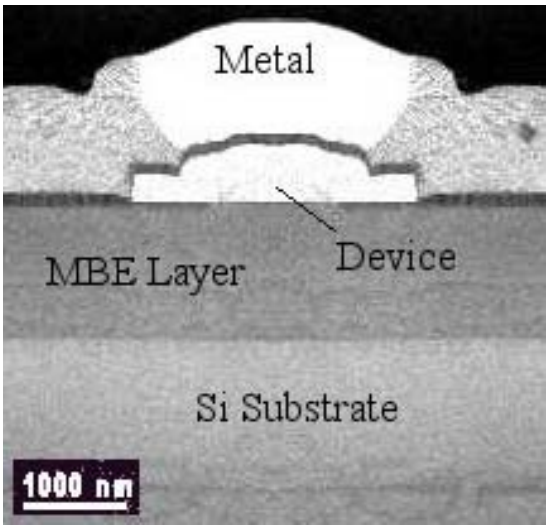

Figure 3, Cross sectional TEM picture of a pMOSFET device fabricated on top of SiGe grown MBE layers.

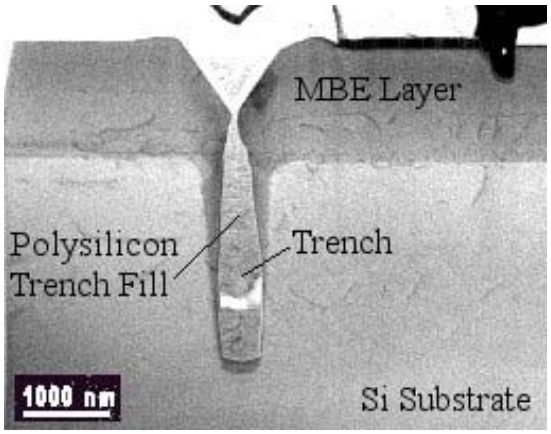

Figure 4, Cross sectional TEM picture od a trench structure used to define the edges of the silicon pillars.

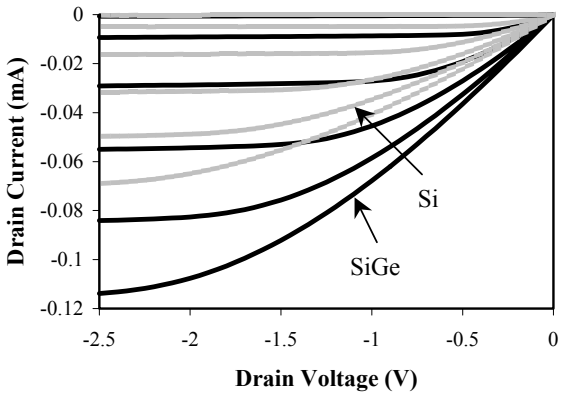

Figure 5, Drain voltage vs, drain current curves for Si and SiGe devices. curves are measured at Vg=Vt to Vt-2.5V for both devices. L=2 micron. Data normalised to a device width of 1 micron.

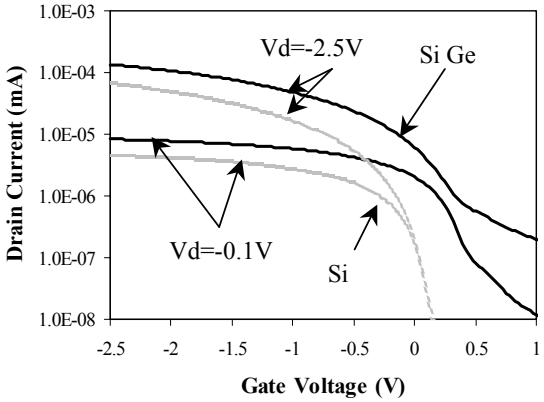

Figure 6, Gate voltage vs. drain current curves of SiGe and Si devices. Curves are measured at Vd=-0.1V and Vd=-2.5V. L=2 micron. Data normaised to a device width of 1 micron.

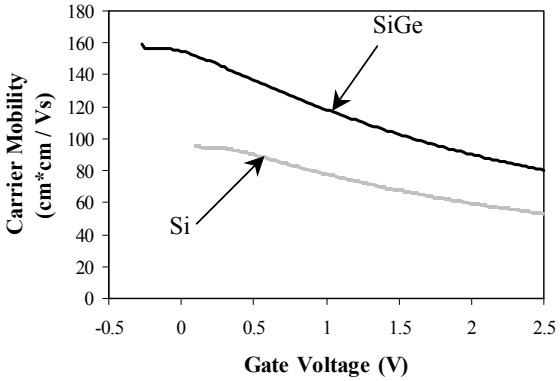

Figure 7, Effective mobility measured at Vd=-0.1V. L=2 micron. Data normaised to a device width of 1 micron.

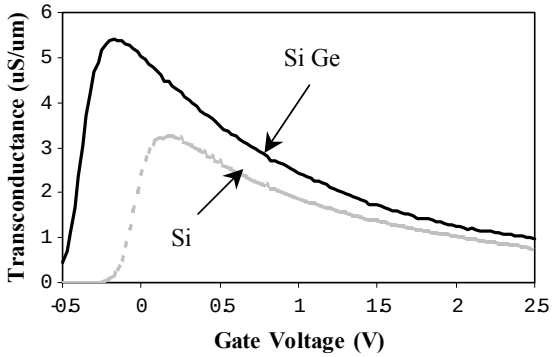

Figure 8, Device transconductance at Vd=-0.1V. L=2 micron. Data normaised to a device width of 1 micron.