Ultra-Thin Oxide Lifetime Estimation Using Transistor Degradation

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Abstract

Degradation of ultra-thin (17Å) oxide transistor parameters under gate stress (both accumulation and inversion) is investigated as an alternative to traditional capacitor stress for 0.1 mm technology. PMOSFET parameters degrade at a faster rate than NMOSFET, indicating that the lifetime will be dictated by PMOSFET. The predicted lifetime using device parameters is smaller than that from the oxide breakdown test.

1. Introduction

Reliability issues in ultra-thin (< 2 nm) dielectrics are of extreme importance for the 0.1 μm node and below. Traditional methods of estimating QBD and TDDB fail to yield useful results since they report lifetimes in excess of 10^7 years [1]. In addition, the definition of oxide breakdown (soft and hard) and methods of detecting it in ultra-thin oxide are attracting some attention [2,3,4]. Considerable studies have been done in locating the exact location and consequences of the breakdown [5,6,7]. Henson [6] reported two distinct breakdown failure phenomena, one in the channel resulting in increased gate leakage at low gate voltages and a second in the source/drain overlap region resulting in gate leakage increase for all gate voltages. Tsai [7] also has emphasized the significance of the actual breakdown location and reported increased gate induced drain leakage (GIDL) current.

While significant attention has been paid to the breakdown phenomena, not enough study exists relating it to actual device degradation. Our study attempts to fill this gap by analyzing the degradation of transistor parameters over the stress time under a range of stress voltages for 17Å gate oxides. Understanding this data provides us with a method of predicting realistic transistor lifetime under worst case operating conditions.

2. Experiment

N and PMOSFETs were fabricated on nominally p-type (100) silicon substrates. The fabrication followed a typical CMOS flow with dual oxide growth. All oxides (targeted 17Å/62Å) were nitrided by a NO anneal step during the last oxidation step. Poly patterning, extension and S/D implants appropriate for a 0.1 μm transistor node followed this step. Oxide capacitance measurements for the thinnest oxide were performed on 30x30 μm^2 capacitors to reduce the effects of gate oxide leakage. The extracted oxide thickness is around 17Å as shown in Fig. 1. The measured oxide thickness by TEM is close to the extracted value.

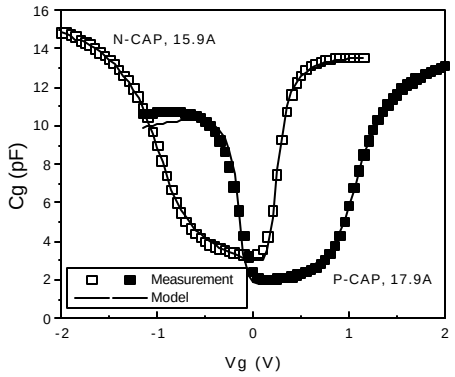

Fig 1. CV test and model extraction.

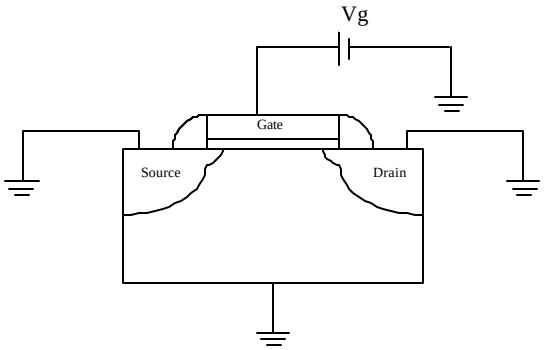

Fig 2. The setup at stress condition.

The target (W/L = 5/0.1), long channel (W/L = 5/5) transistors and capacitors (30x30 μm^2) were stressed in both accumulation (source/drain floating) and inversion (source/drain grounded) with stress voltages ranging from 2.9 V to 3.6 V. At each stress voltage, target devices were stressed in logarithmically increasing time steps up to 6000 seconds. The setup of the stress condition is shown in Fig. 2. The transistor gate, drain, source and substrate characteristics were recorded after each time interval to find the leakage path. All tests were carried out at room temperature. The transistors under test share both gate and well pads with other transistors on the same pad group. By monitoring the gate current at

operating voltage (±1V), the breakdown of gate dielectric can be evaluated.

3. Results and Discussion

During stress, the threshold voltage (V_T), transconductance (G_M), linear drain current ($I_{D,LIN}$), saturation drain current ($I_{D,SAT}$), and subthreshold slope were all monitored. The subthreshold slope shows less degradation compared with other parameters. The degradation of G_M, $I_{D,LIN}$ and $I_{D,SAT}$ track each other. V_T and $I_{D,SAT}$ were selected to present the degradation. 10 mV shift of V_T or 5% $I_{D,SAT}$ degradation, whichever occurs first, was selected as the lifetime criterion.

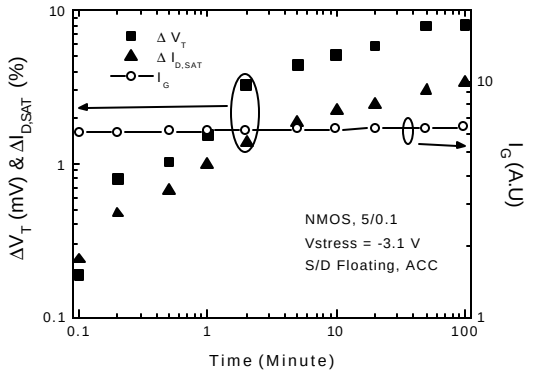

Fig 3. 5/0.1 NMOSFET parameter degradation stressed in accumulation

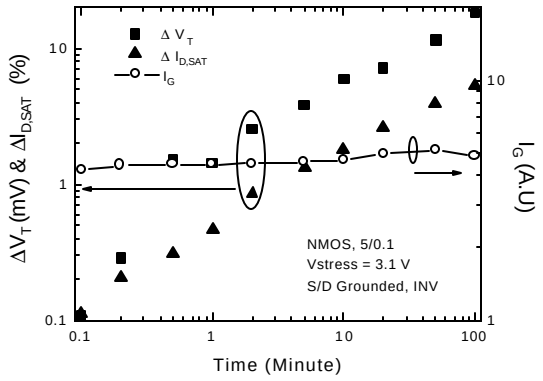

Fig 4. 5/0.1 NMOSFET parameter degradation stressed in inversion

Gate current, V_T, and $I_{D,SAT}$ degradation of 5/0.1 NMOSFET stressed in accumulation (ACC) and inversion (INV) are shown in Figs. 3 and 4, respectively. No breakdown is observed at this voltage during stress.

V_T and $I_{D,SAT}$ degradation slopes decrease with increasing stress time, similar to the hot carrier degradation [8]. At the beginning stage, the degradation slope is around 0.6; while in the long run, the slope changes to 0.2, as shown in Fig. 5. For NMOSFETs, lifetime is smaller based on 5% $I_{D,SAT}$ degradation. The lifetime under accumulation stress is much smaller than that under inversion stress, as shown in Fig 6.

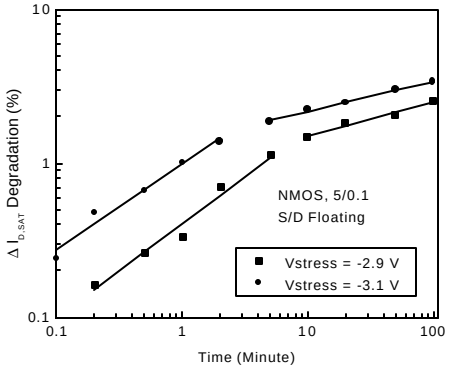

Fig 5. 5/0.1 NMOSFET parameter degradation shows two-stage slope.

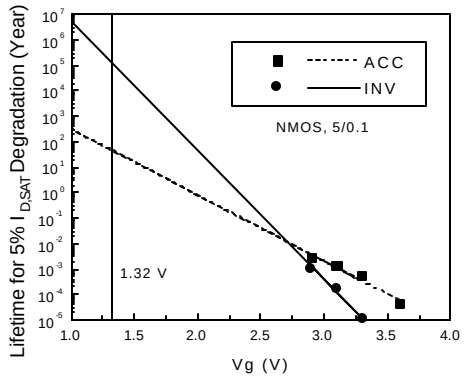

Fig 6. 5/0.1 NMOSFET Lifetime data

Gate current, V_T, and $I_{D,SAT}$ degradation of 5/5 NMOSFETs stressed in inversion are shown in Fig. 7, with only soft breakdown observed. Similar to the short channel devices, the degradation slope becomes smaller with extended stress time and the breakdown is between gate and source/drain. Similar rates of degradation are observed for accumulation and inversion cases as shown in Fig. 8.

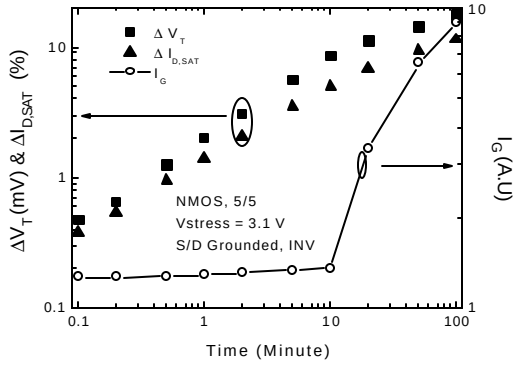

Fig 7. 5/5 NMOSFET parameter degradation stressed in inversion

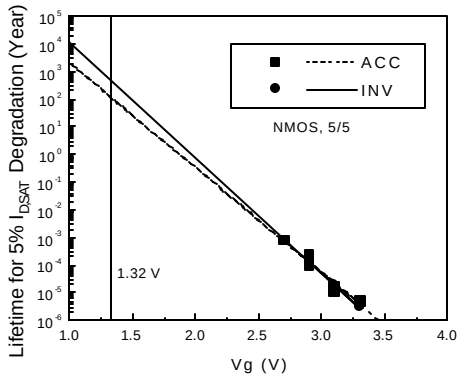

Fig 8. 5/5 NMOSFET Lifetime data

For all NMOSFETs tested, the degradation is worse under accumulation than inversion at the worst case operating voltage. Under inversion stress, the degradation is mainly at the source/drain edge. Experiments conducted under inversion stress with source/drain floating exhibited no degradation.

In case of 5/0.1 PMOSFETs, V_T and $I_{D,SAT}$ degradation is much faster than that of NMOSFETs, as shown in Figs. 9 and 10, consistent with the recent reports on nitrided oxide [9]. Under accumulation stress, hard breakdown is observed; while no breakdown was observed for stress in inversion case. In case at hard breakdown, the leakage path is between gate and substrate.

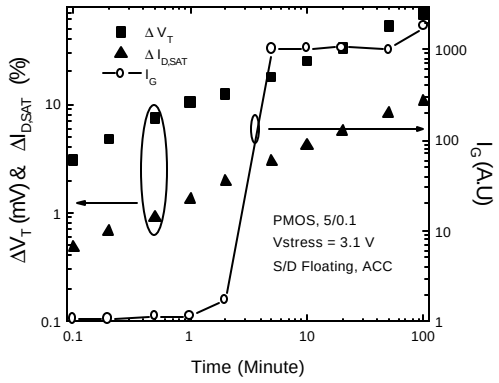

Fig 9. 5/0.1 PMOSFET parameter degradation stressed in accumulation.

For 5/5 PMOSFETs, no breakdown was observed in inversion case and soft breakdown was observed in accumulation case as shown in Figs 11 and 12. The leakage path for soft breakdown is between gate and substrate.

10 mV V_T shift is the lifetime criterion for PMOSFETs because V_T degrades much faster than $I_{D,SAT}$. Similar amounts of degradation are observed under accumulation and inversion stress, as shown in Figs. 13 and 14.

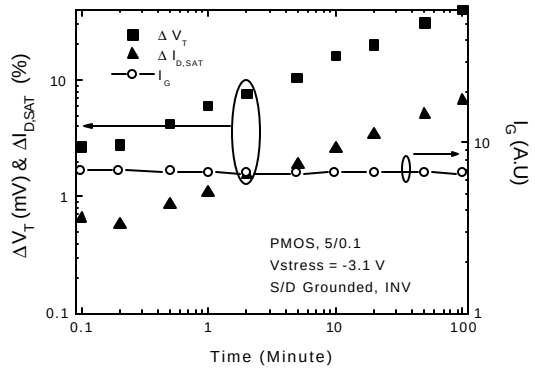

Fig 10. 5/0.1 PMOSFET parameter degradation stressed in inversion.

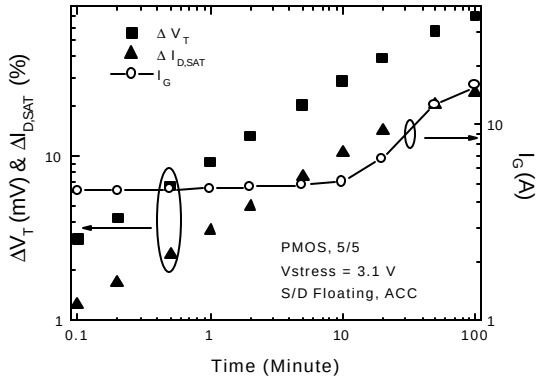

Fig 11. 5/5 PMOSFET parameter degradation stressed in accumulation.

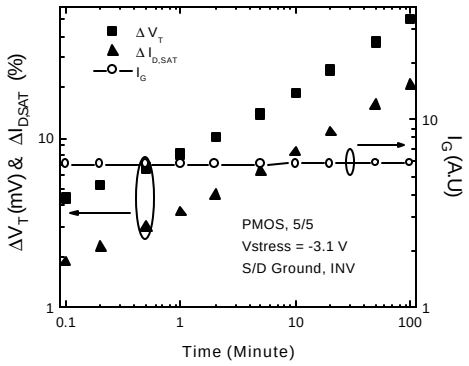

Fig 12. 5/5 PMOSFET parameter degradation stressed in inversion.

For PMOSFET under inversion stress, the degradation is mainly at the source/drain edge. Experiments conducted under inversion stress with floating source/drain exhibited no degradation.

The ramped voltage tests on 100X100 μm^2 capacitors show that the capacitors do not breakdown even up to 4V, indicating that traditional oxide lifetime estimation methods would predict much higher value than the parameter degradation.

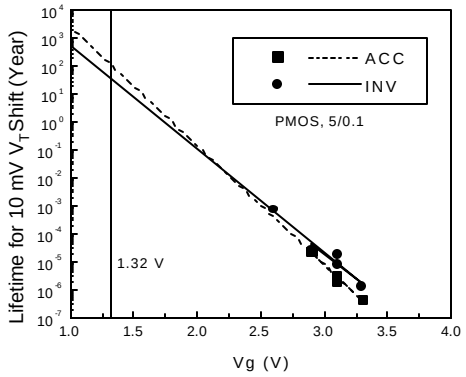

Fig 13. 5/0.1 PMOSFET Lifetime data

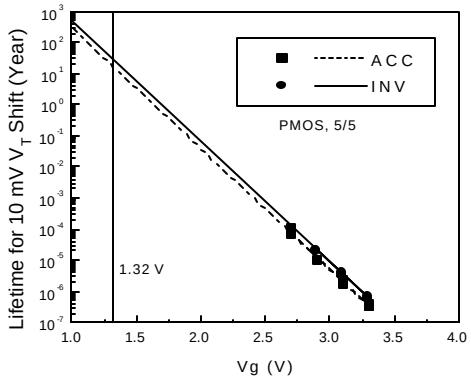

Fig 14. 5/5 PMOSFET Lifetime data.

The CV measurements before and after stress on 30x30 μm^2 capacitors are shown in Figs. 15 and 16 for NCAP and PCAP, respectively. The flat band shift is more severe on PCAP than on NCAP. For NCAP, the flat band shift is worse in inversion; while for PCAP, the flat band shift is more severe at accumulation, consistent with the transistor data.

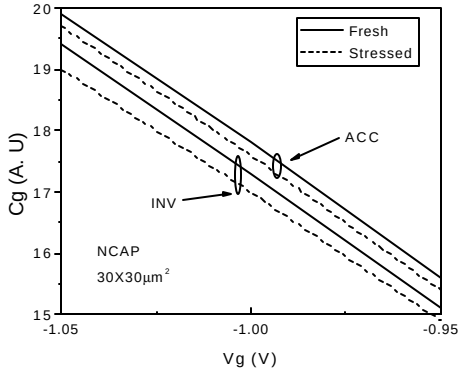

Fig 15. NCAP CV measurement before and after stress.

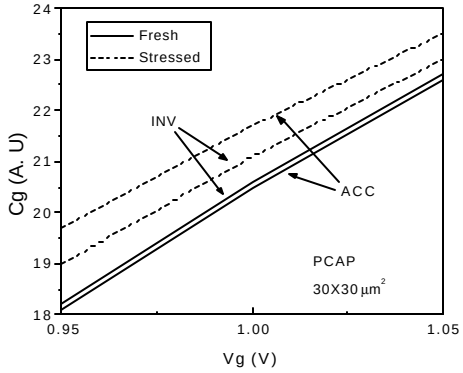

Fig 16. PCAP CV measurement before and after stress.

Transistors on the 0.1 μm node are expected to be 1.2 V tolerant and the lifetime for PMOSFETs under 1.32 V operation shown in Figs. 13 and 14 is 50 and 20 years, respectively, as compared to 10^7 years predicted by traditional methods. It should be noted here that these stress tests were conducted at room temperature and a complete understanding will be obtained when the tests are repeated at 125°C, which leads to a faster degradation [10]. This can put a limit on PMOSFET operation for 0.1 μm technology.

4. Conclusions

Degradation of ultra-thin (17Å) oxide transistor parameters under gate stress was examined in detail. Gate breakdown in transistors is mainly between gate and source/drain for NMOSFETs and between gate and substrate for PMOSFETs. Device characteristics show two-stage degradation under extended stress. For NMOSFETs, $I_{D,SAT}$ degrades faster while V_T shift is worse for PMOSFETs. Even without oxide breakdown, PMOSFETs show strong V_T degradation, which might put a limit on reliability of 0.1 μm devices. The predicted lifetime using device parameters is smaller than that from the oxide breakdown test.

5. References

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