Gate Material Properties Induced 0.25 µm SRAM Marginality

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Abstract

A new failure mechanism was studied on high density and high performances 0.25µm SRAM memories. A local anomalous polysilicon grain growth, promoted by a Phosphorus gate predoped implantation, induced a modification of dopant diffusion into N-doped transistor gate. This local variation of small transistor threshold voltage, was responsible for a severe yield loss in large SRAM memory array. This phenomenon was both related to gate material properties and gate predoped implantation conditions. This paper presents a complete characterization of this new failure mechanism, based on physical and electrical measurements. Finally, main results of process experiments, performed to solve the problem, are discussed.

1. Introduction

A large number of applications are now requiring CMOS products with large embedded SRAM memories. High density and high performances SRAM are very sensitive to process fluctuations, depending also on cell design robustness. In particular, gate doping and small transistor threshold voltage control are becoming very critical for sub-quarter micron technologies [1],[2]. In this paper, a new failure mechansim, responsible for a severe 0.25µm CMOS HD-SRAM yield loss, is studied. After a brief description of the electrical signature of phenomenon, a detailed characterization of the failure mechanism, based on both in-line and off-line physical analysis is presented. In particular, the key role of gate amorphous silicon properties, and phosphorous predoped implantation conditions are described. Finally, different ways for process optimization are discussed, with electrical results obtained on a large HDSRAM memory array.

2. Problem description and characterization

A severe yield loss was observed when a 0.25µm CMOS logic product, with 512 kbits of embedded HDSRAM, was transferred from one ST production plant to another. The HDSRAM design is a classical 6T transistors cell, with mirror design between two adjacent rows of the array, thus generating odd and even rows of cells. The main yield loss was localized in HDSRAM part of product, with about 1 cell failed per 100.000 cells. An electrical bitmap analysis has shown that main part of bit fails are single bit fail, which are localized on odd rows (> 80%), showing a clear row parity effect, not explained by process defectivity or photo misalignement issue. First, such a row parity effect was related to a local modification of polysilicon gate surface, observed with SEM in-line observations,

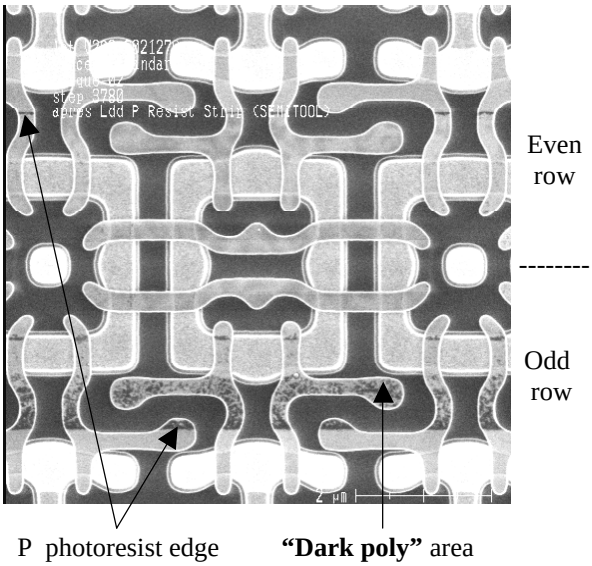

Fig.1: SEM top-view observation of HDSRAM array, just after PLDD implant: a "dark poly" area is observed only on odd rows (where electrical bit fails are localized), limited by the edge of the Phosphorous pre-doping implant photoresist.

only at very low electron beam voltage (<0.8 keV). The dependence to the electron beam voltage is probably related to the fact that polysilicon film modification is very superficial. This parity modification of the surface of polysilicon gates was evidenced only after the

amorphous silicon crystallization step, performed during furnace gate reoxidation process, just after gate definition. As illustrated in figure 1, odd rows exhibit a "dark poly" aspect, while even rows show a normal bright poly aspect. Dark poly area is limited by the edge of the Phosphorous pre-doping implant photoresist, performed prior to gate definition (just after silicon amorphous film gate deposition), in order to avoid gate depletion of N-doped transistors. The electrical parity of bit fail corresponds to the morphological parity of "dark poly" areas. Moreover, a top-view TEM analysis has been done on a single bit fail, after electrical bitmapping localization and wafer deprocessing (Fig.2). TEM results show the existence of a large C_{54} $TiSi_2$ single grain in the $TiSi_2$/poly stack of one NMOS transistor of the failing cell, while other transistors have normal grain size. This result tends to confirm that electrical failure mechanism is related to the modification of polysilicon surface properties on top of N-doped transistor regions. However, it is difficult to conclude about the real polysilicon grain size, situated just below the large salicide grain.

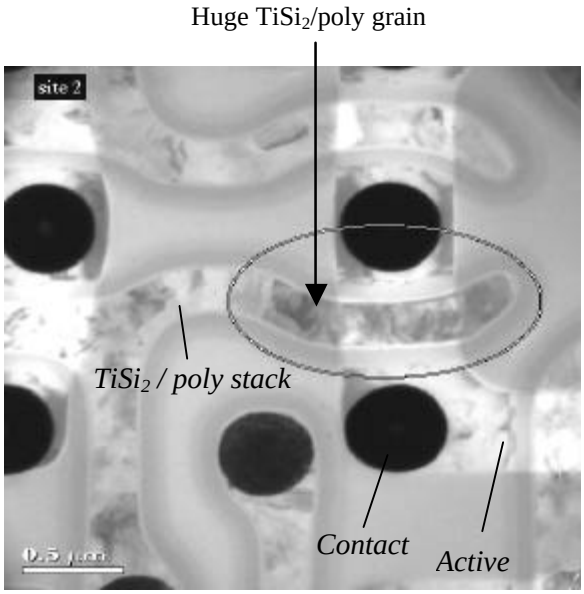

Fig.2: TEM top-view of HDSRAM single bit fail cell (after deprocessing): huge grain of $TiSi_2$/poly observed on top of inverter NMOS gate.

3. Mechanism description

It has been clearly demonstrated that failure mechanism is based on a row parity effect, related to a local modification of gate polysilicon surface properties ("dark poly"), limited by the Phosphorous predoping implant photoresist edge. This high dose 4.10^{15} at/cm^2 implant is performed with a +7° tilt, creating an asymmetry between even and odd rows. Figure 3 illustrates in cross section the impact of the P predoping implant on the odd row (row fail): the +7° tilted implant reacts with the sidewall of the photoresist, leading to a local modification of the amorphous silicon surface, near the photoresist edge.

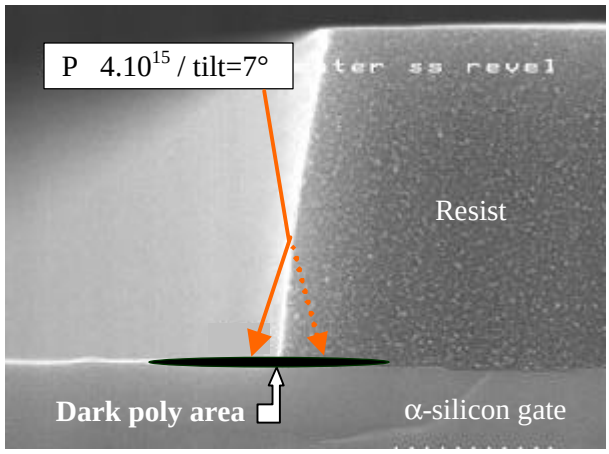

Fig.3: SEM cross section of predoping implant photoresist (on top of α-Si gate), with schematic of +7° tilt Phosphorous ion beam implantation.

In order to characterize this local modification of the amorphous silicon surface, near the photoresist edge, Auger analysis was performed in a scanning AES equipment (Fig.4). A Phosphorus peak was evidenced near photoresist edge, in the dark poly region, while it was absent in the bright poly region. This indicates an excess of Phosphorous dopant on top of dark poly gates, in a very superficial layer of about 20Å.

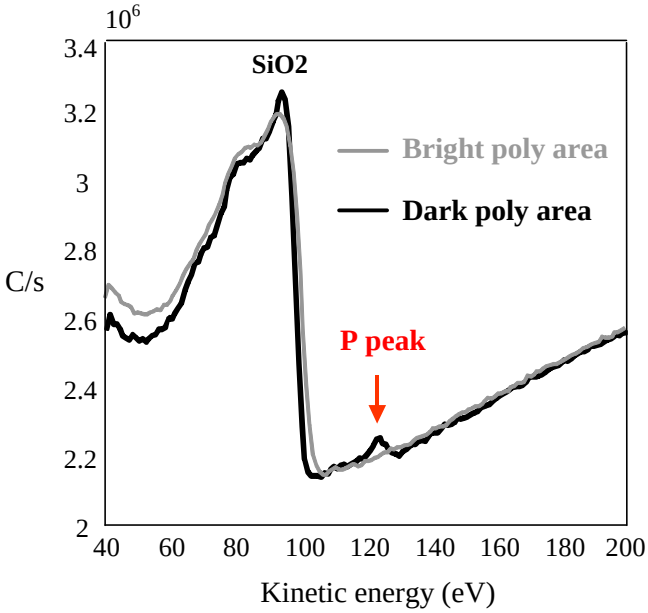

Fig.4: AES spectra on top of bright & dark poly areas. An excess of Phosphorous is evidenced only on top of dark poly gates.

To verify the parity hypothesis, it has been confirmed that changing the predoping implant tilt from +7° to –7°, the localization of electrical single bit fail was changing from odd to even rows. This is due to the fact that changing the implant tilt, the ion beam is reacting with the opposite sidewall of the resist. Notice that quad mode implant (with four rotation) was also tried and led to a symmetrical bit fail pattern, but total fail number was not significantly decreased. Moreover, a comparison of different types of implant equipments has shown equivalent results. Even if the Phosphorous implant was clearly involved in the failure mechanism, another parameter was playing a key role: amorphous silicon gate material. A comparison between different types of LPCVD furnace was performed. The main difference between furnaces was the content of oxygen present in the boat (leakage), and the presence or not of a load/lock system. Figure 5 presents SIMS profiles of oxygen in amorphous silicon film, for two different LPCVD furnaces: furnace A without load/lock and furnace B with load/lock system and lower leakage. It was evidenced that furnace B induced about 1 decade lower O_2 concentration in as-deposited amorphous silicon film, than furnace A.

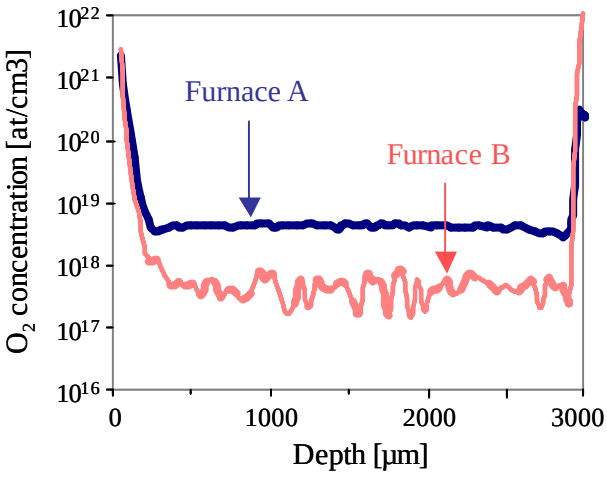

Fig.5: Oxygen SIMS profile in 3000Å amorphous silicon film, for two different LPCVD furnaces: O_2 concentration is one decade lower in furnace B, with load/lock system and lower leakage.

As a result, the polysilicon resistivity obtained at the end of the process, after implants and thermal treatments, was lower in furnace B than in furnace A (Fig.6). This is related to the key role of oxygen, acting as a polysilicon grain growth limiter [3],[4]: the polysilicon grain size is larger in furnace B, due to a lower O_2 concentration contained in α-Si film after deposition. From an electrical point of view, furnace B gave worse results, with a very high level of HDSRAM single bit rejects (Fig.6). The larger the gate polysilicon grain size, the higher the dispersion of transistor threshold voltage in memory array. This is due to the very low number of grain boundaries available on the gate active part of small transistor embedded in HDSRAM cell. It is reported that for sub-quarter micron technologies, a better transistor threshold voltage stability is obtained by using a small grain size polysilicon film as gate material [2]. As a consequence, electrical results obtained with furnace A was significantly better than furnace B, with a percentage of bit fail reject lower than 15%.

In conclusion, the complete failure mechanism proposed is the following: the local Phosphorus over-concentration, evidenced at the surface of “dark poly” areas, tends to lower the crystallization temperature and to promote the quick growth of large polysilicon grains [4], or more probably the appearance of large grains by the secondary grain growth mechanism described by R. Plugaru et al. [5]. This phenomenon is also strongly dependent on the content of oxygen present in the as-deposited amorphous silicon film. The lower the content of oxygen, the larger the polysilicon grain size formed, during thermal treatments following amorphous silicon deposition. The presence of large poly grain size in memory array is responsible for a non uniform dopant diffusion into gate material, resulting in dispersion of small transistor threshold voltage. Depending on SRAM design robustness, this dispersion can locally lead to memory fail during cell read operation. Notice that another possible mechanism can be related to the modification of small transistor threshold voltage, due to large grain $TiSi_2$/poly film stress. A similar mechanism has been reported recently by S. Sito et al. [6].

4. Process optimization

Three possible ways have been investigated to get rid of the problem. Trials on Phosphorus implant conditions have been performed, especially on tilt and dose implant. Changing the dose from +/- 25% or ion beam current by a factor 5 was not able to recover the problem. New trials with different LPCVD furnaces have been done. Figure 6 shows HDSRAM yield results has a function of 4 different furnaces. It was confirmed that, the higher the content of oxygen in the furnace, the higher the polysilicon resistivity and lower the HDSRAM yield loss. A harware modification of B type furnace was envisaged, in order to introduce a low well-controlled amount of Oxygen. Unfortunately, despite successful trials [3], it is difficult to introduce reproductably a few parts per million of oxygen in a furnace, without increasing particle defectivity. Finally, modification of the amorphous silicon surface properties, after α-silicon deposition in B type furnace (worst case), has been studied. Because failure mechanism takes place at the extreme surface of the poly gate material, process trials with specific surface treatments have been tried. Dark poly areas have been suppressed by using surface treatments, combining cleanings and plasma oxidations, in order to modify the

status of amorphous silicon surface before the first crystallization step. The suppression of dark poly areas has been correlated to an almost complete suppression of HDSRAM yield loss (Fig.6), recovering a random defectivity limited rate of rejects, as was observed on A type furnace. This optimized process has been succesfully introduced in volume production for all 0.25µm CMOS products.

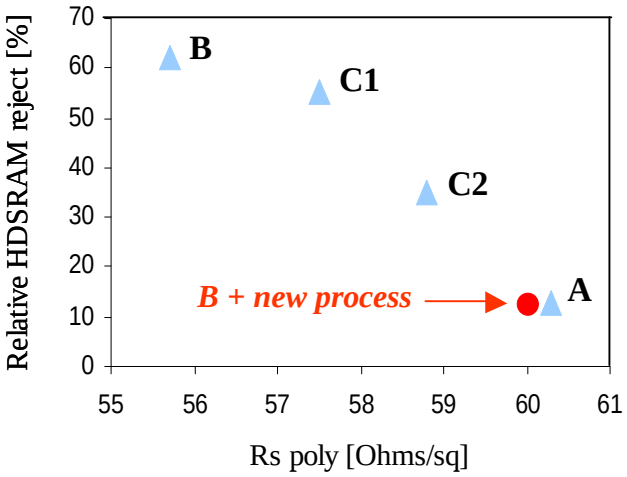

Fig.6: Relative HDSRAM yield loss as a function of polysilicon resistance, for different LPCVD furnaces A, B, C1, C2. New optimized process (●) with furnace B gives equivalent results than furnace A.

5. Conclusion

A new failure mechanism was studied on high density and high performances 0.25µm SRAM memories. It has been demonstrated that a local anomalous polysilicon grain growth, promoted by a Phosphorus gate predoped implantation, can induce a local modification of dopant diffusion into N-doped transistor gate. This local variation of small transistor threshold voltage, was responsible for a severe yield loss in large SRAM memory array. It has been demonstrated that this phenomenon was both related to amorphous silicon gate material properties and gate predoped implantation conditions.

An adequat process optimization, based on amorphous silicon surface treatments, has been developed and implemented in volume production. This process was able to completely suppress the "dark poly" phenomenon, while recovering a random defectivity limited yield on large HDSRAM memories. Crystallisation-based mechanisms in CMOS polysilicon gates are very complex and for the future, with the continuous shrink of gate dimension, it will become even more severe. Controlling grain size in polysilicon and salicides will thus remain a strong preoccupation. In parallel, design improvement must be continued to get more robust HDSRAM cell to process parameters variation.

Acknowledgments.

The authors wish to thank ST Rousset Physical Analysis Laboratory team for in depth characterization, and ST Agrate R&D Physical Analysis Laboratory for Auger measurements.
Many thanks also to ST Crolles team and in particular to B. Garcin and M. Varrot for helpful technical discussions.

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