

# Impact of Statistical Threshold Voltage Fluctuations and Quantum Mechanical Effects on CMOS Circuits with Gigabit Feature Size

Stefan Schwantes and Wolfgang Krautschneider  
 Technical University of Hamburg-Harburg  
 Eissendorfer Strasse 38, 21071 Hamburg, Germany  
 Schwantes@tu-harburg.de

## Abstract

We have investigated the impact of statistical threshold voltage fluctuations on the functionality of digital CMOS circuits in the nanometer region. An analytical model considering short channel and quantum mechanical effects is presented that shows good agreement with two-dimensional device simulations for feature sizes below 100 nm.

It is found that a minimum equivalent oxide thickness is required for reliable operation of digital CMOS circuits with gigabit feature sizes and that planar CMOS technologies below a feature size of 25 nm may be replaced by fully-depleted technologies which show a less threshold voltage variations.

## 1. Introduction

The threshold voltage ( $V_{TH}$ ) variation due to statistical impurity fluctuations in the channel region is one of the most serious problems in scaled MOSFETs [1], because the  $V_{TH}$  fluctuations significantly increase as the device is scaled down.

In this work we investigated the impact of the threshold voltage fluctuations on the functionality of digital CMOS circuits with 10 nm to 100 nm feature size. We performed two-dimensional device simulations with ATLAS [2] utilizing the coupled Schrodinger-Poisson equation to obtain the threshold voltage fluctuations. An analytical model was developed to explain the results of the device simulations and to replaced the time intensive simulations. Optimized BSIM3 parameters were used for the SPICE simulations of digital CMOS circuits. The SPICE parameters were obtained by device simulation with ATLAS.

## 2. Modelling the threshold voltage fluctuations

To suppress short channel effects retrograde and super-halo doping profiles are necessary [3]. An simple analytical model for the standard deviation of the threshold voltage of MOSFETs with retrograde profile was developed in [1].

$$\sigma V_{TH} = \left( \frac{q}{C_{OX}} \right) \sqrt{N_{EFF} W_{DEP} / WL} \quad (1)$$

$W_{DEP}$  denotes the depletion width and  $W$  and  $L$  the MOSFET channel width and length respectively.  $N_{EFF}$  is the effective channel doping. By integrating  $N_{EFF}$  over the whole channel region, halo profiles can be also described by equation 1.

Table 1. Technology parameters for Fig. 1 and 3

Feature Size	100 nm	50 nm	25 nm	10 nm
Gate oxide	2 nm	1.5 nm	1.2 nm	1 nm

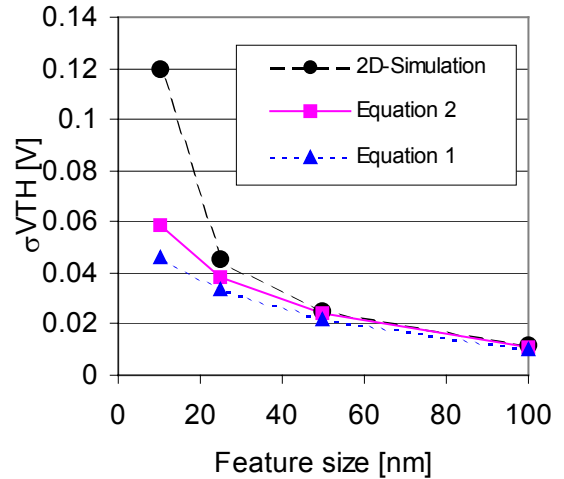


Figure 1. Comparison of Equation 1 and 2 with two-dimensional device simulations utilising the coupled Poisson-Schrodinger equation. Channel width is two times the channel length.

The increasing relevance of the space charge region in the vicinity of the drain junction due to shrinking of the channel length can be described by the charge sharing model [4]. For short channel transistors the  $V_{TH}$  mismatch becomes:

$$\sigma_{VTH\_SCE} = \sigma_{VTH} \frac{1 - \frac{C_1}{L}}{\sqrt{1 - \frac{f_{CS}}{L}}} \quad (2)$$

with

$$C_1 = f_{CS} - \frac{W_{DEP} R_j}{f_{CS} + R_j},$$

$$f_{CS} = R_j \left( \sqrt{1 + \frac{2W_{DEP}}{R_j}} - 1 \right)$$

$R_j$  is the junction depth

A comparisons for feature sizes of 10 nm to 100 nm of eq. 1 and eq. 2 with two-dimensional device simulations utilising the coupled Poisson-Schrodinger equation is shown in Fig. 1. The appropriate technology parameters can be found in Table 1. We used silicon dioxide as a gate material because an alternative dielectric with a sufficient degree of maturity is not available so far. This results in an oxide thickness exceeding the ITRS Roadmap data by a factor of two.

A good agreement between the numerical simulation and eq. 2 can be seen in Fig. 1 up to the 50 nm generation. For smaller feature sizes an increasing mismatch occurs, as quantum mechanical effects have to be taken into account.

As can be seen in equation 1 the threshold voltage deviation depends strongly on the electrical oxide thickness. Due to the high electric fields at small effective oxide thicknesses two parasitic effects, the poly depletion effect and the quantum mechanical carrier shift, will increase the electrical oxide thickness as can be seen in Fig. 2.

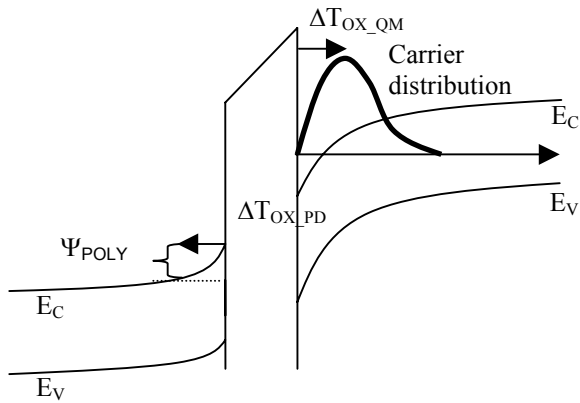


Figure 2. Schematic of the electrical oxide thickness increase due to poly depletion and quantum mechanical carrier distribution

The quantum mechanical effect adds  $\Delta T_{OX\_QM} = (\epsilon_{OX}/\epsilon_{SI})(x_{average}^{QM} - x_{average}^{CLASSIC})$  or about 0.3 to 0.4 nm to the gate oxide [5].

$x_{average}^{QM}$  can be described as [5]:

$$x_{average}^{QM} = \left( \frac{9h^2 \epsilon_{SI}}{16qQ^S m_e \pi^2} \right)^{\frac{1}{3}} \quad (3)$$

where  $m_e$  is the electron effective mass and

$Q^S = Q_{DEP} + \frac{11}{32} Q_i$  is a combination of the depletion

and inversion charge per unit area in the channel. Both can be obtained from the classical MOS-physics. A further increase of the electrical oxide thickness by 0.2 nm is observed due to the poly depletion effect (Fig. 3) and can be described by [6]:

$$\Delta T_{OX\_PD} = \sqrt{\frac{8kT}{q^2 N_{POLY} \epsilon_{SI}}} \quad (4)$$

with  $N_{POLY}$  being the polysilicon dopant concentration.

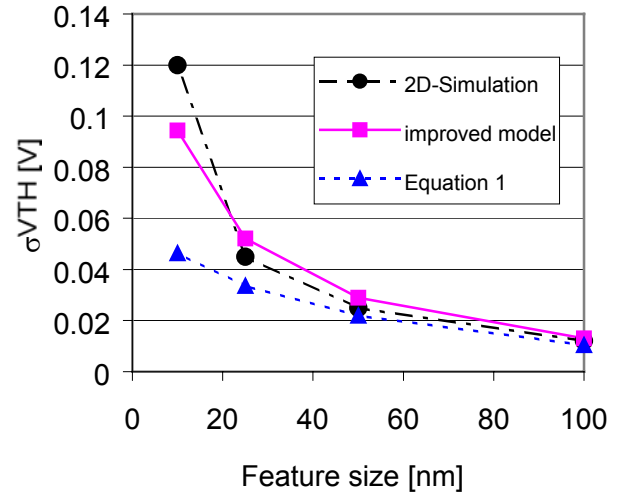


Figure 3. Comparison of eqs. 1 and 2 with two-dimensional device simulation utilising the coupled Poisson-Schrodinger equation.

As can be seen in Fig. 3, adding the polydepletion effect and the quantum mechanical carrier shift to eq. 2 results in an accurate prediction of the standard threshold voltage deviation.

### 3. Circuit simulation

Scaling down the minimum feature size causes an significant increase of the threshold voltage fluctuations (fig. 3). One possibility to decrease the  $V_{TH}$  fluctuations is reduction of the equivalent gate oxide thickness. By assuming the equivalent oxide thickness predicted by the ITRS roadmap [7] a reduction of the threshold voltage fluctuations can be achieved (Fig. 4). The corresponding technology parameters are shown in Table 2.

Table 2. Technology parameters according to the ITRS Roadmap

Feature Size	100 nm	50 nm	25 nm	10 nm
Gate oxide	1.3 nm	1.0 nm	0.7 nm	0.5 nm
Supply Voltage	1.0 V	0.8 V	0.6 V	0.4 V

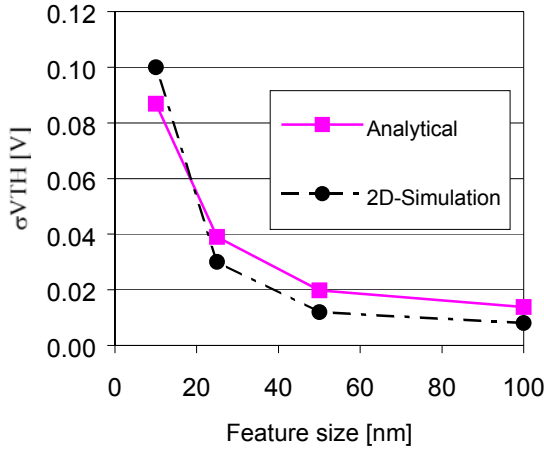


Figure 4. Standard threshold voltage deviation for reduced oxide thickness (Table 2).

For large digital circuits the  $6\sigma$  deviation must be considered due to the huge number of transistors. We started to investigate the impact of  $V_{TH}$  variation on a simple CMOS inverter. We used an inverter with electrical symmetry with a switching voltage of  $V_{DD}/2$ . Due to  $6\sigma$  deviation a shift of the switching voltage is observed. Fig. 5 plots the shift of the switching voltage versus the minimum feature size. A dramatic shift of the switching point occurs for feature sizes below 25 nm. This results in a reduced noise margin for static CMOS gates and will endanger their proper functionality.

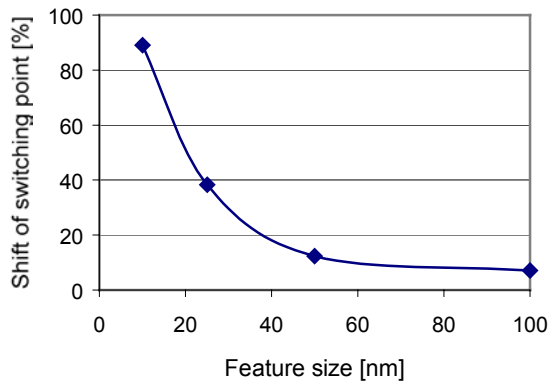


Fig 5. Shift of the switching voltage of an electrically symmetrical CMOS inverter due to the  $V_{TH}$  mismatch in percentage of  $V_{DD}/2$

We will now investigate the impact of the  $6\sigma$   $V_{TH}$  deviation on large memory systems. Fig 6. shows the schematic of a CMOS SRAM cell. We assumed a

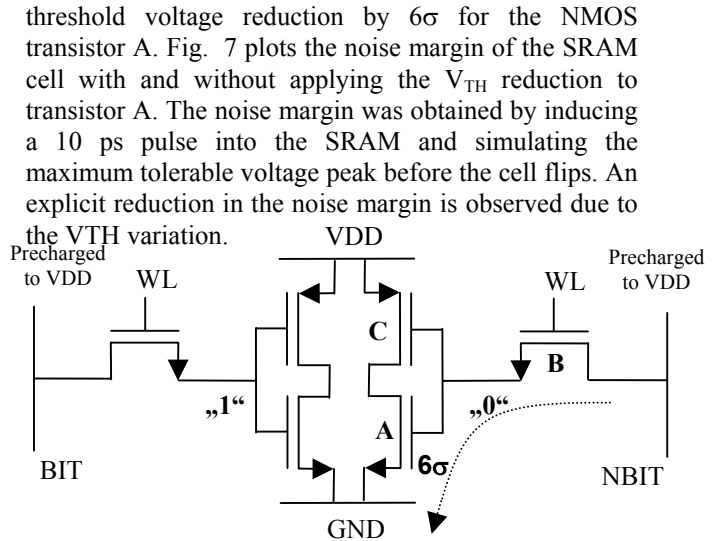


Fig 6. Schematic of a 6T-SRAM.

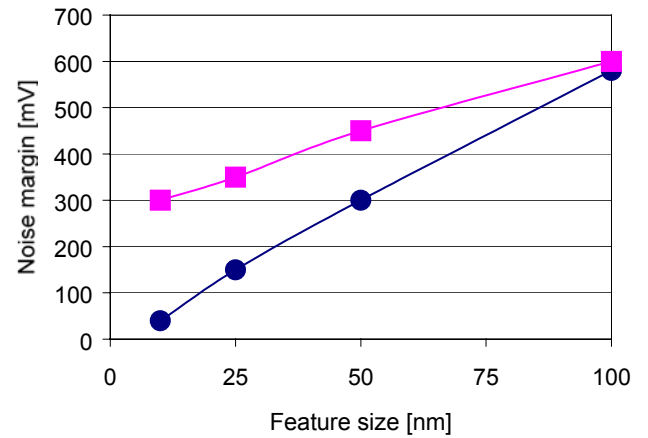


Fig. 7. Noise margin of the 6T-SRAM cell with the technology parameters from Table 2. Simulations were performed with (circles) and without (squares) the threshold voltage variations.

A further reduction of the noise margin is expected due to the read disturb [8]. During a read access of an SRAM cell, transistors A and B form a resistive divider. Together with the precharged NBIT-line this leads to a temporary increase of the "0" node. If the voltage increase at node "0" exceeds the switching point of the inverter formed by transistors A and C, then the SRAM cell will flip and the stored information will be destroyed. Fig. 8 shows the maximum peak voltage of the read disturb during a read access for different feature sizes. It scales slowly due to the reduction of the supply voltage. Fig. 8 also contains a plot of the remaining noise margin which has been reduced due to the read disturb and the  $6\sigma$   $V_{TH}$  deviation. It can be seen that the remaining noise margin approaches zero for the sub 25 nm generations. The consequence of this is that the proper functionality of the 6T-SRAM cells is no longer guaranteed for sub 25 nm CMOS generation.

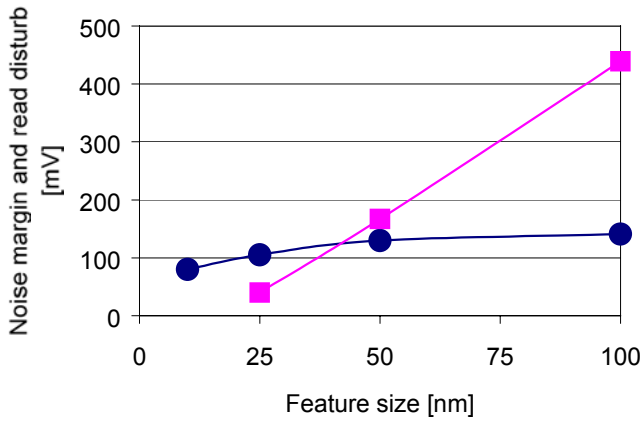


Fig. 8 Maximum voltage peak during the read disturb (circles) and reduced noise margin (squares).

We now investigate the effect of the equivalent oxide thickness on the SRAM cell stability. Fig 9 shows the standard threshold voltage variation for the 25 nm CMOS generation as a function of the equivalent gate oxide thickness. The  $V_{TH}$  variation was obtained by the two dimensional device simulator and the analytical model. It can be seen that  $V_{TH}$  scales linear with the equivalent oxide thickness.

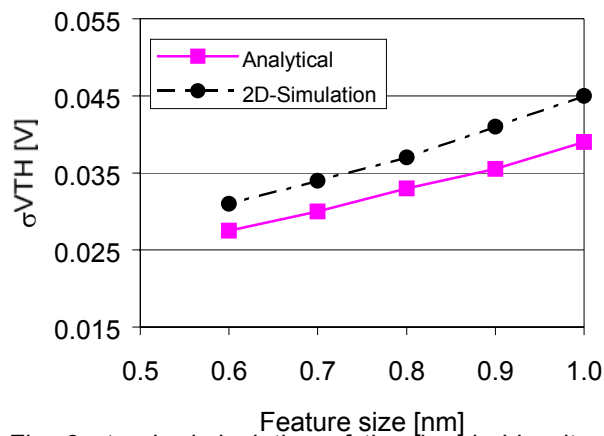


Fig. 9 standard deviation of the threshold voltage calculated by numerical simulation and the analytical model.

Table 3 gives an overview on the effect of the equivalent gate oxide thickness on the SRAM cell stability for the 25 nm CMOS generation. The first number in Table 3 is the simulated maximum read disturb peak and the second number the remaining noise margin due to the  $6\sigma$  deviation. It can be seen, that for an equivalent oxide thickness above 0.7 nm the read disturbs exceeds the noise margin and will therefore destroy the information of the SRAM cell during the read process. Due to the large threshold voltage deviation a planar 25 nm CMOS technology requires a minimum equivalent oxide thickness of 0.7 nm. Otherwise the proper functionality is no longer guaranteed

Table 3. Maximum read disturb voltage (solid) and Noise margin

VDD [V]	TOX = 0.7 nm	TOX = 0.8 nm	TOX = 0.9 nm
0.8	<b>143mV</b> / 170mV	<b>150mV</b> / 130mV	<b>152mV</b> / 110mV
0.7	<b>121mV</b> / 160mV	<b>132mV</b> / 100mV	<b>131mV</b> / 80mV
0.6	<b>102mV</b> / 150mV	<b>105mV</b> / 80mV	<b>112mV</b> / 52mV

#### 4. Conclusion

We have presented an analytical approach to describe the threshold voltage fluctuation due to statistical dopant variation in gigascale CMOS transistors.

Circuit simulations have shown, that the threshold voltage variations become a detrimental effect for large future circuits. A minimum equivalent gate oxide thickness is required for reliable operation. Using silicon dioxide as an dielectric material for gate oxide thickness' below 1 nm will endanger the proper functionality of static CMOS gates [9]. This makes the development of alternative gate dielectric materials necessary.

It is questionable if the planar CMOS technology is still usable for sub 25 nm feature size or fully depleted SOI transistor with less threshold voltage deviation [10] must be used for ultra large scale circuits.

#### References

- [1] K.Takeuchi et al. "Channel Engineering for the Reduction of Random-Voltage-Induced Threshold Voltage Variation", p. 841, IEDM 1997
- [2] [www.silvaco.com](http://www.silvaco.com)
- [3] Y.Taur, et al. "25 nm CMOS Design Considerations", IEDM 1998
- [4] R.Difrenza et al. "The Impact of Short Channel and Quantum Effects on the MOS Transistor Mismatch", p. 127, ULIS 2002, Workshop on ultimate integration of silicon
- [5] F.Stern et al., "Self-consistent results for n-type Si inversion layers", Phy. Rev. B5, p. 4891
- [6] Y.Taur and T.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 1998
- [7] ITRS Roadmap 2001, <http://public.itrs.net/>
- [8] A.J. Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuation on CMOS SRAM Cell Stability", IEEE J. Solid-State Circuits, vol. 36, p. 658, April 2001
- [9] S.Schwantes and W.Krautschneider, "Relevance of the gate current for the functionality of deep submicron CMOS circuits", p.471, ESSDERC 2001
- [10] A. Asenov et al., "Quantum Corrections in the Simulation of Decanano MOSFETs", p.111, ULIS 2002