High Hot-Carrier and ESD Immunity Device for High-Voltage I/O NMOSFETs in 0.1-μm CMOS Technology

Hyeokjae Lee, Shiang-Yang Ong, Elgin Quek, Francis Benistant, Manju Sarkar, and Sanford Chu
Technology Development Group, Chartered Semiconductor Manufacturing, Singapore738406
leehyeokjae@charteredsemi.com

Abstract

In this paper, we report the hot carrier and the ESD related device characteristics in 0.1-μm 3.3 V I/O LDD MOSFETs without hybrid (Phos. + As) typed LDD structure. In order to suggest the device guideline for the LDD and the channel doping profiles, the investigation focuses on the analysis of electrical characteristics, such as the short channel effect, the reverse short channel effect, the substrate current, the off-state leakage current, and the comparison of the electrical field with various LDD process conditions using 2-D device simulator.

1. Introduction

Modern CMOS processes are optimsed to get the maximum performance for the transistor used in digital circuits, with as boundary condition a certain lifetime. The targeted nominal lifetime is typically 5-10 years of continuous operation under specified worst-case operating conditions [1-9]. For example, minimum-length transistor operated at the nominal supply voltage will live at least the nominal lifetime. Higher stress results shorter lifetime; for MOSFET this stress usually corresponds to an electric-field strength in the device. Thus, in core devices, hot carrier effects can be relived by using reduced supply voltage whereas hot carrier reliability in input/output (I/O) devices [1-4] becomes major challenge in dual gate-oxide technology [4, 5, 7, 9].

The design and the process condition of lightly doped drain (LDD) region are important to I/O device reliability. Many device designers investigated the high hot carrier immunity and the high electrostatic discharge (ESD) immunity device structure for I/O device [1-6]. A hybrid arsenic/phosphorus (As/P) LDD structure is currently adopted for high voltage I/O MOSFETs [1, 2]. Due to the low diffusivity, arsenic is preferred in forming shallow junctions with a steep doping distribution, but is made in forming abrupt junction which increases the peak electric field in channel region and deteriorates the hot carrier resistance and the ESD immunity [3]. The use of phosphorus in LDD implant can be help grading the nLDD doping profile and results in a smaller electric field. However, Nayak *et al.* [1] had reported that the electrical characteristics and the hot carrier immunity of the pure phosphorus nLDD structure were better than those of hybrid As/P LDD structure. In this paper, it is our intention to optimse the phosphorus LDD doping profile without short channel effect degradation, to change the implant angle and the implant dose, and the heat cycle effect during thin file deposition after source/drain (S/D) implant.

Table 1. Key split items for high voltage I/O NMOSFETs.

Split Items	Condition
LDD implant dose	~ 10^{13}/cm^3
LDD implant angle	small, large
LDD implant energy	low, high (low + 10 keV)
V_{TH} implant dose	V_{TH} target: 0.5 ~ 0.7 V
Thin film deposition	plasma or CVD

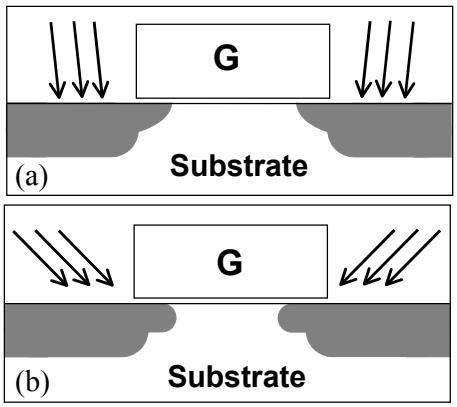

Figure 1. Schematic design concepts of the pure phosphorous structure using cross-sectional view of I/O NMOSFETs. (a) Conventional small angle titled LDD structure and (b) large angle titled LDD structure.

2. Experimental Conditions

After shallow trench isolation (STI) formation, well and retrograde channel was formed. Devices were fabricated based on 0.1-μm CMOS technology with dual poly (n+/p+) gate and dual gate oxide thickness. $CoSi_2$ salicide process was applied to reduce gate electrode and source/drain resistance. In order to suppress the thermal budge, a high-ramp-rate spike annealing process has been

performed for forming the LDD and the S/D region. The wafers were split items in listed in Table 1. We analyzed the LDD dose and the implant-angle effect, and thin film thermal effects during the oxide deposition process. Fig.1 shows the schematic device design concepts of the pure phosphorous structure using cross-sectional view of I/O MOSFETs.

3. Electrical Characteristics

Fig. 2 shows that the threshold voltage (V_{TH}) roll-off (up) characteristics are slightly dependent on the value of V_{TH} with the high V_{TH} and the low V_{TH} devices.

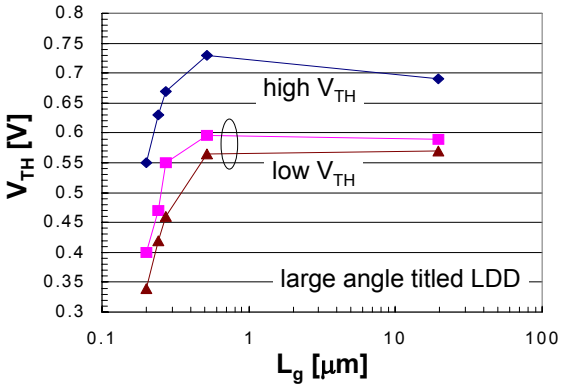

Figure 2. The threshold voltage as a function of the gate length with three processes conditions. V_{TH} were extracted at the constant drain current with 0.1 V of V_{DS}.

The short channel effects are compared with various split conditions shown in Fig. 3. ΔV_{TH} is the difference of V_{TH} between 0.24 μm of L_g and 0.2 μm of L_g and is criterion of the short channel effect in this paper. The V_{TH} variation of high LDD dose devices in low V_{TH} split group [in high V_{TH} dose split group] is 30 ~ 40% [5 ~ 10%] higher than those of low LDD dose devices. LDD implant energy is not the serious factor of short channel effect due to small energy deference (10 keV in this split, see in Table 1) between low implant energy and high implant energy. The implant angle influence in the high dose LDD device is more sever than those of the low dose LDD device, but relative high V_{TH} (0.7 V) split group is not sever. From this result, we find that the relative high V_{TH} and high LDD dose split group are more suitable process condition. Fig. 4 shows the reverse short channel effects with various device splits. Reverse short channel effect (ΔV_{TH}), which means the threshold voltage difference between 20 μm of L_g and maximum V_{TH} of short channel device, is shown the dependence of V_{TH} implant dose. The V_{TH} difference of the high V_{TH} split group is larger than that of the low V_{TH} split group because the channel dopant moves to the surface near to source/drain caused by transient enhanced diffusion (TED) during S/D annealing. Fig. 5 presents the operating domain I_{Dsat}-I_{off} for NMOSFETs. The devices with the high V_{TH} and the high LDD dose split group have significantly better I_{Dsat}-I_{off} characteristics than those with the low V_{TH} and the low LDD dose split group. The improvement is partly attributed to the better short channel effect and low S/D resistance.

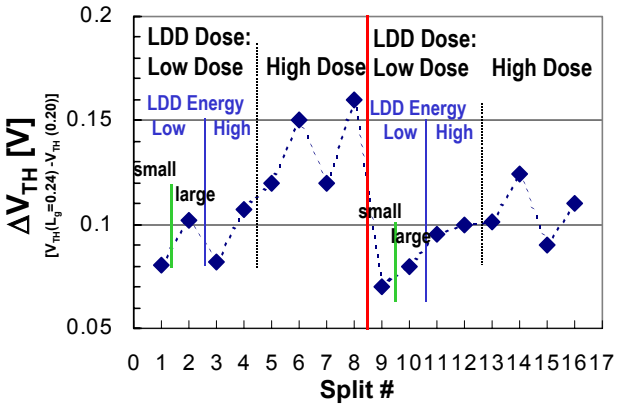

Figure 3 Short channel effect for I/O NMOSFETs with various split conditions. ΔV_{TH} means the V_{TH} different between V_{TH} (0.24) and V_{TH} (0.2).

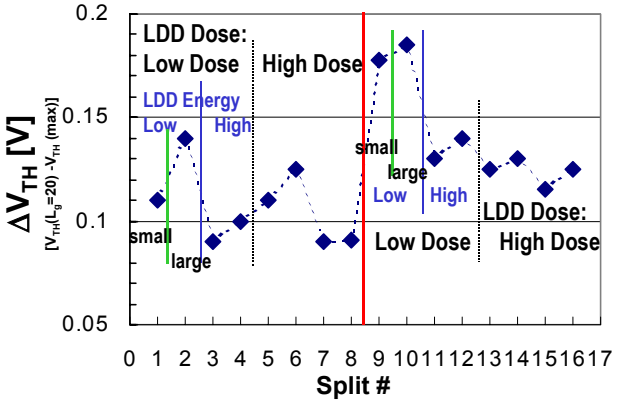

Figure 4. Reverse short channel effect for I/O NMOSFETs with various split conditions.

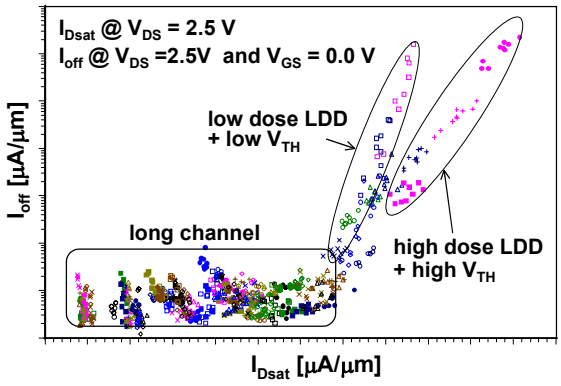

Figure 5. Comparison of off-state drain leakage current (I_{off}) versus saturation drain current (I_{Dsat}) for various LDD process conditions.

4. Device Simulation

We performed for optimisation to meet device performance and minimise the electric field for hot carrier immunity for boron in n-channel LDD MOSFET using 2-D device simulator. The electric field represents an avalanche region with impact ionization. The lateral electric fields are compared with three different LDD MOSFET at horizontal cut-line 0.04 μm below gate oxide region. Fig. 6(a) and (b) show the cross-sectional view of MOSFETs and the electric field at cut-line. In Fig. 6(b), this value of the electric field at 0.04 μm below gate oxide region is sufficiently to pass hot carrier reliability specification.

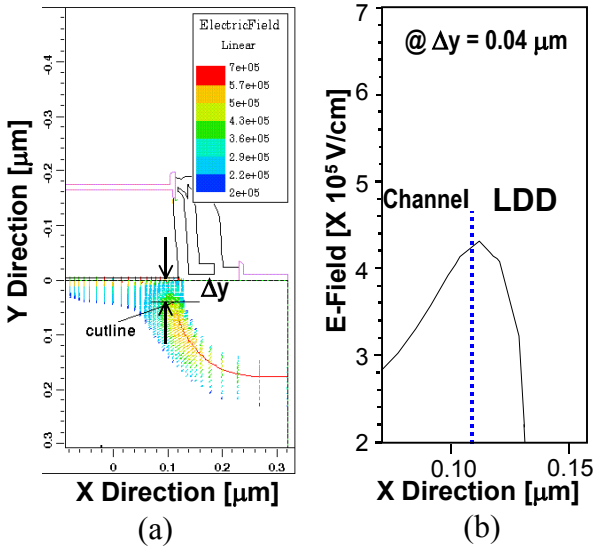

Figure 6. (a) The cross-sectional view for device simulation. (b) Electric field (4.3 X 10^5 V/cm) at the cut-line (at 0.04 μm below gate oxide) as optimised for 4.5 nm NMOSFETs w/o pocket (where measured hot carrier immunity was within spec).

Comparison of the electric field with three different devices at the operating voltage is shown in Fig. 7. In the figure, **device-a** has the high dose and the large angle tiled LDD structure, **device-b** has high dose and the small angle tiled LDD structure, and **device-c** has the low dose and the large angle tiled LDD structure. The simulated electric fields for I/O NMOSFETs after optimasation are less than the optimsation done for 4.5-nm-gate-oixde -thick NMOSFETs without pocket implant which were passed the specification of the hot carrier lifetime. In device-a, the electric field region moves deeper into the substrate and the magnitude of the electric field is lowering than that in device-c and device-c. The channel current path is therefore separated from the electric field region, thus leading to a smaller impact ionization rate than in device-b, and device-c. As simulation result, better hot carrier reliability can be obtained by higher LDD dose and larger angle titled implant. Fig. 8 shows the electric field variation according to the cut-line locations. The peak electric field is located in near cut-line 80 nm below gate interface. The location of the electric field is deeper than the reported hybrid LDD structure [2] in the similar CMOS technology.

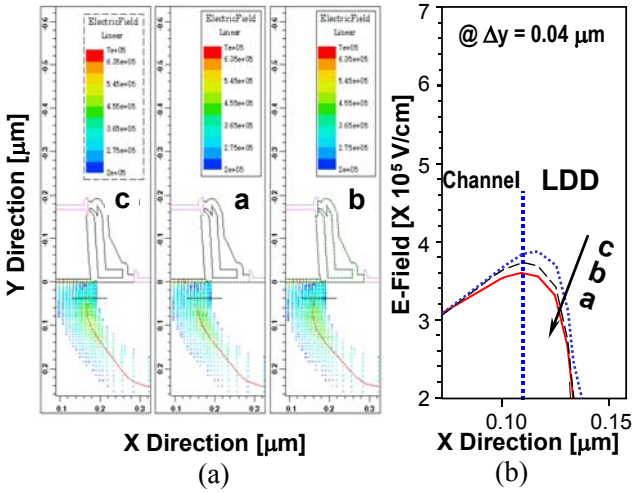

Figure 7. (a) Electric field contours with various devices. (b) The comparison of electric fields for three different devices (solid line-a: high dose and large angle tiled LDD structure, dashed line-b: high dose and small angle tiled LDD structure, dotted line-c: low dose and large angle tiled LDD structure).

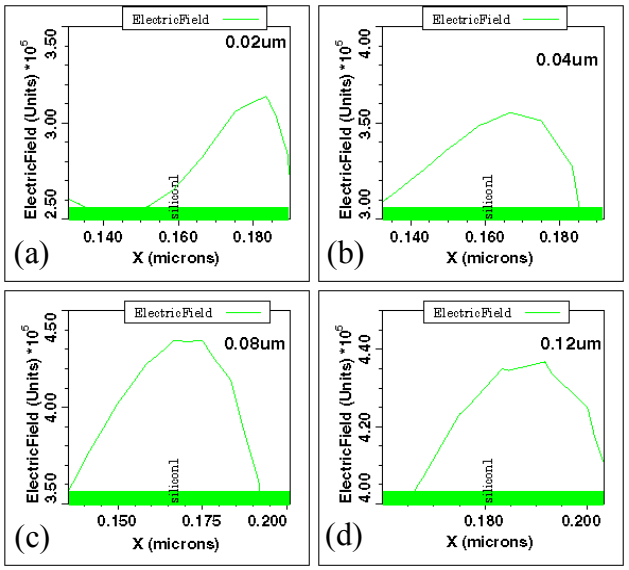

Figure 8. Electric fields for 0.1-μm process as at slide line (device-a) in Fig. 7 with boron in channel. The fields are at cut-lines 0.02-μm (a), 0.04-μm (b), 0.08-μm (c), and 0.12-μm (d) below gate interface.

5. BELO Process Effects

The substrate current is generated by impact ionization in drain junction region. Thus, comparison of substrate current with different process conditions; we can predict the hot carrier immunity. Fig. 9 shows the change of substrate current according to the LDD implant dose and the different back-end-of-line (BEOL) process. Increases LDD dose from low LDD as a result of high LDD dose (1.4 times higher than low LDD dose) improves I_{Bmax}-I_{Dsat} performance the resulting of more grade junction.

The improvement of I_{Bmax}-I_{Dsat} is partly contributed to the more graded LDD junction profile as a result of the higher thermal budget (Thin Film-2) without short-channel-effect degradation, during silicide block process for the poly-si gate and the active resistor after LDD implant. Comparison of thin film-1 and low LDD dose group, the current drivability of thin film-2 and high LDD dose group increases about 8% and the substrate current of one decreases ~ 15% respectively.

The gate reoixdation process for I/O MOSFETs reduces the substrate current due to lower vertical electric field and more graded LDD junction caused by oxide enhanced diffusion and thermal effects (not shown in this paper). Also, gate reoxidation process improves the operating circuit speed due to the reduction of gate overlap capacitance.

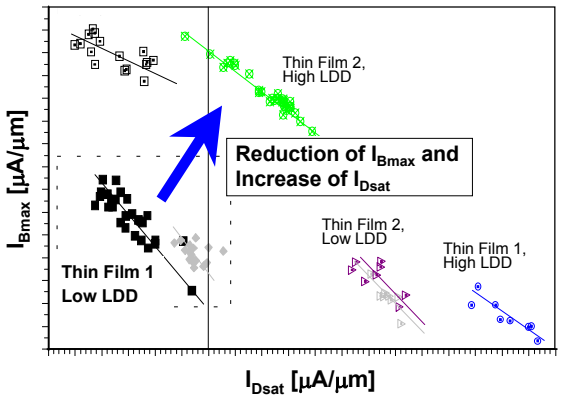

Figure 9. The influences of the substrate currents and the operation currents were change caused by the change of LDD implant dose and thin film deposition condition. Dashed box shows the standard process condition.

6. Conclusion

We have shown that drain engineering plays an important role in scaling of high voltage I/O MOSFETs and analog MOSFETs with thin gate oxide and channel engineering for 0.1-μm CMOS technology. Overlapped phosphorus LDD devices suppress the hot carrier injection into gate oxide and interface between oxide and silicon because large angle titled implant is to keep the hot carrier generation site away from the Si/SiO_2 interface and to reduce electric field. Also, without short-channel-effect degradation, the increase of LDD dose concentration and the change of thin-film deposition process condition improve I_{Bmax}/I_{Dsat} performance due to more graded S/D junction. Although, the ESD related electrical characteristics are not shown in this paper, the heavier/deeper phosphorus-implant performed at the LDD step and the graded junction implant after the spacer formation structure improves the ESD performance without additional high-dose ESD implant step.

7. Acknowledgements

The authors would like to thank the member of unit process module, process integration module and TCAD team for helpful discussions and supporting.

References

[1] D. K. Nayak, M-.Yin Hao, J. Umali, and R. Rakkhit, " A Comprehensive study of Performance and Reliability of P, As, and Hybrid As/P nLDD Junctions for Deep-submicron CMOS Logic Technology", *IEEE Electron Devices*, vol. 18, no. 6, pp.281-283, June 1997.

[2] H.C-.H. Wang, C. Wang, C. Diaz, B-.K. Liew, J. Sun, and T. Wang, "Arsenic/Phosphorus of Phosphorus Transient Enhanced Diffusion for High Voltage Input/Output CMOS devices," *IEEE Trans. Electron Device*, vol. 49, no. 1, pp.67-71, Jan. 2002.

[3] G. V. Groeseneken, "Hot Carrier Degradation and ESD in Submicrometer CMOS Technologies: How Do They Interact?" *IEEE Trans. Device and Materials Reliability*, vol.1, no.1, pp.23-32, March 2001.

[4] T. B. Hook, E. Adler, F. Guarin, J. Lukaitis, N. Rovedo, and K. Schrufer, "The Effects of Fluorine on Parametrics and Reliability in a 0.18-μm 3.5/6.8 nm Dual Gate Oxide CMOS," *IEEE Trans. Electron Device*, vol. 48, no.7, pp.1346-1353, July 2001.

[5] A-.J. Annena, G. J. G. Geelen, and P.C. de Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 36, no.3, pp.528-538, March 2001.

[6] R. Bellens, G. Van den bosch, P. Habas, J-.P. Mieville, G. Badenes, A. Clerix, G. Groeseneken, L. Deferm, and H. E. Maes, "Performance and Reliability Aspects of FOND: A New Deep Submicron CMOS Device Concept," *IEEE Trans. Electron Device*, vol. 43, no.9, pp.1407-1415, Sep. 1996.

[7] A. Chatterjee, D. Mosher, S. Sridhar, Y. Kim, M. Nandakumar, S-W. Aur, Z. Chen, and P. Madhani, S. Tang, R. Aggarwal, S. Ashbum, and H. Shichijo, "Analog Integration in a 0.35 μm Cu Metal Pitch 0.1 μm gate Length, Low-power Digital CMOS Technology," IEEE IEDM Technical Digest 2001, pp.211-214.

[8] E. Li, E. Rosenbaum, T. Tao, and P. Fang, "Projecting Lifetime of Deep Submicron MOSFETs," *IEEE Trans. Electron Device*, vol. 48, no.4, pp.671-678, April 2001.

[9] Y-.S. Lin, H-.T Huang, C-.C. Wu, Y-.K. Leung, H-.Yang. Pan, T-.E. Chang, W-.M. Chen, J-.J. Liaw, and C. H. Diaz, "On the SiO_2-Based Gate-Dielectric Scaling Limit for Low-Standby Power Applications in the Context of a 0.13 μm CMOS Logic Technology," *IEEE Trans. Electron Device*, vol. 49, no.3, pp.442-448, March 2002.