65 nm Transistors for a 90 nm CMOS SOC Platform

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Abstract

Transistors with 65nm physical gate length for a 90 nm node CMOS technology are reported. Current drive of 775/270 mA/mm (Ioff=30nA/mm) at 1V was achieved for N/P-Ch transistors using a 16 Å oxynitrided gate dielectric to reduce the gate leakage current. The N-channel performance is one of the highest reported thus far. Also, impact of process improvements including pre-gate surface clean, choice of contact ILD material and salicide on the transistor performance was demonstrated. These improvements were used to achieve a higher current drive at a fixed off-state leakage current.

1. Introduction

Aggressive scaling of CMOS devices to sub-0.1 um and below requires increasingly thinner gate dielectrics and lower threshold voltages for high-speed applications. This leads to higher gate leakage and transistor off currents and thus higher chip stand-by power consumption. High K dielectrics have been suggested as a replacement to oxide and oxynitrides to reduce the gate dielectric leakage current. However, based on the most recent studies still more investigation is needed before integrating these dielectric films into commercial CMOS process [1]. Meanwhile, better device and process optimisation allows using a thicker gate oxide with lower leakage current while achieving the required performances for high-speed devices.

In this work, low energy S/D drain extension implants as well as B11 for P^+ deep junctions were used to achieve good short channel behaviour and reduce boron penetration through the thin gate oxide. The choice of pre-gate oxide clean in growing multiple gate oxides using grow-etch-grow scheme was shown to have a significant impact on the device performance. Shallower junctions demand reduced silicon consumption during salicidation leading to the use of nickel instead of cobalt to maintain a similar sheet resistance [2]. Therefore, the impact of NiSi on the transistor performance was investigated in this study. Furthermore, the use of NiSi restricts post-salicidation thermal budget, which led to investigation of HDP over PSG film for contact inter layer dielectric (ILD). These results are important for the manufacturability of the sub- 0.1 μm technologies.

2. Process Integration

Key process steps and features are shown in Fig. 1. N and P channel transistors down to 65nm were fabricated on (100) silicon substrate. After formation of shallow trench isolation and well engineering, triple gate oxides were grown using NO anneal to suppress boron penetration.

- **STI**
- **Well engineering**
- **Triple oxide**
- **Polysilicon gate**
- **Low energy extension**
- **Nitride-composite spacers**
- **S/D implants**
- **Co or Ni silicidation**
- **HDP or PSG for contact ILD**

Figure 1. Process steps

Grow-etch-grow process was used to form triple gate oxides needed for SOC platform. Normally RCA clean is used after the oxide etch and photo-resist strip. However, the chemical oxide formed after photoresist strip may contain impurities that can cause carrier scattering and lowered mobility. To avoid this, a clean process with very dilute HF was used to remove this chemical oxide before growing a 16 Å oxynitride film for high performance devices. Polysilicon gate electrode was deposited and patterned using a 193nm photolithography tool. Then, shallow extension junctions were formed by As and BF_2 implants with energies as low as 3keV followed by nitride spacer formation. A low energy B11 implant was used to form the source/drain junctions for the P-channel devices to reduce the boron penetration caused by fluorine in BF_2. 150 Å of Ni or 100 Å of Co was used for salicidation process. Use of nickel allows formation of a more uniform silicide film with lower sheet resistance compared to that of the cobalt silicide for a similar silicide thickness. Finally, devices were fabricated with

HDP or PSG film as inter layer dielectric (ILD) for contacts and their impact on the P-ch transistor performance was studied. A SEM cross-section of the final transistor with a channel length of 65 nm is shown in Fig. 2.

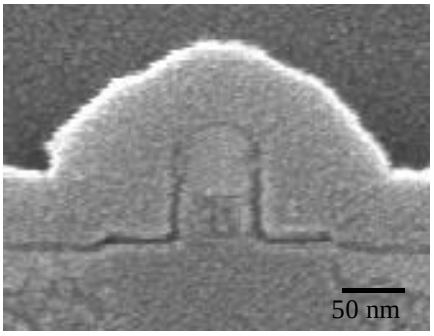

Figure 2. 65 nm device cross-section

3. Device Performance and Improvement

C-V characteristic of the NMOS capacitor is shown in Fig. 3. Small area capacitors (30x30µm) were used in order to minimize the impact of the gate leakage current on the C-V measurement. The extracted gate oxide thickness from the C-V data using NCSU's model [3] is about 15.8 Å. Gate oxide area leakage current is shown in Fig. 4. This leakage current was measured with the source and drain connected to substrate and is about 0.8 A/cm^2 for the 15.8 Å oxide. This low gate leakage current was achieved by efficient nitrogen incorporation through the NO anneal.

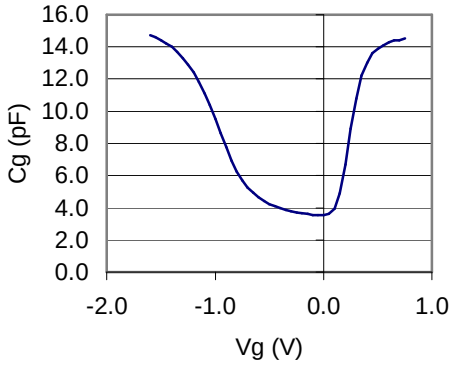

Figure 3. C-V of 30x30 um NMOS capacitor

N and P channel transistor characteristics are shown in Figs. 5 & 6. A current drive of 775 and 270 µA/µm was achieved for N and P channel devices, respectively, at Ioff=30nA/µm and Vdd=1V. Both N and P channel devices show good sub-threshold behavior with slopes of approximately 86 mV/dec and 95 mV/dec, respectively. Ion-Ioff behavior of the N and P channel devices over a range of channel lengths is shown in Fig. 7, demonstrating working devices with Ioff as low as 1nA/µm.

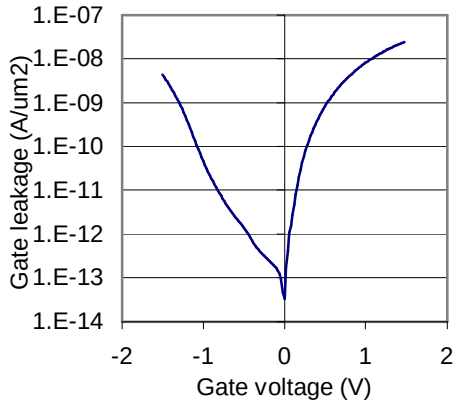

Figure 4. Gate leakage current for N-channel device

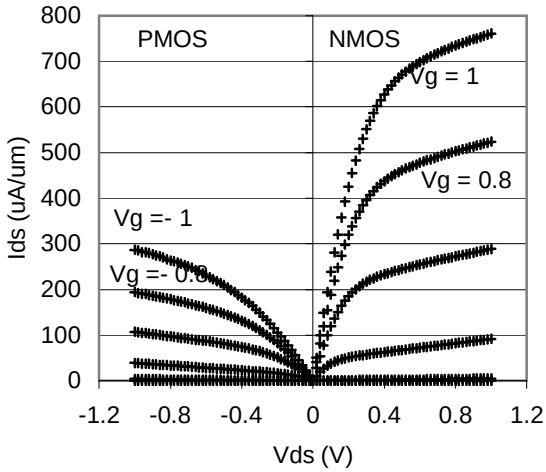

Figure 5. Ids-Vds characteristics of 65nm N and P channel transistors for 1Volt operation.

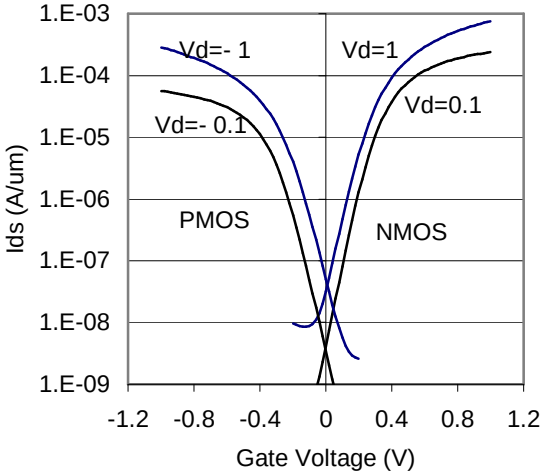

Figure 6. Ids-Vgs characteristics of 65nm N and P channel transistors with EOT of 15.8 Å. Sub-threshold slopes for N and P-ch devices are 86 and 95 mV/dec, respectively.

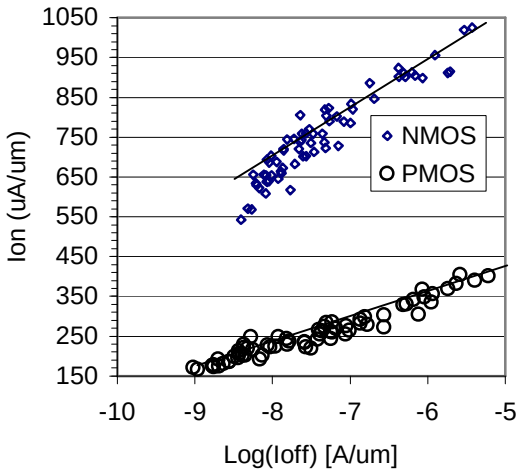

Figure 7. Ion-Ioff behaviour of N and P channel transistors operating at 1Volt

A comparison of the current drives achieved in this work and other sub 0.1 µm technology node device performances reported most recently [4,5,6] are listed in Table 1. The N-channel current drive at Ioff=60nA/um is 820µA/um, which is one of the highest reported in industry for 1.0 V operation.

Table 1. A comparison to other recent works

1.0V operation		This work		IBM	Motorola	Hitachi
				IEDM 01	IEDM 01	IEDM 01
N-ch	Idsat (uA/um)	775	820	800	680	670
	Ioff (nA/um)	30	60	60	10	100
P-ch	Idsat (uA/um)	270	290	340	290	280
	Ioff (nA/um)	30	60	60	10	100

As discussed earlier, in grow-etch-grow process the chemical oxide formed after photoresist strip/clean can cause carrier scattering and lowered mobility. Impact of the pre-gate oxide clean with very dilute HF on the device performance is shown in Fig. 8. An 8% increase in the current drive of the NMOSFET was observed for the HF last pre-gate oxide clean at the same Ioff value. The quality of the silicon surface prior to oxidation improves high field mobility, leading to observed improved performance.

Furthermore, the use of Ni salicide process also boosts the current drive by another 10% for P-ch transistors as shown in Fig. 9. This is due to the reduced series resistance and reduced thermal budget in nickel mono-silicide formation. Ni salicide reduced diffusion sheet resistances by ~30% in comparison to Co salicide.

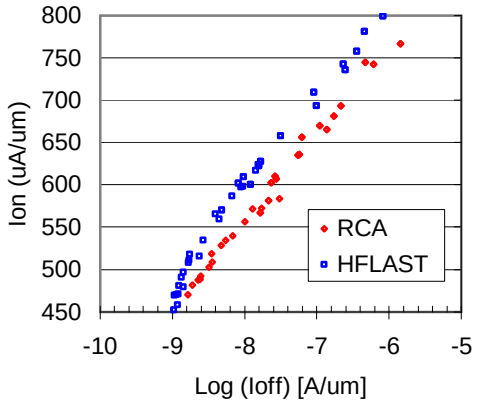

Figure 8. Pre-gate oxidation clean impact on the N-channel transistors current drive.

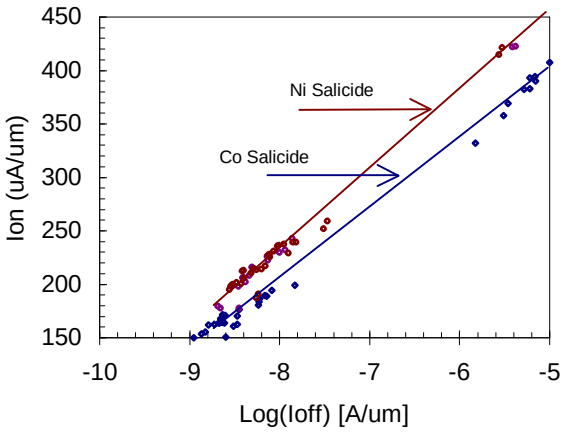

Figure 9. Impact of Ni vs.Co salicide on P-ch device

The use of low temperature HDP oxide vs. PSG as the contact ILD material shows an 8% improvement in P channel performance as shown in Fig. 10. This improvement is believed to be due to reduced thermal budget for HDP process in comparison to PSG process, which further reduces boron penetration.

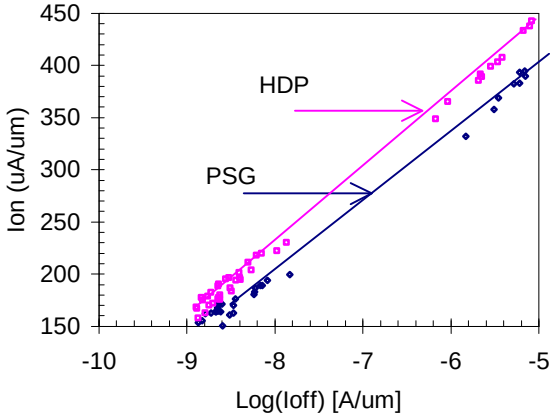

Figure 10. PMOS Ion-Ioff deterioration due to PSG

Finally, the delay per stage of an inverter ring oscillator with single fan-out is shown in Fig. 11, which demonstrates a 9.9 psec delay for fast devices and a 10.9 psec delay for nominal N/P channel devices with Idn/Idp=775/270 μA/μm can be achieved.

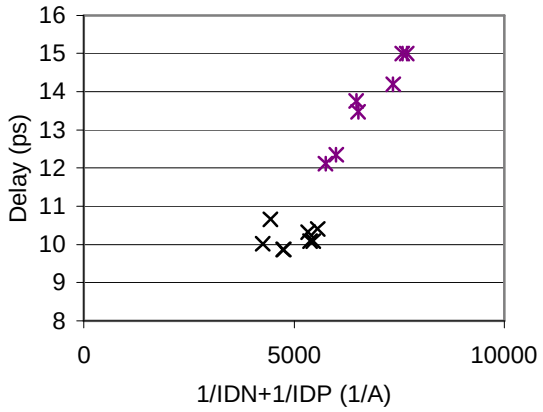

Figure 11. Ring oscillator delay at 1V operation

4. Conclusions

65nm high performance transistors (Idn/Idp= 775/270 μA/μm@1V and 30nA/μm off-state leakage) for 90 nm CMOS technology node were demonstrated. Different process improvement techniques were used to achieve higher transistor drive currents at the same off state leakages. An 8% increase in the current drive of the NMOSFET was achieved when HF last pre-gate clean was used. Also, use of HDP as ILD material for contacts improved the current drive of PMOSFET by about 8% in comparison to PSG. Application of NiSi had a similar impact on the current drive (10%) with respect to the cobalt salicide. Above process improvements led to a low ring oscillator delay of 9.9 psec per stage.

5. Acknowledgements

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6. References

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