Improved Deep Sub-micron CMOS Ring Oscillator Performance with n-HDD and n-LDD P^+ + As^+ Co-Implant

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Abstract

The purpose of this work is to investigate the influence on speed and energy consumption of CMOS inverters, resulting from the usage of a P^+ + As^+ co-implantation for the fabrication of the source/drain junctions and extensions for two technologies: 100 nm and 130 nm (nominal gate length). Additionaly, the effect of oxide thickness on power consumption was verified. To perform the experiment, n-MOS devices were fabricated with and without a co-implanted n-HDD and n-LDD. The speed vs. energy performance was measured in 41 stages ring oscillators. For 100 nm devices with 1.5 nm oxide, the ring oscillators of the co-implanted samples, showed up to 40 % gate-delay improvement, but at the expense of higher energy consumption. For 130 nm devices with 2.0 nm thick oxide an improvement of 19 % was achieved, without increase in energy consumption. 130 nm devices with co-implanted n-LDD showed a reduction in gate-delay of $\simeq$8 %.

1. Introduction

Intrinsic device and interconnect capacitances and resistances are key elements that limit speed performance in CMOS technologies. Therefore, during the cycles for process integration of a CMOS flow it is necessary to monitor variables that can lead to a convenient assesment of those parasitics. Although $I_{\rm on}$ and $I_{\rm off}$ data are extensively used to compare and fine tune process flows, they contain information regarding only DC parameters. Flows that produce devices with similar $I_{\rm on} \times I_{\rm off}$ characteristics can result in different speed performance.

It is also used to estimate the technology potential speed by plotting CV/I (estimated gate delay) vs. CV^2 (estimated energy per transition) [1, 2], where C is an estimative of the total parasitic capacitances, extracted from test structures, V is the nominal drain voltage and I is an estimative of the average on-state current for both channels (n and p), also extracted from test structures. This procedure is not adequate for advanced devices because the total current consumption is largely influenced by their high off-state current and the effect of device's intrinsic parasitic elements coupled to parasitics from the interconnections. It does not give a correct idea of performance vs. energy consumption at circuit level.

A more realistic approach to get a figure for the speed performance vs. energy consumption is the usage of ring oscillators with CMOS inverters. In this case, gate delay and energy per transition are directly measured by monitoring the frequency and the current consumption of the oscillator [3, 4].

In this work, n-MOS devices were fabricated with different LDD and HDD implant schemes and ROP data (*Ring Oscillator Performance*) was obtained and analysed.

2. Methodology and Experiment

Ring oscillators with 41 stages were fabricated with state-of-the-art CMOS processes. n-MOS devices received different implant conditions for junctions and extensions. The standard implants are done with arsenic only. The co-implanted devices got a phosphorus implantation on top of the arsenic profile. The arsenic implantation has the function of providing a low sheet resistance and the phosphorus implantation is intended to render a smoother junction with lower capacitance. Previous works demonstrated lower parasitics in n-MOS with co-implanted HDD [5] and LDD [6]. To verify the influence on ROP of a P^+ co-implantation on top of the As^+ implantation for the n-HDD and n-LDD, six wafers were prepared, labeled WFR01 to WFR06. These wafers were processed with two different technologies. One targeted for 100 nm devices and another one targeted for 130 nm devices. Both have shallow trench

isolation (STI) and each lot has the same CMOS flow up to metal one with only the differences in n-HDD and n-LDD conditions shown in Table 1.

Table 1. *n-LDD and n-HDD characteristics of the lots processed to verify the effect of P^+ + As^+ co-implants in ROP.*

WFR	L_g [nm]	t_{ox} [nm]	n-LDD	n-HDD
01	100	1.5	As^+, 5 keV	As^+, 40 keV
02	100	1.5	As^+, 5 keV	As^+, 40 keV + P^+, 10 keV
03	130	2.0	As^+, 5 keV	As^+, 50 keV
04	130	2.0	As^+, 5 keV	As^+, 50 keV + P^+, 6 keV
05	130	2.0	As^+, 5 keV	As^+, 50 keV
06	130	2.0	As^+, 5 keV + P^+, 1 keV	As^+, 50 keV

3. Results

Junction capacitance

Junction capacitance was measured in N+/P-Well square diodes with an area of 2.5×10^5 μm^2 and the results are shown in the plot of Fig. 1.

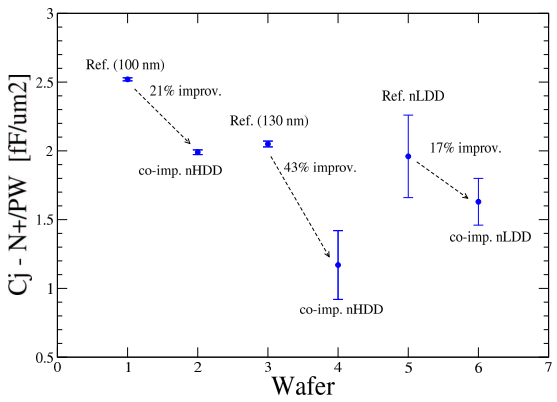

Figure 1. *Junction capacitances measured in square diodes with 2.5×10^5 μm^2 for samples with and without a phosphorus co-implantation. The x-axis represents the wafer number.*

For 100 nm process (wafers WFR01 and WFR02) there was a 21 % improvement for the junction capacitance in the sample with phophorus co-implant (C_j reduced from ≈2.5 fF/μm^2 to ≈2.0 fF/μm^2). For 130 nm technology (wafers WFR03 and WFR04) the improvement was around 43 % for the co-implanted junctions (C_j reduced from ≈2.0 fF/μm^2 to ≈1.2 fF/μm^2). The co-implanted n-LDD also resulted in lower junction capacitance (17 % improvement). This reduction in the junction capacitance is attributed to the smoother doping profile rendered by the phosphorus implantation.

Ring Oscillator Performance

The gate delay reduced for all co-implanted samples (n-LDD as well as n-HDD). The energy consumption didn't improve in all cases and was found to be strongly influenced by the gate oxide thickness.

The plot in Fig. 2 shows the results for wafers WFR01 and WFR02 (1.5 nm gate oxide, with and without a phophorus co-implant), for different drain bias. One can see a significative decrease in gate delay for the devices co-implanted n-HDD (40 % gate delay reduction at 1.2 V). But this improvement happens at the expense of an increase of up to 35 % in energy consumption. To explain such an increase one have to consider

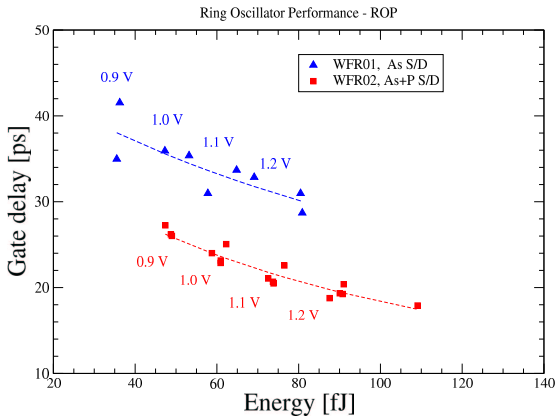

Figure 2. *Gate delay vs. energy consumption measured in ring oscillators with 41 CMOS inverters, $L_g = 100$ nm, $W_p/W_n = 17/10$ μm. The drain bias is varied from 0.9 V to 1.2 V*

that the power supplied to the oscillator is given by the sum of two components ($P = P_{\text{dynamic}} + P_{\text{static}}$) and for technologies with thick oxide, the dynamic power dominates and is usually approximated by CV^2 [5]. However, for thin oxides used in advanced CMOS, the

static power may become important, since high oxide tunneling currents may occur. The static power is given essentially by the total leakage current ($P = V I_{leakage}$) [7], which may be represented by the sum of three components:

$$I_{\text{leakage}} = I_{\text{off}} + I_g + I_j$$

where I_g is the oxide tunneling current, I_j is the reverse bias junction leakage and I_{off} is the subthreshold current. For thick oxides ($\geq$ 2 nm), I_{off} is the dominant component, but when t_{ox} changes from 2.0 nm to 1.5 nm, the oxide leakage current increases two orders of magnitude, for the same bias, and its contribution to the total leakage becomes more relevant. This fact was verified in this work and it explains the higher energy consumption observed in the ring oscillators fabricated with the 100 nm technology. It is also interesting to point out that the optimized W_p/W_n ratio used for technologies in which $I_{\text{leakage}} \approx I_{\text{off}}$ is ≈ 1.7 [7] and this value doesn't hold anymore when the gate oxide tunneling plays a role in the total leakage current. Consequently, further study is necessary to find a W_p/W_n ratio that optimizes the switching speed in deep sub-micron devices with thin oxides.

For WFR03 and WFR04 (2 nm gate oxide) there was also a significative improvement in gate delay (19 % reduction at 1.5 V) but without increase in energy consumption (Fig. 3). This happens because of the lower gate leakage current associated to the thicker gate oxide and also the lower I_{off} presented by these wafers (Fig. 5).

For wafers WFR01 to WFR04 the parameter that had the most remarkable change was the junction capacitance (C_j). This parameter is recognized as the most important component of the gate delay and also of the power dissipation, specially at low voltages [8]. Hence it was expected a general improvement in ROP following the C_j data shown in Fig. 1. This was not the case for 100 nm devices ($t_{\text{ox}} = 1.5$ nm) because the reduction in C_j was counter-balanced by the increase in the gate capacitance, that implied in higher I_{off} and the higher I_g.

For WFR05 and WFR06 (2 nm gate oxide) there was an improvement in gate delay of about 8 % for the sample with co-implanted n-LDD (Fig. 4). This may be associated also to reduction in parasitic capacitances, especially the gate to drain overlap capacitance, resulting from the smoother doping profile. A reduction in energy consumption was also observed for this sample. In this case, the total implant dose was increased in the co-implanted device, the slight reduction in energy consumption is attributed to a reduction in the extension resistance, leading to less power dissipation.

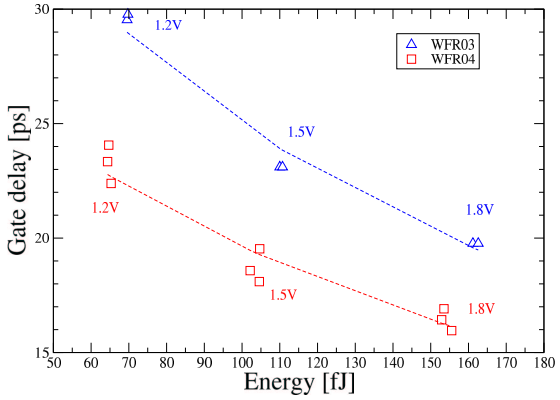

Figure 3. *Gate delay vs. energy consumption measured in ring oscillators with 41 CMOS inverters, $L_g = 130$ nm, $W_p/W_n = 17/10$ μm. The drain bias is varied from 1.2 V to 1.8 V.*

Intrinsic Transistor Performance

Figure 5 shows ITP plots (*Intrinsic Transistor Performance - $I_{\text{on}} \times I_{\text{off}}$*) for n-MOS devices. The bias conditios for wafers WFR01 to WFR04 was 1.2 V and for WFR05 and WFR06 it was 1.5 V. Analysing each pair of wafers that had a co-implantation split, i.e., WFR01/02, WFR03/04 and WFR05/06, we can observe that WFR04 showed in average a slightly higher drive current than WFR03 which certainly was also a factor that influenced the reduction in gate delay observed in WFR04. However, for the other pairs, there is no significative difference in the ITP plots. This shows clearly that process flows showing the same ITP plot can result in CMOS inverters with very different speed performance and enery consumption.

4. Conclusions

Ring oscillators with CMOS inverters were fabricated, with different implant conditions for the n-MOS device. A phosphorus co-implantation was used both for the junction as well as for the extensions.

For a 100 nm technology with $t_{ox} = 1.5$ nm It was found that a P^+ + As^+ co-implant for S/D fabrication of NMOS devices improves the gate delay in up to 40 % while increasing the energy consumption in 35 %, with respect to a process with As^+ implant only. This speed improvement is attributed to the smoother phosphorus

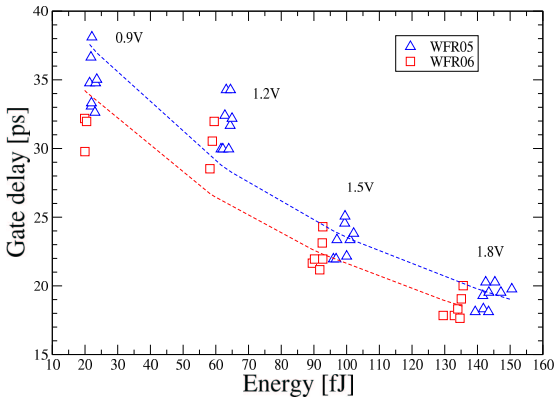

Figure 4. *Gate delay vs. energy consumption for the wafers with co-implanted n-LDD. $L_g = 130$ nm, $W_p/W_n = 17/10$ μm. The drain bias is varied from 0.9 V to 1.8 V.*

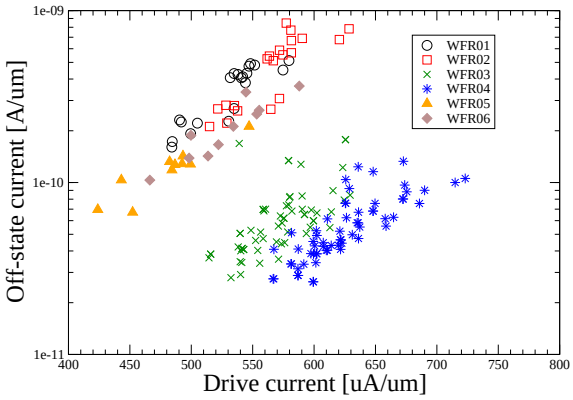

Figure 5. *ITP plot for nMOS. $V_{dd} = 1.2V$ for wafers 01 to 04 and 1.5V for wafers 05 and 06. $L_g = 100$ nm for WFR01/02 and 130 nm for the other wafers.*

doping profile, and consequent junction capacitance reduction.

For a 130 nm technology with $t_{ox} = 2.0$ nm, the gate-delay reduced 19 % for the co-implanted n-HDD and there was no increase in energy consumption. The reduction in gate-delay was related to the C_j improvement and the low energy consumption was attributed to the lower gate tunneling current. This shows the importance of reducing the oxide tunneling in order to keep the energy consumption well controlled. For the co-implanted n-LDD an improvement of 8 % in gate delay was achieved without energy increase.

Comparing ROP for 100 nm and 130 technologies, it was found a different pattern in energy consumption. 100 nm oscillators consume more power because of its high gate tunneling current and requires re-optimization of the W_p/W_n ratio.

The analysis of ring oscillator performance was found indispensable in a feed-back loop for the fine tunning of deep-submicron CMOS process flows.

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