Influence of Doping Profile and Halo Implantation on the Threshold Voltage Mismatch of a 0.13 μm CMOS Technology

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Abstract

The fluctuation mechanisms which determine the threshold voltage mismatch of a 0.13 μm technology are investigated by varying the bulk bias. The correct doping profile, obtained by SIMS measurements, is included in the analysis. This leads theoretically to a 20-35 % lower threshold voltage mismatch than when the profile is assumed uniform. The experimental threshold voltage mismatch is significantly higher than the theoretical limit caused by doping fluctuations. This is caused by the halo implant, which is implanted through the gate. The fluctuation in this charge is not described by Poisson statistics. It is mainly caused by the random character of the poly-silicon gate material. By correlating threshold voltage mismatch to current factor mismatch it is shown that the halo implant also causes extra fluctuations in gate depletion.

1. Introduction

Threshold voltage mismatch is one of the main analogue performance indicators of a CMOS technology, since it determines the accuracy-speed-power trade-off of the basic analogue building blocks. For digital CMOS it is considered to be one of the downscaling roadblocks. The fundamental lower limit of threshold voltage mismatch is due to doping fluctuations [1-3]. Two other causes of mismatch are oxide capacitance fluctuations and interface charge fluctuations [1,4]. These three fluctuation mechanisms can be distinguished by examining the bulk bias dependence [4,5].

In this work, for the first time, the contributions of all three fluctuation mechanisms are determined. The true doping profile, obtained with SIMS measurements, is included in the analysis. Section 3 investigates the differences between using the correct profile and an, in previous work assumed, uniform profile. Determining the magnitude of the separate fluctuation mechanisms (section 4) gives valuable information for technology optimisation. It is shown that the halo implant can seriously degrade long channel threshold voltage mismatch. In section 5 this effect is thoroughly investigated by varying the halo implant dose and angle.

2. Theory

This section lists the equations for threshold voltage (V_T) and threshold voltage mismatch ($\sigma_{\Delta VT}$) for arbitrary doping profiles. It is assumed that the charge sheet approximation holds and that the depletion region width does not vary with gate bias in strong inversion. In this case the threshold voltage is given by:

$$V_T = V_{FB} + \varphi_B + \frac{Q_i t_{ox}}{\varepsilon_{ox}} + \frac{q t_{ox}}{\varepsilon_{ox}} \int_0^{W_D} N_A(x)dx \,, \qquad (1)$$

where $N_A(x)$ is the doping level at depth x, q the elementary charge, Q_i the interface charge, t_{ox} the electrical oxide thickness (~2.7 nm), V_{FB} the flatband voltage and ε_{ox} the permittivity of the oxide. The bulk potential $\varphi_B = 2\varphi_F = 2(kT/q)\ln(N_A(0)/n_i)$, where n_i is the intrinsic concentration and φ_F the Fermi potential. Besides using the electrical oxide thickness, quantum-mechanical effects are not included. The depletion region width (W_D) is calculated by numerically solving:

$$\frac{q}{\varepsilon_{si}} \int_0^{W_D} x N_A(x)dx = \varphi_B - V_{BS} \,, \qquad (2)$$

where ε_{si} is the permittivity of silicon.

The total threshold voltage mismatch ($\sigma_{\Delta VT,total}$) is calculated by quadratically adding the contributions from doping fluctuations ($\sigma_{\Delta VT,doping}$), interface charge ($\sigma_{\Delta VT,Qi}$) and oxide thickness ($\sigma_{\Delta VT,Cox}$):

$$\sigma^2_{\Delta VT,total} = \sigma^2_{\Delta VT,doping} + \sigma^2_{\Delta VT,Qi} + \sigma^2_{\Delta VT,Cox} \qquad (3)$$

The contribution due to doping fluctuations is modelled in [2,3] and is given by:

$$\sigma^2_{\Delta VT,doping} = \frac{2q^2 t^2_{ox}}{WL\varepsilon^2_{ox}} \int_0^{W_D} N_A(x)\left(1 - \frac{x}{W_D}\right)^2 dx \qquad (4)$$

This equation was experimentally verified in [6]. The contribution due to interface charge is given by [1]:

$$\sigma^2_{\Delta VT,Qi} = \frac{2qQ_i t^2_{ox}}{WL\varepsilon^2_{ox}} \qquad (5)$$

Both equations are based on the assumption that charge fluctuations are described by a Poisson distribution for which $\sigma^2_{NA} = N_A/WL$ (per unit depth) and

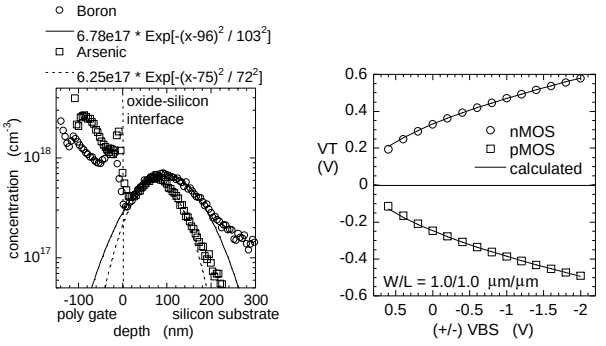


Figure 1: a) *SIMS measurements of doping profiles for nMOS and pMOS transistors.* b) *experimental and calculated threshold voltage as function of the bulk bias.*

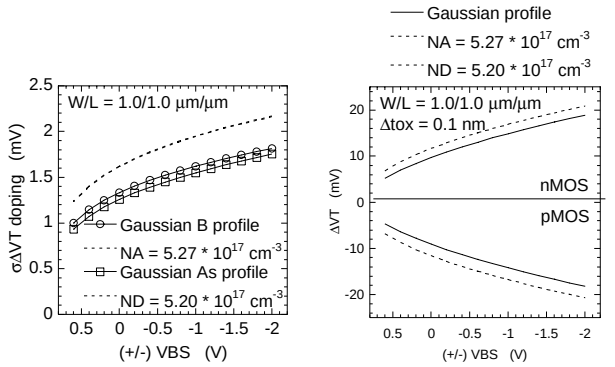


Figure 2: *Calculated influence of uniform profiles and the Gaussian profiles from figure 1 on threshold voltage mismatch due to* a) *doping fluctuations and* b) *an increase in oxide thickness of 1 Å*

$\sigma_{Qi}^2 = qQ_i / WL$. The contribution due to oxide thickness fluctuations follows from equation 1 and is given by:

$$\sigma_{\Delta VT,Cox} = \frac{q}{\varepsilon_{ox}} \int_0^{W_D} N_A(x)dx \cdot \sigma_{\Delta tox} \qquad (6)$$

Note that the bulk bias dependence in equations 1, 4 and 6 arises from the bulk bias dependence of the depletion layer width, which is given by equation 2.

3. Comparison of Gaussian and uniform doping profiles

To examine the influence of the doping profile on threshold voltage mismatch, SIMS measurements were performed. The results are plotted in figure 1a. The doping in the gate is caused by the halo implant. The measurement is inaccurate close to the oxide-silicon interface due to roughness of the gate. To obtain an accurate description of the profile, a Gaussian shape is assumed, which is fitted to the peak. Figure 1b shows that the bulk bias dependence of the threshold voltage is well described by equations 1 and 2, using this Gaussian profile. A similar bulk bias dependence can be obtained

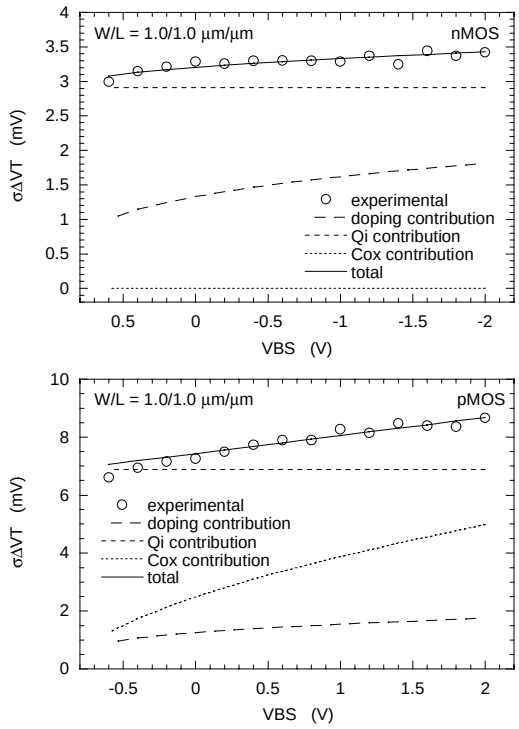


Figure 3: *Experimental threshold voltage mismatch as a function of the bulk bias and the contribution of the three fluctuation mechanisms*

when a uniform profile is assumed. In this case for nMOS devices $N_A=5.27\cdot10^{17}$ cm^{-3} and for pMOS devices $N_D=5.20\cdot10^{17}$ cm^{-3}. In this work, the threshold voltage is extracted with the maximum slope method.

Figure 2 compares the calculated threshold voltage mismatch contributions for the case of the Gaussian and uniform profiles. It is seen that by using the Gaussian profile the predicted threshold voltage mismatch due to doping fluctuations is 20-35 % smaller and the threshold voltage mismatch due to oxide capacitance fluctuations is 10-25 % smaller. It follows from equations 2, 4 and 6 that this is due to the position of the doping, which is located further away from the interface for a Gaussian profile. Fluctuations due to interface charge do not vary with the bulk bias.

4. Separation of fluctuation mechanisms

To separate the fluctuation mechanisms of a 0.13 µm technology [7], threshold voltage mismatch is extracted as a function of the bulk bias from 42 device pairs. The contribution due to doping fluctuations can be calculated from equation 4, because the correct doping profile is known. This contribution is subtracted from the total mismatch, using equation 3. From the residue the contributions due to interface charge and oxide thickness fluctuations are extracted by a linear least squares fit.

The results of this exercise are shown in figure 3. For the nMOS transistors the largest contribution to the mismatch is caused by interface charge fluctuations. The bulk bias dependence is completely due to doping

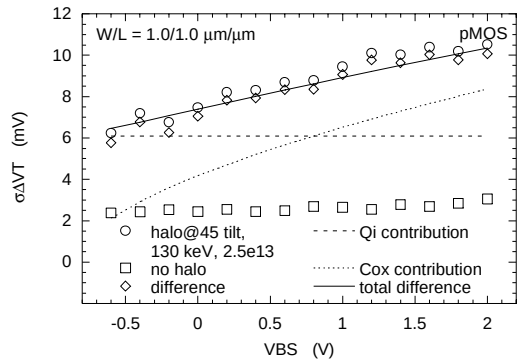
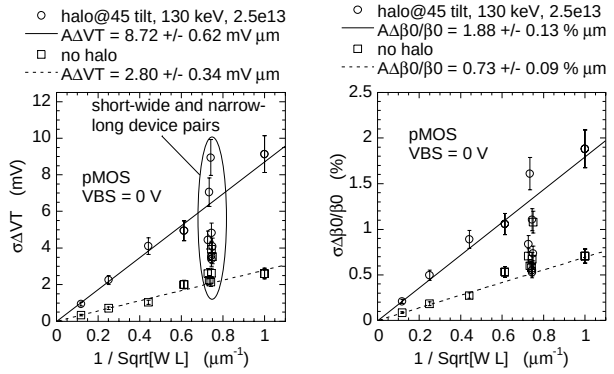


Figure 4: *Comparison of bulk bias behaviour of threshold voltage mismatch for transistors with and without halo implant*



(a) (b)

Figure 5: $1/\sqrt{WL}$ *behaviour of* a) *threshold voltage mismatch and* b) *current factor mismatch for transistor pairs with and without halo implant*

fluctuations. Fluctuations in the oxide thickness are negligible. For the pMOS transistors all mechanisms are present. The largest contribution is again due to interface charge fluctuations. From equation 6 the fluctuations in oxide thickness are calculated to be $\sigma^2_{\Delta tox}/t^2_{ox} = 2.0\,\%^2\,\mu\text{m}^2/WL$. These fluctuations are not caused by fluctuations in physical oxide thickness, since they would also have been observed for the nMOS transistors. They can therefore be attributed to fluctuations in gate depletion [8], which differs for nMOS and pMOS transistors. It will now be shown for the pMOS transistors, that the large contribution of 'interface charge' fluctuations and the fluctuations in oxide capacitance are due to the halo implant.

5. Impact of halo implantation

Figure 4 compares the bulk bias behaviour of the pMOSFET threshold voltage mismatch for a wafer without halo and for a wafer which received a (too strong) 45° Arsenic halo implant at an energy of 130 keV and with a dose of $2.5{\cdot}10^{13}$ cm^{-2}. Figure 5 shows the $1/\sqrt{WL}$ behaviour [1,9] of the threshold voltage mismatch and the current factor mismatch. From figure 4 it follows that the halo increases both the fluctuations due

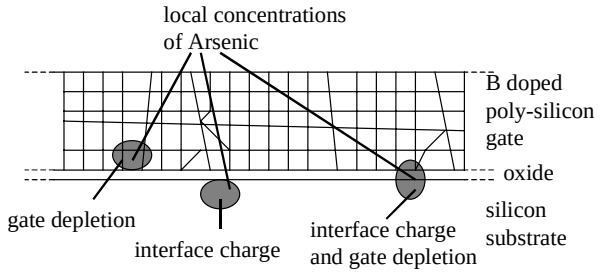
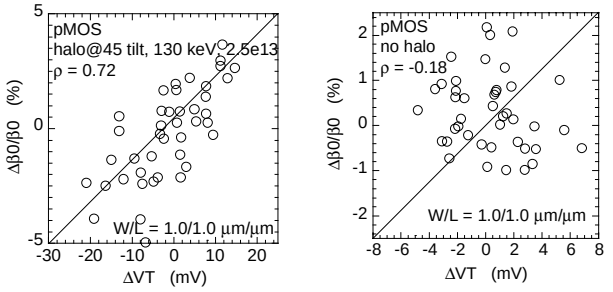


Figure 6: *Schematic drawing of the position of local high concentrations of Arsenic close to the gate oxide*



(a) (b)

Figure 7: *Correlation between threshold voltage mismatch and current factor mismatch for transistor pairs with* (a) *and without* (b) *halo's.* V_{BS}*=0 V*

to charge close to the silicon-oxide interface and the fluctuations in gate depletion. Apart from deviations for short and narrow devices, normal $1/\sqrt{WL}$ behaviour is observed for both cases. It can therefore be concluded that the halo implantation increases the doping level close to the oxide over the whole area of the transistor and not only at the source and drain ends. The increase in 'interface charge' fluctuations means that the halo is implanted through the 150 nm thick poly gate. Because this halo charge (Q_h) is located close to the oxide-silicon interface it has the same effect on threshold voltage and threshold voltage mismatch as interface charge. A long-channel threshold voltage shift of 50 mV is observed. From equation 1 it follows that this corresponds to an increase in Q_h of $4.0{\cdot}10^{11}$ cm^{-2}. According to equation 5 this extra charge gives rise to an increase in $A_{\Delta VT}{}^2$ of 1.3 mV^{2}µm^2, which is much smaller than the observed difference of 35 mV^{2}µm^2. This shows that the main part of the fluctuations is not due to the discreteness of the doping, but that it is caused by the random character of the poly-silicon gate material (see figure 6). The grain sizes, gate roughness and the position of the grain boundaries are not exactly the same for two separate gates. This leads to a different amount of charge, implanted through each gate.

The oxide capacitance contribution to the increase in threshold voltage mismatch (see figure 4) corresponds to $\sigma^2_{\Delta tox}/t^2_{ox} = 2.89\,\%^2\,\mu\text{m}^2/WL$, which is very close to the $3.00\,\%^2\,\mu\text{m}^2$ change in $A_{\Delta\beta0/\beta0}{}^2$, observed in figure 5. This proves that the halo implant indeed causes oxide

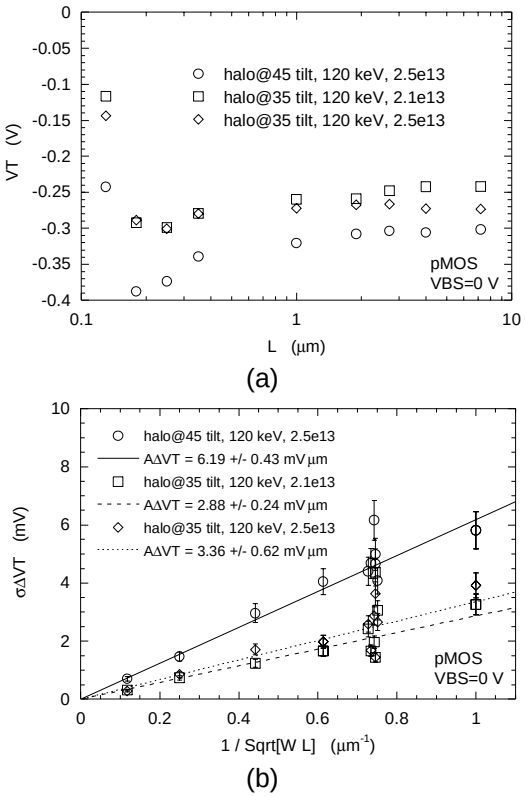


Figure 8: *Threshold voltage roll-off* (a) *and mismatch* (b) *for transistors with 35º and 45º halo implants*

capacitance fluctuations. The halo implant locally compensates the gate doping at the oxide-poly interface (see figure 6). Figure 7 shows that a significant correlation exists between ΔV_T and $\Delta\beta_0/\beta_0$ in the case of halo implantation. The correlation is too high to be purely explained by oxide capacitance fluctuations. This reveals a correlation between fluctuations in Q_h and oxide capacitance. This correlation can be explained by the existence of local regions with higher concentrations of Arsenic, which include as well the gate as the substrate (see figure 6). From modelling point of view this means that a correlation factor needs to be added to the right hand side of equation 3.

Figure 8 compares the influence of different halo implantation angles (35° and 45°) on threshold voltage roll-off and $1/\sqrt{WL}$ behaviour. It follows that in the case of a 45° implantation, a larger part of the halo is implanted through the gate, although the energies of the implants are the same. This shows that 45° is a preferred angle for shooting Arsenic through the examined poly-silicon material. This halo implantation condition should be avoided, because it results in a serious degradation of threshold voltage mismatch. In figure 8 it is also seen that when the 35° halo dose is decreased the long-channel threshold voltage and $A_{\Delta VT}$ decrease. This indicates that at 35° part of the halo is still implanted through the gate.

6. Conclusions

The threshold voltage mismatch of a 0.13 µm technology has been examined. The mismatch is caused by fluctuations in doping, interface charge and oxide thickness. These three mechanisms were separated by examining the bulk bias dependence. The correct doping profile, obtained by SIMS measurements, was used in the analysis. This lead to a 20-35 % lowering of the predicted doping fluctuation contribution and a 10-25 % lowering of the oxide thickness fluctuation contribution. The main part of the threshold voltage mismatch is caused by 'interface charge' fluctuations, for as well nMOS as pMOS transistors. For the case of the pMOS transistors this is caused by implanting a small part of the Arsenic halo through the gate. The fluctuation in this charge is not described by Poisson statistics, but it is due to the random character of the poly-silicon gate material. The halo also increases fluctuations in gate depletion, because it locally compensates the gate doping. Changing the halo implantation angle from 45° to 35° results in a significant decrease of threshold voltage mismatch. This shows that 45° is a preferred angle for implanting Arsenic through the gate. This implantation angle should therefore not be used at the investigated energies. However, also for the 35° angle the halo is still implanted through the gate. This effect has to be taken into account, when optimising modern CMOS technologies, since it results in a serious increase in threshold voltage mismatch.

The Authors acknowledge the support of IWT and Alcatel Microelectronics.

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