Investigations on Poly-SiGe gate in full 0.1µm CMOS integration

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Abstract

CMOS transistors down to 0.1µm gate length were successfully fabricated with polySiGe gate. Various germanium fractions (<25%) were investigated coupled with different gate doping impurities. We show that Arsenic can reduce the benefit of polySiGe in terms of dopant activation in the gate. However, we demonstrated that an optimum germanium fraction (20%) can reduce polydepletion in both nMOS and pMOS transistors. We also examined on the impact of polySiGe on the gate oxide reliability, showing that the oxide lifetime of devices integrated with a polySiGe electrode has been improved.

1 Introduction

With the scaling down of the MOS transistor toward deep submicron dimensions, new technological challenges emerge especially concerning the gate stack. Indeed, the polysilicon gate exhibits polydepletion that becomes a larger and larger fraction of the equivalent oxide thickness (EOT). Different solutions are proposed to deal with this phenomenon. First, the conventional approach is to maximise the dopant activation at the gate oxide interface (i.e. higher dopant dose and thermal budget). However, this is limited by the diffusion of dopants, especially at pMOS side where Boron is very likely to penetrate through the ultra thin gate oxide barrier into the substrate.

Introducing new gate materials is a mean to address this issue. Metal gate can suppress polydepletion and dopant diffusion, but mid-gap or dual metal gates also address new challenges such as buried channel (to lower Vt) [1,2] or technological issues (material availability, metal etching).

Poly-SiGe has been reported as a promising gate material due to its ability to increase the dopant activation and thus to reduce the polydepletion, especially on pMOS devices. Significant improvements were demonstrated in pMOS transistors for high germanium fraction (>30%) whereas, in the meantime, degradation was observed on nMOS devices for such germanium fractions [3,4]. Investigations on lower germanium fractions have shown promising results for full CMOS integration. All this is in line with [5,6] that reported worse arsenic and phosphorus deactivation in polySiGe than in polySi for high germanium fraction (Figure 1).

The gate oxide reliability is also a major concern for deep sub-micron technologies since the silicon dioxide, few monolayers thick, is reaching its limit. The gate oxide wear-out is now unequivocally found to be driven by electrodes either following the anode hole injection process or by the hydrogen release process depending on schools [7,8,9]. As a result, using polySiGe as a gate material may influence gate oxide lifetime.

In this paper, we present a full CMOS integration with polySiGe gate; the germanium fraction ranging from 0% to 25%. Different pre-doping and source drain implants conditions were investigated. We also show that an optimum germanium fraction can be found to reduce polydepletion and improve performances for both nMOS and pMOS transistors simultaneously. We also present investigations on the polySiGe impact on oxide lifetime.

2 Experimental

Five set of structure were compared in this study: All the structures were processed with a nitrided gate oxide (extracted EOT: 24Å, Fig.2), thermally grown. The reference set was gated with 1500Å of amourphous-Si whereas the four other set were gated with a bi-layer stack of 500Å of polySiGe completed by 1000Å of polySi in order to obtain a 1500Å high-gate, like the reference. We processed four different germanium fractions: 2.5%, 15%, 20% and 25%. The polySiGe was deposited by RTCVD with $SiH_4/GeH_4/H_2$, between 600and 650°C. As far as the gate pre-doping is concerned, nMOS gates were pre-doped with phosphorus 3e15at/cm², 25keV, whereas pMOS gates were split into pre-doped (boron, 2e15at/cm², 2keV**)** and unpre-doped devices. Transistors down to 90nm gate length were patterned. Arsenic and BF2 were used for respectively nMOS and pMOS extensions. Concerning nMOS devices, the Source/Drain were implanted either with Arsenic or with Phosphorus at 2e15at/cm², 15keV and 5keV respectively. To summary, the same dose of dopant species was implanted in the nMOS gate (5e15at/cm²) but either with Phosphorus only or with Phosphorus and Arsenic in order to investigate the behaviour of Arsenic activation within polySiGe. PMOS Source/Drain were implanted with boron at 3e15at/cm², 2keV for pMOS. The activation anneal was done at 1000°C, 15s. The source/drain junctions were Co-silicided in order to reduce the series resistances.

3 Electrical results

3.1 Polydepletion

In order to estimate the activation of dopant species in the gate with respect to the germanium fraction, we have plotted in Fig.3 the capacitance measured in inversion at Vdd on 100x100µm² devices. Indeed, the more the activation, the higher the capacitance in inversion. Concerning nMOS devices implanted with both Arsenic and Phosphorus, as expected, this capacitance is close to be constant (without any degradation). But we can see that using a full Phosphorus implantation leads to a better activation in the gate for the same dose implant. This shows that using Arsenic impurity in the gate can limit the activation gain expected in Fig.1 with full Phosphorus impurity. On pMOS side, unpre-doped devices exhibit a better Boron activation with germanium fraction higher than 20%. As expected, introducing the Boron pre-doping had improved the activation on all the samples.

Now, let us look at the polydepletion, estimated as the relative shift in gate capacitance between poly and metal gate, at Vdd). One can see in Fig.4 that a minimum of polydepletion seems to appear for a germanium fraction close to 20%, for nMOS devices. We can also add that no degradation of the polydepletion can be observed up to 25% germanium fraction.

Fig.4, where the polydepletion for pMOS devices is reported, shows that for germanium fraction higher than 15% percent we have reduced the polydepletion. Notice that, polySiGe gates were impacted more than polySi references by using Boron pre-doping. The depletion increase observed with the 2.5% germanium fraction is not explained so far.

These results demonstrate that an optimal germanium fraction can be found to reduce polydepletion on both nMOS and pMOS devices simultaneously. This germanium fraction is estimated at around 20%. But it is noticeable that the decrease of polydepletion in pMOS devices for such germanium fraction is not as high as the one reported in [1,10,11] for higher germanium fractions.

3.2 Transistors

In this study, we have performed CMOS transistors down to 0.1µm gate length. As suspected the devices with Phosphorus Source/Drain were not functional (high diffusion of Phosphorus in the channel) and so will not be presented here. Threshold voltages of polySiGe devices are plotted in the Figs.5 and 6. The Vt shift observed on polySiGe devices with germanium fraction higher than 15% is due to the polySiGe workfunction. This shift is limited in nMOS devices (50mV) whereas it is larger (100mV) at pMOS side. The pMOS Vt is also driven by the polydepletion reduction due to Boron pre-doping (about 25mV). This polydepletion decrease permits to reduce short channel effects as we can see in Fig.6.

Concerning performances, a slight gain is observed with polySiGe devices due to depletion reduction. The best results obtained for polySi reference and polySiGe gates are presented in the table.1. The best nMOS and pMOS transistors were obtained for 20%Ge, with Boron pre-doping for pMOS. Typical subthheshold characteristics of these devices are presented on Fig.7.

Table 1. Best results obtained for polySi reference and polySiGe devices, EOT=24Å, @ |Vdd|=1.2V, WxL=10x0.1µm²

	PolySi reference		PolySiGe	
	nMOS	pMOS	nMOS	pMOS
Ion (µA/µm)	537	179	610	211
Ioff (nA/µm)	20	0.035	22	0.1
Ion normalised @ Ioff=1nA	523	217	545	241
S (mV/dec)	77	77	80	81
Vtsat (V)	0.26	0.46	0.18	0.45

3.3 Oxide reliability

To check this point carefully, constant voltage stresses have been carried out on nMOS and pMOS in the accumulation regime using the same gate voltage whatever the germanium fraction.

No time to failure difference has been found for nMOS (Fig.8) and a slight but significant loss is noticed in the case of pMOS (Fig.9). Nevertheless, in both cases, the failure occurrence is very different as illustrated by the Fig.10.

In the case of polySi-gated devices the oxide breaks progressively as reported in [12]: after the so-called SILC phase, the current becomes noisy and increases continuously till it reaches the current compliance level.

On the contrary, in the case of the polySiGe-gated devices, the noisy behaviour is “annealed” after few seconds and the SILC phase continues as if the previous failure has never occurred. This behaviour can be repeated many times (Fig.3) before the final dramatic breakdown. Light emission microscopy observations have confirmed not only that opened spots are not optically active after the current noise vanishing but also that the active local spot is systematically different of the previous ones (not shown here).

Since we know that a device can undergo a quasi-breakdown and continue to work properly [13], it seems clear that the Weibull distributions shown in Fig.8 and 9 for polySiGe-gated devices do not reflect the real time to device breakdown.

At that point, we define a delay beginning at the first noisy behaviour and ending at the final breakdown. For nMOS, Fig.11 shows that the delay increases exponentially with the increasing germanium fraction. For a pMOS, the delay is so long that it cannot be measured within thousands of seconds (case of Fig.10).

First, this periodical noisy behaviour has nothing to do with electric breakdown depicted by Jackson et al

[14]. Indeed, all the experiments have been done using the same measurement equipment. Second, it does not reflect an increase of the wear-out conduction path progressiveness due to the germanium fraction since each event is localised on a different spot. Moreover each failure occurrence behaves progressively.

Nevertheless, according to Okada's work [15], this behaviour can be related to the density of latent defect and reflects the "breakdown path creation efficiency" that seems to be mainly influenced by the geranium included in the gate materials whatever the doping profile.

4 Conclusions

We demonstrated in this paper a full 0.1µm CMOS integration with polySiGe gate showing that an optimal germanium fraction can be found to improve both nMOS and pMOS devices. We have also shown that the Arsenic can limit this gain on nMOS side. Moreover, it seems now clear that gate material is a major issue for gate oxide reliability and especially polySiGe. Anyway further investigations should be carried out in order to confirm this behaviour and to quantify rigorously lifetime improvement.

5 References

[1] E. Josse *et al.*, ESSDERC2000, p.548
[2] B. Tavel *et al.*, ESSDERC2001, p. 151
[3] J.Alieu *et al.*, VLSI1998, p. 192
[4] J.Alieu *et al.*, ESSDERC1999, p. 152
[5] T.J. King *et al.*, *Trans. On Elec. Dev.*, vol. 41, pp. 1253-1262, 1994
[6] C. Salm *et al.*, *J. Electrochem. Soc.*, vol. 144, 1997
[7] Nicollian *et al.*, IRPS2000, p. 7.
[8] M. A. Alam *et al.*, IRPS2000, pp. 21-26.
[9] D. J. DiMaria *et al*, *J.Appl.Phys.*, vol. 73, pp. 3367-3384, 1993.
[10] Y. Ponomarev *et al.*, *Trans. On Elec. Dev*, vol. 47, pp.848-855, 2000
[11]W-C Lee *et al.*, VLSI1998
[12] F. Monsieur *et al*, IRPS2002 (to be published)
[13] T. Pompl *et al*, IRPS1999, pp. 82-87.
[14] J. C. Jackson *et al*, *Appl. Phys. Lett.*, vol. 71, pp. 3682-3684, 1997.
[15] K. Okada, *Jpn. J. Appl. Phys.*, vol. 36, pp.1443-1447, 1997.

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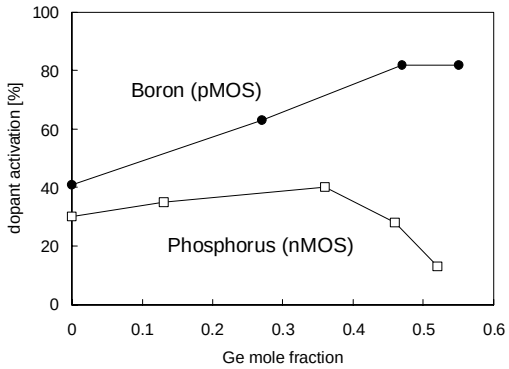


Figure 1: Dopant activation in the PolySiGe with respect to the germanium fraction. After T. King et al. IEEE TED 1994.

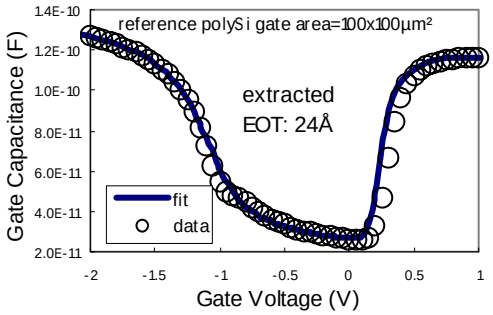


Figure 2: experimental and simulated CV curves of 100x100µm² nMOS transistor of reference split. Extracted EOT is 24Å.

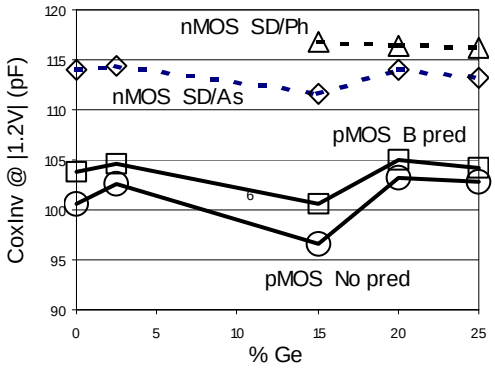
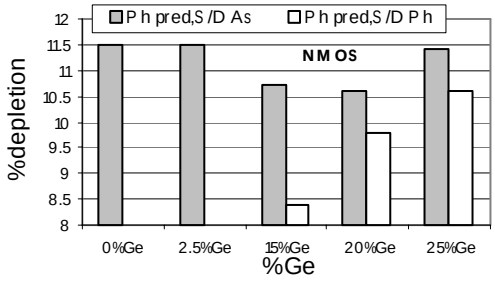


Figure 3: oxide capacitance in inversion versus the Ge fraction measured on 100x100µm² transistors, @ |Vg|=1.2V



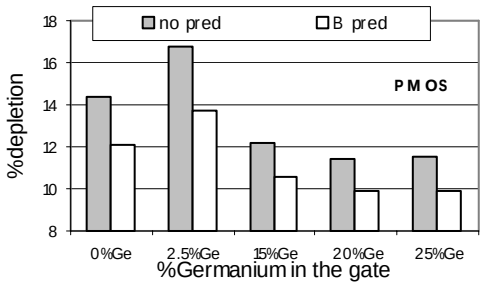


Figure 4: calculated depletion versus Ge fraction measured on 100x100µm² nMOS (above) and pMOS (below) transistors

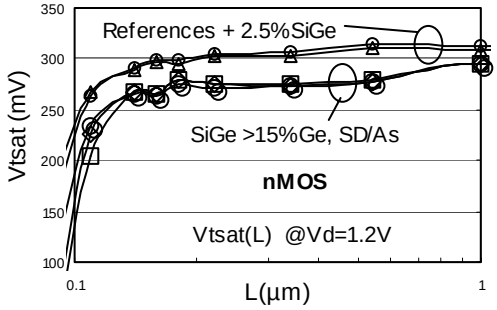


Figure 5: Saturation threshold voltage versus gate length of nMOS transistors for various Ge fraction

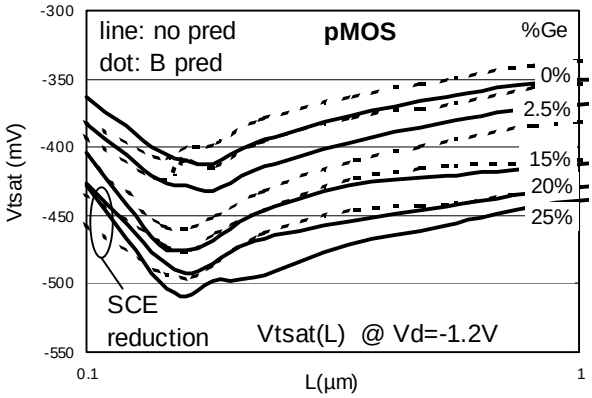


Figure 6: Saturation threshold voltage versus gate length of pMOS transistors for various Ge fraction

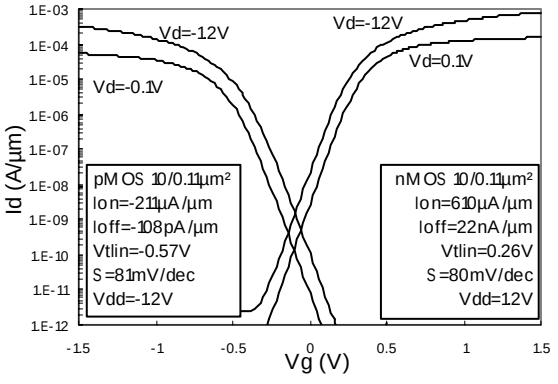


Figure 7: subthreshold characteristics of WxL=10/0.1µm² nMOS and pMOS transistor, EOT=24Å, 20%Ge, |Vdd|=1.2V

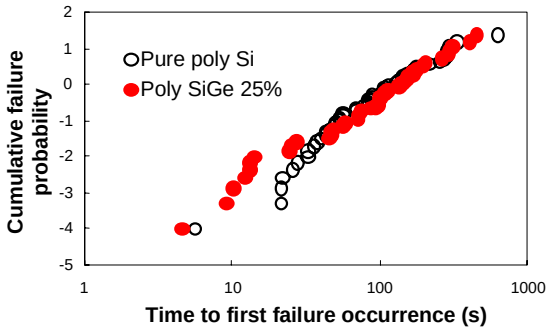


Figure 8: Time to first failure cumulative distributions obtained for different germanium fraction for nMOS in the accumulation regime (Vg=-3.7 V, Tox=20Å, T=25°C, A=10000µm²).

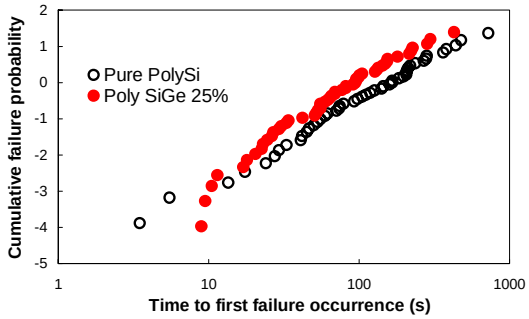


Figure 9: Time to first failure cumulative distribution obtained for different germanium fraction for pMOS in the accumulation regime (Vg=3.7 V, Tox=20Å, T=25°C, A=10000µm²).

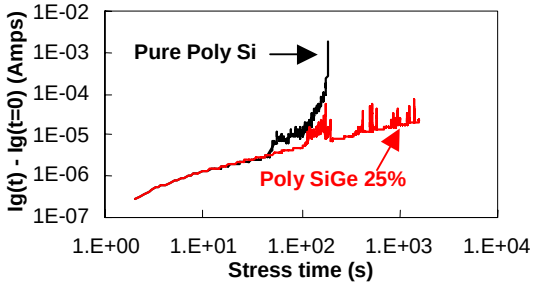


Figure 10: Constant Voltage stress carried out on pMOS in the accumulation regime (Vg=3.7 V, Tox=20Å, T=25°C, A=10000µm²).

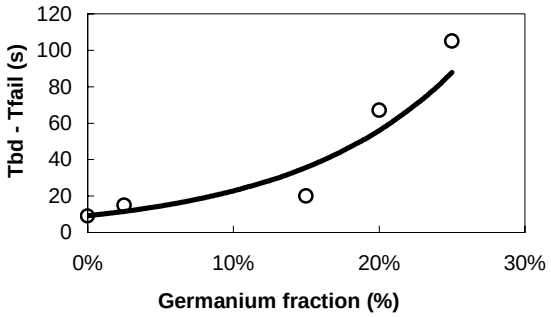


Figure 11: Delay between the first failure event (Fig.12) and the dramatic final breakdown event plotted with respect to the Ge fraction for nMOS in the accumulation regime.