Programming by Tunneling in Nanocrystal Memories

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Abstract

Si nanocrystals have been deposited onto oxidized Si substrates by chemical vapor deposition of SiH_4. The dots have been completely embedded into SiO_2 and used as floating gate of MOS memory devices. The tunneling of electrons through the gate stack, their trapping in the Si dots and detrapping, and their storage have been experimentally investigated. The results are shown and discussed.

1. Introduction

Nanostructures showing memory effects obtained by exploiting the storage of a few electrons have recently attracted much attention as promising candidates for the realization of future generations of memory arrays at high density and low power. Many approaches to realize such nanostructures have been proposed, based on chemical vapor deposition (CVD) of Si nanocrystals onto oxidized Si substrates [1], aerosol deposition [2], annealing of silicon rich oxide [3], ion implantation into SiO_2 of Si and Ge [4], Sb and Sn [5], and oxidation of SiGe alloys [6]. In the near term these devices appear also to be a very interesting approach for the scaling of flash memory devices [7].

We have realized MOS structures with Si nanocrystals deposited by CVD to investigate their potential as candidates for flash scaling [8]. In this paper we report some important aspects concerning the tunneling of electrons through the gate stack and their storage into the Si nanocrystals.

2. Experimental

MOS capacitors and n-channel MOSFETs with a gate dielectric stack consisting in a tunnel oxide of either 3 or 4 nm of thickness, Si nanocrystals, and a control oxide of either 7 or 8 nm of thickness were realized by a standard scaled CMOS process flow. The nanocrystals were formed by CVD of SiH_4 with H_2 as carrier gas at a pressure of 80 Torr and at temperatures in the range from 500 to 600 °C. The deposited dots, initially characterized by an amorphous structure, are crystallized by a rapid thermal annealing at 1000 °C, and they are then covered with a CVD control oxide.

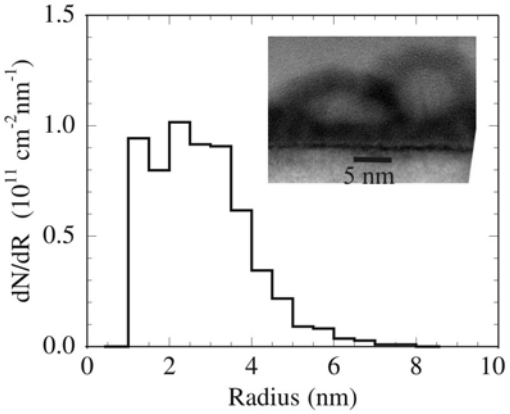

Figure 1. Si dot size distribution.

3. Results and discussion

Through CVD we have obtained nanocrystals well separated, of sizes of the order of a few nanometers, and densities from 3×10^{11} to 7×10^{11} dots / cm^2. Fig. 1 reports a typical distribution of grain radii, with a dispersion of the order of a few nm and a density of about 3×10^{11} dots / cm^2.

These structures are suitable to realize a memory. The inset of Fig. 2 shows a typical hysteresis of two high-frequency C-V characteristics of an MOS capacitor with Si nanocrystals performed after programming the device with a 1 s pulse at +5 V on the control gate and after erase with a 1 s pulse at –5 V. When the device is

subjected alternatively to such program and erase stresses for 100,000 times, no evident wearout is observed as far as the program/erase window is concerned, even though the MOS area is quite large and equal to 1×10^{-4} cm^2. This is shown in Fig. 2, which reports the capacitance measured at 0.24 V after each W or E pulse.

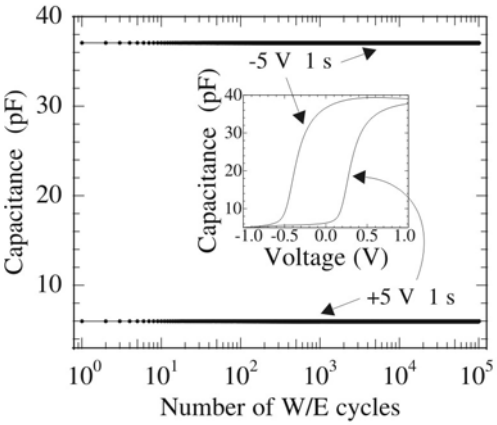

Figure 2. Endurance to W/E cycles.

Charge retention is quite good. Fig. 3 reports the time derivative of the threshold voltage (V_T) of nanocrystal memory cells with tunnel and control oxide of 4 nm and 8 nm, respectively, and with a 0.2×0.3 μm^2 gate area, programmed with $\Delta V_T = V_{TW} - V_{TE}$ up to ≈2 V. At room temperature, even when the charge level stored in the nanocrystals is quite high, the retention is well above many tens of hours and, by extrapolation, it is of the order of 1 month for $\Delta V_T \approx 0.5$ V. It is important to note that these are worst case evaluations since the reported dV_T/dt values are the initial rates. Anyway, to be compatible with the requirements of non volatile memories, the level of retention has to be further improved, but this should be feasible by simply increasing of a few angstroms the tunnel oxide thickness.

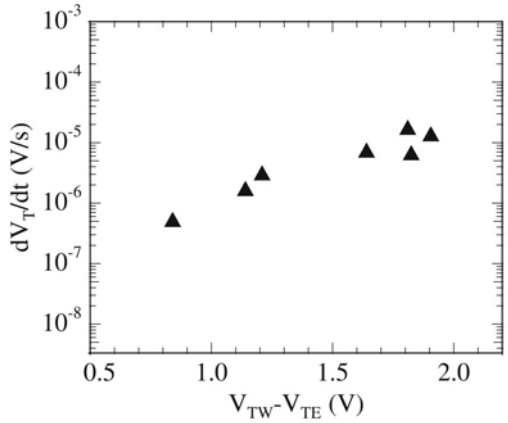

Figure 3. Charge retention (4 nm tunnel oxide).

These devices show peculiar characteristics when programmed by tunnel through the oxide. Fig. 5 shows a sequence of high-frequency C-V characteristics performed on a Si nanocrystal MOS capacitor of 10^{-4} cm^2 of area and with tunnel and control oxide of 3 nm and 7 nm of thickness, respectively. Si dot density and size distribution are as those shown in Fig. 1. The sequence of C-V curves is taken by first erasing the device with a pulse of –7 V of 5 s and then performing a program pulse on the control gate of 10 ms of duration to a voltage in the range from 5 to 9 V. In Fig. 4, each reported C-V curve is taken after an erase/program sequence. From the data it is evident that the curves shift toward higher voltages, as the program pulse bias increases. This corresponds to an increasing electron trapping in the dots with a clear saturation effect at the highest voltages. A systematic investigation of the programming characteristics, based on measurements such as those of Fig. 4, is reported in Fig. 5, with program pulses of duration in the range from 1 μs to 1 s. As expected, the flat band voltage shift increases as the program pulse increases in voltage level or in duration. But the data of Fig. 5 show also an evident saturation in the maximum value of flat band voltage shift and a large plateau at that level. The saturation ΔV_{FB} is at ≈ 0.5 V, i.e., in correspondence with about 5 electrons per dot. This maximum is observed in a wide range of voltages, for example, from 5 to 9 V in the case of program pulses of 1 s of duration. The plateau corresponds also to a steady-state condition in a wide voltage range. For example, note that between ≈ 7 V and ≈ 9 V, ΔV_{FB} is at the maximum of ≈ 0.5 V for both 1 s and 0.1 s program pulses. So this value, of the order of about 5 electrons per dot, appears to be not only the maximum charge level that can be stored in the system but also a steady-state condition which can be reached in a wide range of program voltages. For the application of this system to the realization of a memory, the presence of such a wide plateau is a very useful feature, since the system is naturally bi-stable, i.e. either neutral or charged to a level corresponding on average to a fixed small number of electrons per dot.

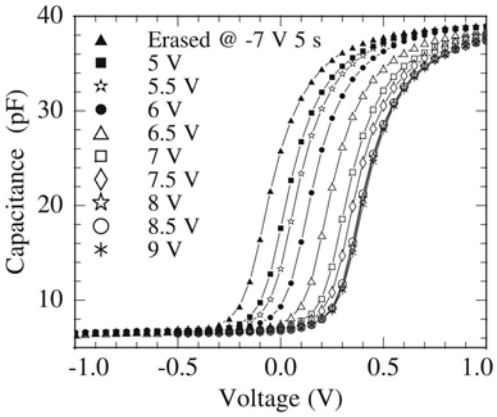

Figure 4. Programming with 10 ms pulses.

We would like now to discuss possible reasons for the observed behavior in the programming curves.

Also in standard floating gate memories programmed by channel hot electron injection there is a critical threshold voltage shift at which the program efficiency drops down [9]. The explanation for such decrease is that in correspondence with the critical shift the floating gate bias becomes equal to the drain voltage and this reduces to zero the field which pushes the channel hot electrons towards the floating gate.

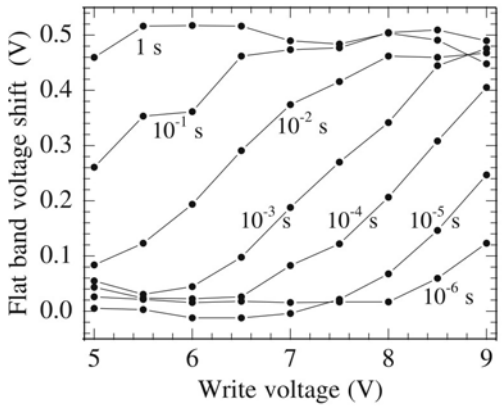

Figure 5. Programming curves (3 nm tunnel oxide).

In the case of programming by tunnel one also expects to reach a maximum threshold voltage shift. This effect can be understood by considering the continuity equation applied to the charge stored on the floating gate Q_{FG} and the current densities J_1 and J_2 through the tunnel and the control oxide, respectively [10]. Fig. 6 shows a sketch of the band diagram of the gate stack with the relevant currents. For low write voltages J_2 is negligible and J_1 dominates. Therefore Q_{FG} is simply the integral of J_1 over time.

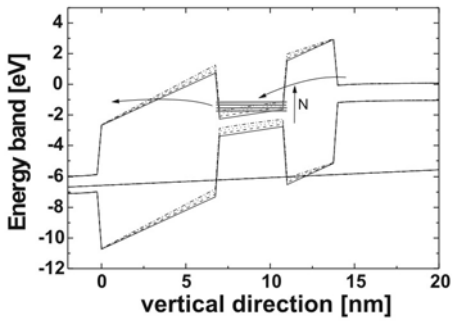

Figure 6. Band diagram of the gate stack.

When the program voltage is high enough, J_2 is not anymore negligible and the maximum stored charge is obtained for voltage drops V_1 and V_2 such that J_1 is equal to J_2 (i.e., in correspondence with the steady-state). From these considerations it results then that Q_{FG} at low programming voltages is an increasing function while at high voltages it decreases. This produces a maximum whose shape is quite sharp compared to the flat plateau that we observe experimentally. In the case of nanocrystal memories, this floating gate model should be corrected as proposed in [11], in order to take into account that the nanocrystals cover only a fraction of the total gate area. We have calculated ΔV_{FB} as a function of the program voltage by using the procedure of [12] to compute J_1 and J_2, by assuming a Si-SiO_2 barrier height equal to 3.15 eV for both J_1 and J_2, and by correcting ΔV_{FB} as proposed in [11] for the area fraction covered by the nanocrystals. The results are shown in Fig. 7. The curves on the left side are calculated in the case in which J_1 dominates and for a program time of 1 s. The labels "maximum" and "minimum shift" refer to whether the charge trapped in the dots is neglected or not to compute the voltage. The curve on the right side of Fig. 7 shows the steady-state. By considering together the various curves, the overall behavior is therefore expected to exhibit a quite sharp peak, contrarily to what shown by the data of Fig. 5, characterized by a wide plateau for a program time of 1 s. This model however provides some valid indications when considered in a wider range of voltages, since it is in good agreement with the data taken in a larger voltage range [8] for what concerns the initial increase at low program voltages and the final decrease at high voltages.

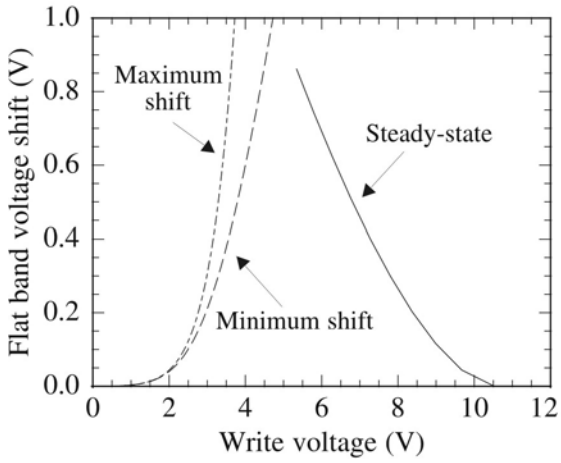

Figure 7. Programming curve expected for the case of Fig. 5.

Therefore, in order to explain the presence of the plateau in the programming curve we have to consider other effects, which would lead to an almost constant saturation flat-band voltage shift ΔV_{FB} in a wide range of write voltage. Here, we propose three mechanisms that may be responsible for such a behavior: (a) Coulomb blockade, (b) dependence of the capture cross section on trapped charge and field, (c) deep levels at the nanocrystals-SiO_2 interface.

1. Coulomb Blockade. First, we discuss single electron charging of each dot. The addition energy classically is equal to q^2/C, where q is the electron charge and C is the total capacitance of the dot. From a 3D solution of the coupled Poisson and Schrödinger equation in 3D [13] we obtain that addition energy of the dot in our case is about 150 mV. The band profile in the vertical direction, obtained from an equivalent 1D

solution of the Poisson-Schrödinger equation in the vertical direction, is plotted in Fig. 6 for a number of electrons ranging from zero to three. As a simplifying assumption, we discard the dot-dot interaction, which is significantly screened by the channel and the gate, and consider each dot as independently and individually charged. It is clear from Fig. 6 that as the dot is charged, the capture rate *g* from the channel to the dot decreases in steps, while the emission probability *r* increases in steps. In Fig. 8 we plot the normalized emission/capture ratio *[r(N+1)/g(N)]/[r(1)/g(0)]* as a function of the write voltage for a number of electrons *N* in the dot ranging from 1 to 5, computed with a model proposed in [14]. On average, in the considered voltage range, the emission/capture ratio increases by one order on magnitude per trapped electron.

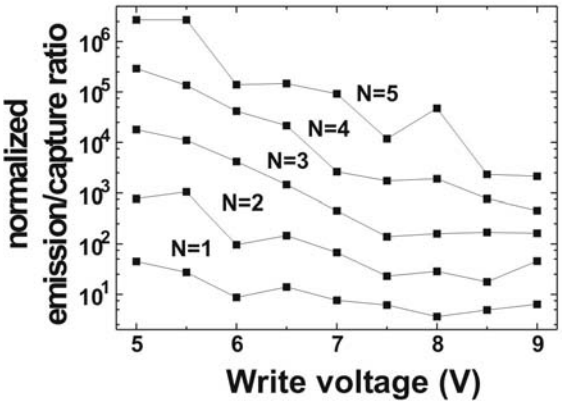

Figure 8. Normalized emission/capture ratio as a function of the program voltage for a number of electrons in the dot ranging from 1 to 5.

2. Decrease of the capture cross section with trapped charge. It is well known in the case of oxide traps, that the capture cross-section decreases of several orders of magnitude as the trap charge state goes from attractive (positively charged), to neutral, to repulsive (negatively charged) [15]. In addition, as the number of trapped electrons N increases, we have an increase of the electric field from the dot to the gate. Then, an additional electron entering the dot, has an increased probability of being emitted to the gate instead of relaxing to the dot ground state.

3. Trap states at the Si/SiO_2 interface. It has been suggested by some authors [16,17] that electrons can get trapped in deep levels at the interface between the nanocrystal and SiO_2, instead of *in* the nanocrystals. This mechanism would naturally lead to a saturation of ΔV_{FB}, once all trap levels are filled. On the other hand, the good quality of the C-V curves (such as those shown in Figs. 2 and 4), the steep subthreshold slopes of the memory cell transcharacteristics, and the good symmetry found between write and erase characteristics, let us think that the quality of the nanocrystal-SiO_2 interface in our samples is significantly better than that considered in [16,17].

4. Summary

In this paper we have shown that Si nanocrystal memories, characterized by promising features concerning the endurance to write-erase cycling and the charge retention even with a tunnel oxide thickness of 3-4 nm, show programming curves with a wide voltage plateau. This suggests that the system is intrinsically bi-stable, i.e., either with zero or with a fixed small number of electrons per dot. As discussed in the last part of the paper, this plateau is most likely the consequence of the small size of the dots which store the charge. Further investigation, by means of experiments and modeling, is needed to understand which is predominant among these proposed effects: all may lead to saturation of ΔV_{FB}, but at the moment it is difficult determine which one is in quantitative agreement with the experimental results.

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