Temperature-Independence-Point Properties for 0.1μm-Scale Pocket-Implant Technologies and the Impact on Circuit Design

K. Hisamitsu, T. Yamaoka, M. Tanaka, D. Kitamaru,
H. Ueno, M. Miura-Mattausch, H.J. Mattausch[1], N.D. Arora[2],
S. Kumashiro[3], T. Yamaguchi[3], K. Yamashita[3], and N. Nakayama[3]
Grad. School of Adv. Sciences of Matter, [1]*Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, 739–8526, Japan*
[2]*Simplex Solutions, Inc. 521 Almanor Avenue, Sunnyvale, CA 94086, USA*
[3]*Semicon. Tech. Academic Research Center, 3-17-2, Shin Yokohama, 222-0033, Japan*
Email:hisamitu@hiroshima-u.ac.jp

Abstract

The temperature-independence point (TIP) of the drain current for MOS transistors in a 0.1μm-scale pocket-implant technology is gate-length ($L_{\rm g}$) dependent and has different magnitudes for n-MOSFET (0.45V – 0.57V) and p-MOSFET (0.69V – 0.77V). Circuits such as ring-oscillators have a TIP, lying between the values for n- and p-MOSFET, which is dominated by the n-MOSFET TIP for long $L_{\rm g}$ and by the p-MOSFET TIP for short $L_{\rm g}$. Due to the high field effect, oscillation periods of ring-oscillators with short $L_{\rm g}$ hardly improve, when the supply voltage is raised beyond the TIP. These observations suggest that an advantageous supply-voltage ($V_{\rm DD}$) choice for pocket-implant technologies is near the TIP of circuits, allowing a favorable combination of short switching delay, minimized temperature dependence and low power dissipation.

1. Introduction

It has been observed that the delay characteristics of ring-oscillators for different temperatures cross at certain applied voltages ($V_{\rm DD}$). We call the voltage point, at which the temperature dependence vanishes, the temperature-independence point (TIP). The importance of the TIP has been recognized since long time for analog designs, where minimized temperature dependence is often desired. The TIP is generally expected to occur at the rather high voltage of 1.2V [1]. An instability concern for low-voltage LSIs with a $V_{\rm DD}$ lower than 1.2V has thus recently been raised, because such LSIs would have to operate in the region of a positive temperature coefficient [2]. Fig. 1 compares oscillation periods of ring-oscillators fabricated with two differnt gate lengths ($L_{\rm g}$) in a 0.1μm technology for various temperatures. As can be seen in Fig. 1 the TIP is in general small enough to relieve instability concerns for low-voltage designs contrary to the previous result [2].

Two feature are obvious from our measurement:

1) The ring-oscillator TIP for short $L_{\rm g}$ is higher than that for long $L_{\rm g}$.
2) Contrary to long $L_{\rm g}$, the oscillation period is hardly improved under the $V_{\rm DD}$ >TIP condition for the short $L_{\rm g}$.

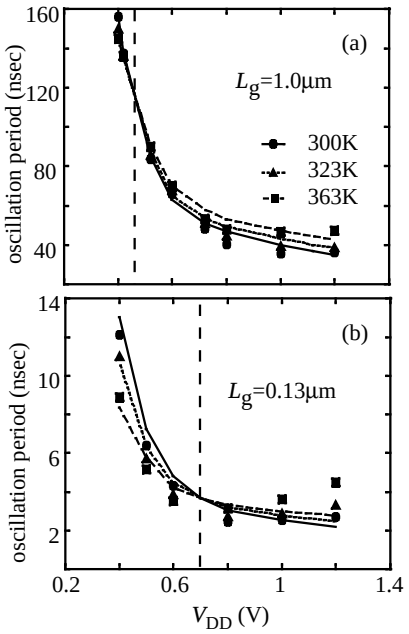

Figure 1. Measured (symbols) and simulated (lines) oscillation period of a ring-oscillator with 31 inverter stages. (a) $L_{\rm g} = 1.0\mu$m, (b) $L_{\rm g} = 0.13\mu$m.

Here we report an analysis of the TIP properties of a ring-oscillator together with those of n- and p-MOSFETs by measurements and simulation for a 0.1μm-scale CMOS technology with pocket-implants [3]. The circuit TIP of ring-oscillators ranges 0.5V – 0.7V for different $L_{\rm g}$, and shorter $L_{\rm g}$ result in a higher TIP. The origin is a different temperature-dependence change of the transistor TIPs for n- and p-MOSFETs as a function of $L_{\rm g}$. This is

caused by a different temperature dependence of electron and hole mobility.

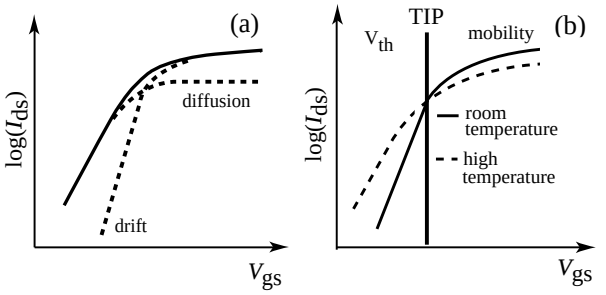

Figure 2. (a) Drift- and diffusion components of $I_{\rm ds}$ as a function of the gate voltage ($V_{\rm gs}$); (b) Schematic temperature dependence of I-V characteristics. A region with minimized temperature dependence and a temperature independence point (TIP) exist due to the different signs of the temperature coefficients of the current components.

2. Characteristics of Temperature-Independence Point (TIP)

The source-drain current ($I_{\rm ds}$) of MOSFETs is well known to consist of a drift-component ($I_{\rm ds}({\rm drift})$) and a diffusion component ($I_{\rm ds}({\rm diff})$), which have different temperature coefficients and are dominant in different operating regions [4]. $I_{\rm ds}({\rm diff})$ dominates in the sub-threshold and weak-inversion region, as shown in Fig. 2a. It has a positive temperature coefficient due to the bandgap narrowing, and therefore induces a threshold-voltage ($V_{\rm th}$) decrease with increasing temperature. On the other hand, $I_{\rm ds}({\rm drift})$ dominates in the main part of the linear region as well as in the saturation region and has a negative temperature coefficient. The reason is a carrier mobility decrease with temperature due to an increased phonon scattering. Consequently, the overall temperature dependence of $I_{\rm ds}$, schematically shown in Fig. 2b, has an intermediate region of minimized temperature dependence.

$V_{\rm th}$ of n- and p-MOSFET are designed to be 0.17V and 0.3V for long $L_{\rm g} = 1.0\mu$m as well as 0.30V and 0.38V for short $L_{\rm g} = 0.13\mu$m. Fig. 3a and b show the temperature dependence of the $I_{\rm ds}$-$V_{\rm gs}$ characteristic of n- and p-MOSFET for $L_{\rm g} = 1.0\mu$m at $V_{\rm ds}$=1.0V. Fig. 4a and b show this temperature dependence for $L_{\rm g} = 0.11\mu$m. The TIP is clearly observed for all cases, but occurs at different magnitudes of $V_{\rm gs}$ for changed $L_{\rm g}$ as well as for n-MOSFETs (0.45V – 0.57V) and p-MOSFETs (0.69V – 0.77V). Lines show the simulation results with the drift-diffusion model for circuit simulation HiSIM (Hiroshima-university STARC IGFET Model) [5, 6], which reproduce the measured temperature and $L_{\rm g}$-dependence of the TIP with good accuracy. Fig. 5 summarizes the $L_{\rm g}$-dependence of the TIP for n- and p-MOSFET as well as the ring-oscillator. The analyzed ring-oscillator circuits consist of 31 inverter stages with a width ($W_{\rm g}$) of 10μm and 5μm for p- and n-MOSFETs. The increase with decreasing $L_{\rm g}$ for both MOSFET types is attributed mainly to the $V_{\rm th}$-increase due to the reverse-short-channel effect (RSCE) caused by the pocket implantation.

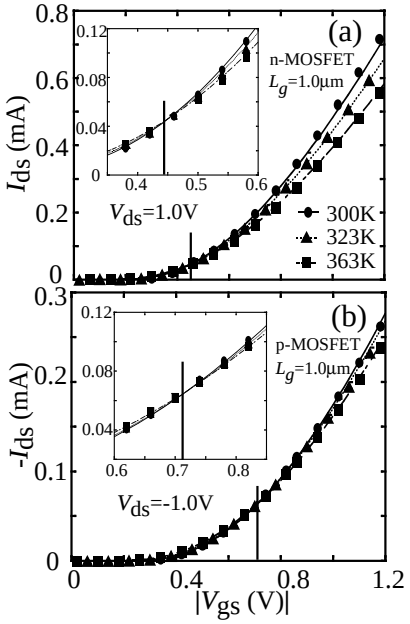

Figure 3. Temperature dependence of the I-V curves of (a) n-MOSFET ($W_{\rm g} = 5\mu$m) (b) p-MOSFET ($W_{\rm g} = 10\mu$m) as a function of the gate voltage ($V_{\rm gs}$) for $L_{\rm g} = 1.0\mu$m. Measured data (symbols) and simulated data with HiSIM (lines) are shown.

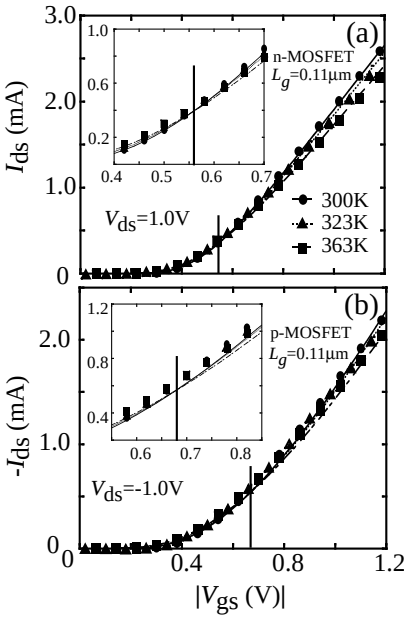

Figure 4. Temperature dependence of the I-V curves of (a) n-MOSFET ($W_{\rm g} = 5\mu$m) (b) p-MOSFET ($W_{\rm g} = 10\mu$m) as a function of the gate voltage ($V_{\rm gs}$) for $L_{\rm g} = 0.11\mu$m. Measured data (symbols) and simulated data with HiSIM (lines) are shown.

The simulated ring-oscillator oscillation periods with HiSIM are depicted together in Fig. 1a and b for the long $L_{\rm g} = 1.0\mu$m and the short $L_{\rm g} = 0.13\mu$m, respectively. Fig. 5 shows a continuous ring-oscillator TIP increase with decreasing $L_{\rm g}$ from about 0.45V for $L_{\rm g} = 1.0\mu$m to 0.7V for $L_{\rm g} = 0.13\mu$m. The ring-oscillator TIP is near to the n-MOSFET TIP for long $L_{\rm g} = 1.0\mu$m. For shorter $L_{\rm g}$ it changes its relative position and gets close to the p-MOSFET TIP at $L_{\rm g} = 0.13\mu$m. This suggests that we have a change from a n-MOSFET domination at long $L_{\rm g}$ to a p-MOSFET domination at short $L_{\rm g}$. The $V_{\rm ds}$ dependence of the TIP is very small as verified in Fig. 6 for n-MOSFETs of short and long $L_{\rm g}$ as a function of $V_{\rm ds}$. After a small increase at the beginning the TIP saturates to a constant value above $V_{\rm ds}$=0.25V. Therefore we can exclude the responsibility of the short-channel effect for the change from n-MOSFET to p-MOSFET domination here.

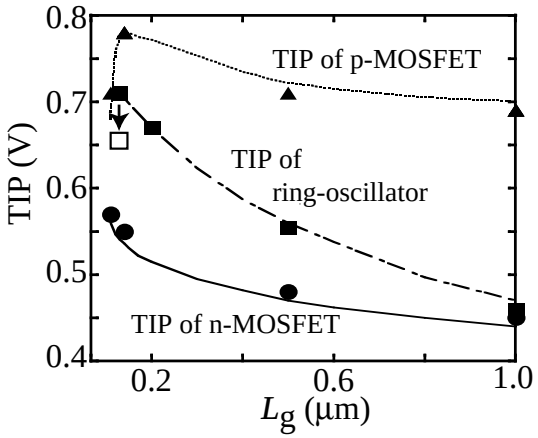

Figure 5. Measured (symbols) and simulated (lines) temperature-independence points (TIP) of n- and p-MOSFET as well as a ring-oscillator circuit as a function of $L_{\rm g}$. Simulations are with HiSIM.

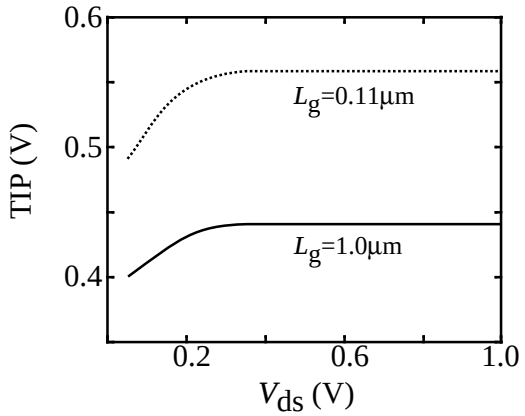

Figure 6. Drain voltage ($V_{\rm ds}$) dependence of the TIP for n-MOSFETs with HiSIM.

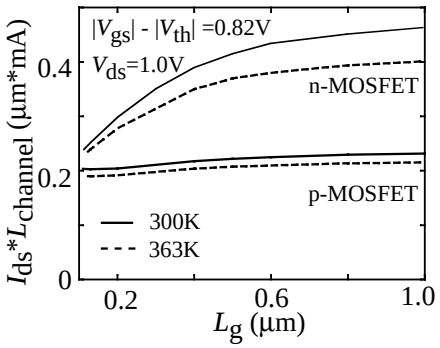

Figure 7. Measured $I_{\rm ds}$ normalized with the channel length ($L_{\rm channel}$) as a function of $L_{\rm g}$. $W_{\rm g}$ is fixed to 10μm for both cases.

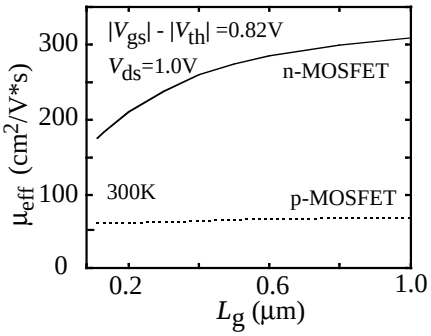

Figure 8. Extracted mobility values with HiSIM as a function of $L_{\rm g}$ for n- and p-MOSFET.

Fig. 7 verifies that the normalized $I_{\rm ds}$ at $V_{\rm ds} = 1$V decreases by more than a factor 2 for the n-MOSFET while it remains almost constant for the p-MOSFET, when $L_{\rm g}$ is reduced from 1.0μm to 0.13μm. The reason for the $I_{\rm ds}$ reduction of the n-MOSFET is attributed to the strong electron mobility degradation with decreasing $L_{\rm g}$ due to the high-field effect, as verified in Fig. 8. The temperature dependence of the high field mobility $\mu_{\rm eff}$ is stronger suppressed than that of the low field mobility μ_0 as demonstrated in Fig. 9. For the low field mobility the phonon scattering is dominant and induces a strong temperature dependence. The influence of the saturation velocity on the high field mobility results in the suppression of its temperature dependence. This is also responsible for the observed smaller temperature dependence of n-$I_{\rm ds}$ at short $L_{\rm g}$ in Fig. 7. The p-MOSFET is stronger influenced by the surface-roughness scattering than the n-MOSFET, and the surface-roughness scattering is independent of temperature, resulting in the weak temperature dependence of the p-MOSFET for all $L_{\rm g}$.

For long $L_{\rm g}$ the temperature dependence of n-$I_{\rm ds}$ is much larger than that of p-$I_{\rm ds}$ (see Fig 7), which explains the n-MOSFET determination of the ring-oscillator TIP in Fig 5. For short $L_{\rm g}$ the temperature dependence of n-$I_{\rm ds}$ and p-$I_{\rm ds}$ become approximately equal. The determination of the ring-oscillator TIP by the p-MOSFET is

now due to the low inverter-switching threshold, demonstrated in Fig. 10 by a solid circle. This low inverter-switching threshold is caused by a smaller $V_{\rm th}$ of the n-MOSFET in comparison to the p-MOSFET. Indeed, the inverter switching-threshold rises if we choose the same $V_{\rm th}$ for n- and p-MOSFET, as shown in Fig 10 by an open circle, and the TIP of the ring-oscillator moves to the middle as shown in Fig. 5 by an open box with an arrow.

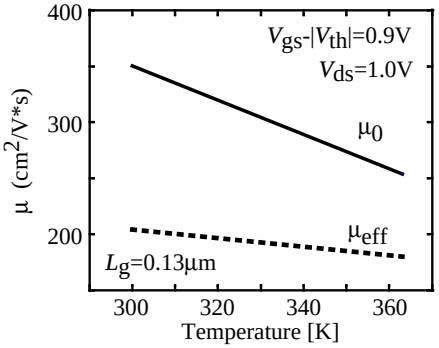

Figure 9. Extracted mobility values of a n-MOSFET with HiSIM as a function of temperature.

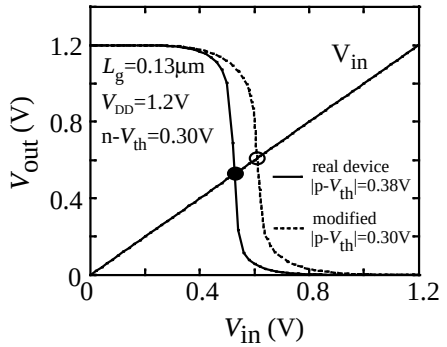

Figure 10. HiSIM simulation of the switching threshold voltage of CMOS inverters through a change of the p-MOSFET $V_{\rm th}$.

3. Discussion

Requirement of low-voltage application is serious for 0.1μm-scale MOSFETs and leads to the necessity of a low TIP. However, the high TIP of p-MOSFETs, which originates from the strong influence of the surface-roughness scattering on the hole mobility, hinders the reduction of $V_{\rm DD}$. One possible solution is to design the $V_{\rm th}$ of the p-MOSFET (p-$V_{\rm th}$) lower than that of the n-MOSFET. Another possibility is to redesign the width ratio between n- and p-MOSFETs in CMOS gates. Reduction of the conventional width ratio of $1:2$ to $1:1$ at shorter $L_{\rm g}$ is a possibility. The reduction of the width has the important advantage of a faster layout-density increase than expected from the $L_{\rm g}$ reduction. To keep the inverter-switching voltage at $V_{\rm DD}/2$, this reduction is efficient. However, the reduction of the TIP for the ring-oscillator cannot be realized. This can be done only by reducing the p-$V_{\rm th}$.

Important is also the fact that the delay hardly improves beyond the TIP for $L_{\rm g} = 0.13\mu$m, while the improvement is still substantial for $L_{\rm g} = 1.0\mu$m. This is attributed to the high-field effect for short $L_{\rm g}$, which prevents further carrier velocity increase as applied voltage becomes larger. These observations suggest, that the TIP may be an optimum design point for optimizing advanced pocket-implant technologies, to combine short delay, minimized temperature dependence and low power dissipation.

4. Conclusion

It is found that the transistor TIPs for a 0.1μm-scale CMOS technology with pocket implants are at about a factor 2 to 2.5 above threshold, are $L_{\rm g}$-dependent and have different magnitudes for n-MOSFET and p-MOSFET. The measured values range from 0.45V – 0.57V for the n-MOSFET and from 0.69V – 0.77V for the p-MOSFET. Circuits such as e. g. a ring-oscillator are found to have a TIP (0.5V – 0.7V), which lies between the TIP-values of n- and p-MOSFET, being dominated by the n-MOSFET TIP for long $L_{\rm g}$ and the p-MOSFET TIP for short $L_{\rm g}$.

The low circuit TIP-values are very favorable for low-voltage applications, relieving the concern of circuit operation with a positive temperature coefficient as well as the possibility of thermal instabilities [2]. Furthermore, the ring-oscillator oscillation period for short $L_{\rm g}$ hardly decreases, in contrast to long $L_{\rm g}$, when the supply voltage is raised beyond the TIP.

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