Suitability of Scaled SOI CMOS for High-frequency Analog Circuits

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Abstract

In this paper we show that the ability of SOI NMOS transistors to function as high-bandwidth amplifiers continuously improves as gate length shrinks below 50 nm. f_T of 196 GHz is achieved at Lpoly = 47 nm. Neither the transconductance nor the input capacitance reaches a limiting value at Lpoly = 47 nm. The gate sheet resistance, which influences the FET input resistance and high-frequency noise, shows little variation and is an acceptable value (7 Ω/square) in the Lpoly = 55 nm to 77 nm range.

We also present four features of an aggressively scaled 0.13-μm partially-depleted SOI CMOS technology that show its suitability for high-frequency circuit applications: RF noise performance comparable to state-of-the art III-V devices, body-tied SOI FETs that achieve the same low-frequency noise as bulk FETs, a multilevel back-end that allows high-density and high-Q passives, and negligible floating-body-induced jitter in RF circuits.

1. FET scaling

It has been shown that the gate delay of scaled CMOS technology continuously decreases as transistor gate length decreases in the 45 nm to 70 nm regime [1]. However, such behavior would be observed even if punchthrough and poor channel control occurred at the shortest gate lengths. In order for high-frequency analog circuits to benefit from scaling, the transconductance and other small-signal parameters must improve as gate length decreases. To date, the opposite has been reported: a decrease in transconductance at gate lengths below 80 nm was presented in [2]. Below we present data to support a claim that high-frequency analog circuits benefit from FET scaling.

We measured the S-parameters of four NFETs from a 0.13-μm partially depleted SOI CMOS technology [3] ranging in gate length from 47 nm to 72 nm. Each device consisted of 64 fingers, each 1.24 μm long. The unity current-gain frequency (f_T), transconductance (g_m) and input capacitance (C_{in}) were extracted from their respective de-embedded small-signal parameter (H_{21}, Y_{21} and Y_{11}) in the frequency range 2 GHz to 20 GHz, over which each parameter had the ideal slope. The results are shown in figures 1 through 3. None of the small-signal parameters reaches a limiting value at the smallest gate length of 47 nm. The input capacitance shows a tendency to saturate at even lower gate lengths, due to finite gate fringing capacitance. The transconductance shows no sign of saturation, indicating that the gate has good control of the channel, and that the effective velocity of electrons in the channel increases with increasing lateral electric field, even at high drain voltage (1.2 V). The f_T of 196 GHz at the shortest gate length is the highest ever reported for a silicon FET with acceptable short channel effect [2].

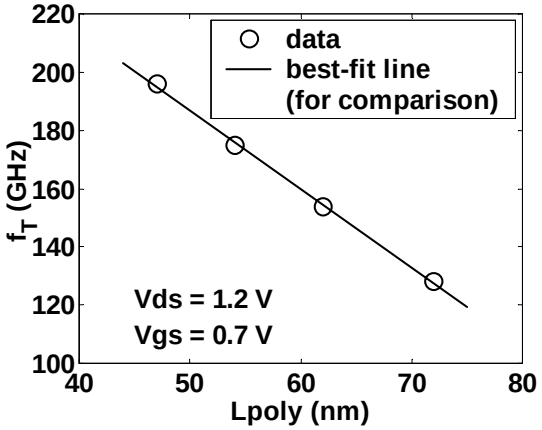

Figure 1. Cutoff frequency vs. poly gate length.

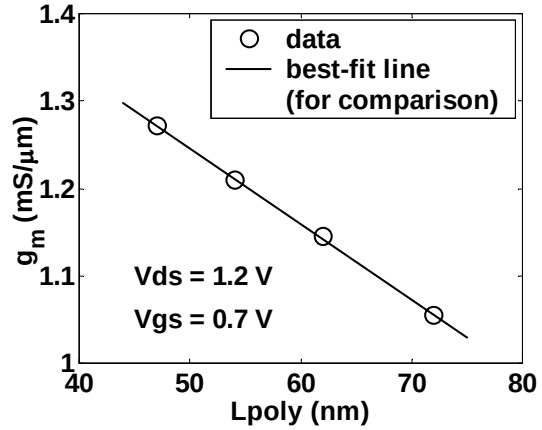

Figure 2. Transconductance vs. poly gate length.

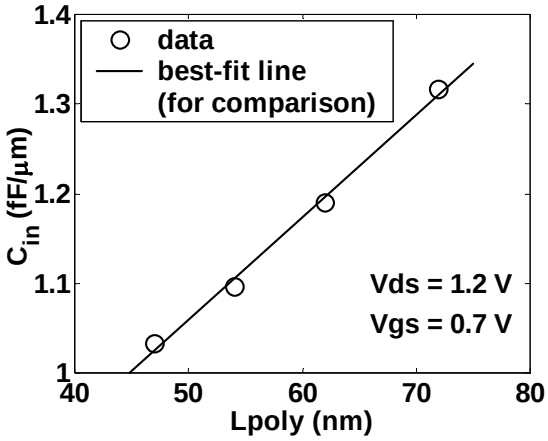

Figure 3. Input capacitance vs. poly gate length.

No discussion of the small-signal parameters of FETs would be complete without a discussion of the maximum frequency of oscillation, f_{max}. This is perhaps the most difficult parameter to measure accurately, because it requires accurate measurement of a very low input resistance (~ 1 Ω) which is in series with the high-impedance input capacitance (~ 90 fF). The theoretical RC time of the input corresponds to a frequency above 1 THz, which means the input resistance is not resolvable in the frequency range accessible to basic equipment (< 20 GHz), and can be distorted by small calibration errors and contact resistance in higher-frequency systems.

We extracted the unilateral power gain from our S-parameter data, and found that it had greater than the ideal 20 dB per decade slope over all frequencies in the 2 GHz to 110 GHz range. No simple FET model can produce this behavior, thus we refrain from stating a measured f_{max} value. However, at 20 GHz, a frequency at which calibration is usually reliable and the unilateral gain can be measured precisely, every FET has a unilateral power gain greater than 20 dB, indicating that f_{max} is probably greater than 200 GHz for every FET. More study is needed of calibration techniques and the dependence of f_{max} on transistor layout to make accurate f_{max} measurement possible.

One possible limiting factor of the f_{max} of scaled FETs is the resistance of the gate's silicide. In [4] it was reported that gate sheet resistance is an increasing function of gate length at drawn gate lengths near 180 nm. It was also shown through process simulation that silicide resistance is the dominant input loss mechanism in the same gate length regime. We measured the gate resistance on FETs with high, easily-measurable total gate resistance (~ 150 Ω) to investigate the gate-length dependence of silicide sheet resistance at gate lengths below 100 nm. The results are shown in figure 4. The measured resistance is effectively constant below 20 GHz, as expected, reflecting accurate measurement. The rolldown in the gate resistance above 20 GHz is either due to parasitic inductance or inaccurate calibration. The sheet resistance is 6.3 Ω/square at a gate length of 77 nm and rises to 7.3 Ω/square at a gate length of 55 nm. This sheet resistance increase is moderate enough to allow aggressively scaled FETs to have very high f_{max}.

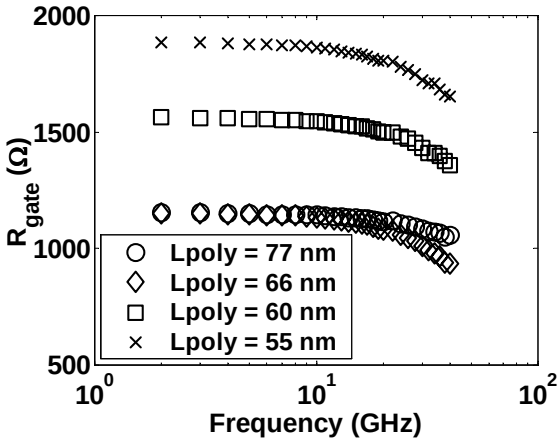

Figure 4. Gate resistance vs. frequency as measured on monitor structures (W=14 μm).

2. RF noise parameters

For the detection of low-amplitude signals, RF noise and gain are the most important figures of merits. We measure an NFET with Lpoly of 65 nm to have a minimum noise figure NFmin less than 2 dB up to 26 GHz (see figure 5). We also measure an associated gain of 19 dB at 2 GHz. These data are the best ever reported for a silicon technology and are similar to that of a state-of-the-art PHEMT. For example, at 12 GHz, the PHEMT ATF-36077 [5] exhibits a 0.5 dB NFmin and an associated gain of 12 dB, versus 1 dB and 14.5 dB, respectively, for our NFET.

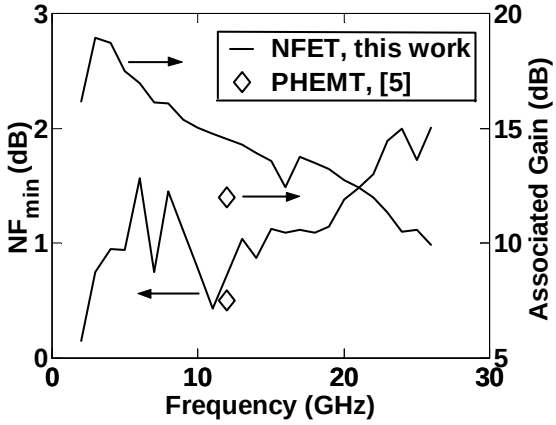

Figure 5. Noise figure and associated gain of an NFET (Vgs = 0.6 V, Vds = 1.2 V, Lpoly = 65 nm) and a PHEMT [5].

3. Low-frequency noise

Low-frequency noise is an important figure of merit for analog circuit designers since it impacts the jitter of VCOs and the charge pump of PLLs. The high nitrogen content of the thin gate oxide of scaled CMOS is known to increase low-frequency noise [6]. Designers can take advantage of the thick (Tinv = 2.9 nm) dual oxide offered in our technology, which has lower 1/f noise than the standard oxide due to its different nitrogen distribution. As shown in figure 6, the measured 1/f noise of a thick-oxide NFET with its body tied to ground is 3x lower than the noise reported for the thick-oxide (7.0 nm) NFET of a 0.18-μm bulk technology [7]. The comparison is fair because the 4x difference in active area is compensated by the 2x difference in current. This demonstrates that oxides with low 1/f noise and aggressively scaled oxides can be integrated, despite increased nitrogen content.

The drain-body diode current of floating-body SOI FETs is known to be a distinct source of low-frequency noise [8]. This noise can be avoided by using devices with body contacts. The noise shown in figure 6 lacks a component with the Lorentzian frequency dependence that is the signature of diode-induced noise. This shows that our SOI technology offers FETs with 1/f noise as good or better than that of bulk FETs.

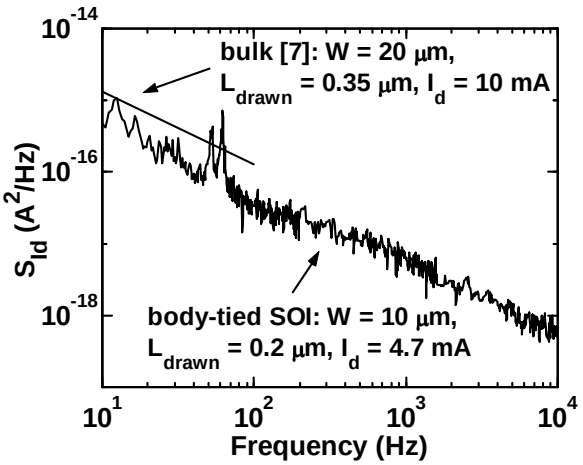

Figure 6. Drain-current noise of a thick-oxide, body-contacted NFET and the thick-oxide NFET of a bulk technology [7].

4. High-performance passives

It is a common conception that the performance of back-end passive components does not benefit from scaling, because the shrinking of wiring levels tends to increase wire resistance and parasitic capacitance. However, digital circuits require thick wires as well as thin wires for low-impedance power and ground distribution. A back end with multiple levels of various sizes can increase the capacitance density and inductance density of certain back-end passives, saving space on wafer and reducing coupling to the substrate. The thick wires can be used to increase the Q of inductors. Examples of such high-density and high-Q passives follow.

Figure 7 shows the inductance and Q of a vertical solenoid, a stacked inductor built with the unmodified back-end of a high-performance digital CMOS technology. It consists of multiple loops of wire on four copper metal levels, which generate a total inductance of 16 nH and a moderate Q of 7 at 2 GHz. The inductor diameter is only 138 μm, thus the inductance density is a record 1.07 nH/μm^2. The vertical solenoid is enabled by the copper vias of the dual damascene process, which are more conductive than tungsten vias.

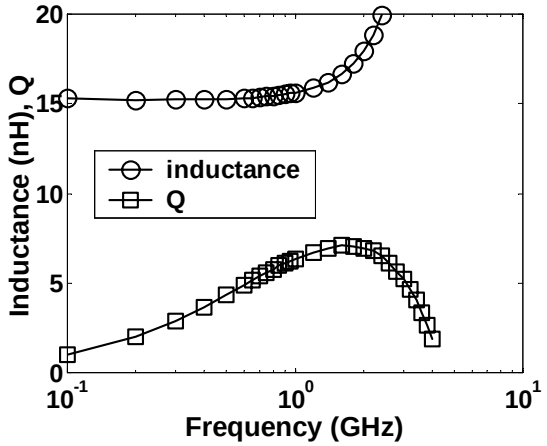

Figure 7. Inductance and single-ended Q of a vertical solenoid (de-embedded).

Figure 8 shows the model-to-hardware correlation for a single-turn inductor built on the two highest metal layers of the back-end described above. The two layers are each 1.2 μm of copper, and are 6.9 mm above the substrate. A record peak Q of 25 was measured at only 2.4 GHz, at an inductance of 0.86 nH. Good agreement with the model is achieved.

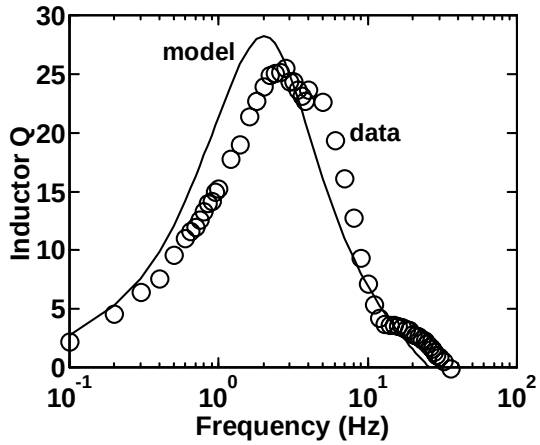

Figure 8. Modeled and measured single-ended Q of a one-turn 0.86 nH inductor (de-embedded).

5. Deterministic jitter

The impact of slow body-voltage transients on the gate delay of floating-body SOI digital circuits is well known [9]. The impact of these transients on analog circuits has not been well explored. We simulated a differential amplifier with a random input to see if the floating body of SOI FETs causes significant deterministic jitter. Figure 9 shows the eye diagram of a capacitively-loaded differential pair subjected to 900 ns (36,000 bits) of random data at 40 Gb/s with 0.6 V input swing. The simulation started at a DC condition of zero differential input voltage, and the first 100 ns of data was excluded from the diagram to neglect the initial transient. We are justified in neglecting the initial transient because 100 ns is much shorter that typical setup times of wireless networks. The jitter is too small to measure, showing that slow body-related transients are not a concern for typical RF circuits while processing data.

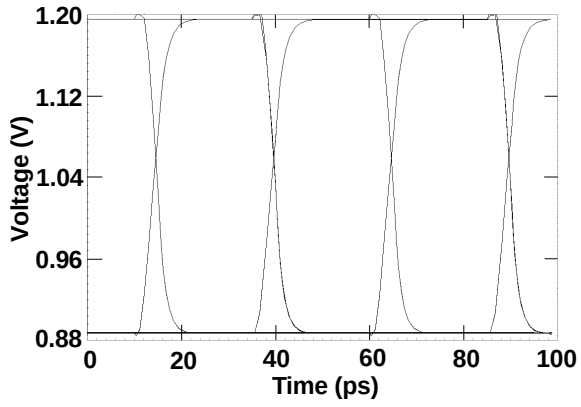

Figure 9. Eye diagram of the output of a differential amplifier.

6. Conclusion

We have shown that some important figures of merit for high-frequency analog transistor performance (f_T, g_m, C_{in}) continuously improve as FET gate length is scaled below 50 nm. We have also shown that high-performance components for high-frequency analog circuits, such as transistors with low 1/f noise and excellent RF noise, and high-density, high-Q passives, can be integrated in an aggressively scaled technology.

We acknowledge the assistance with measurement from R. Groves, C. LaMothe, M. Longstreet and S. Sweeney, the contributions of our colleagues at the Advanced Semiconductor Technology Center, and the support of G. Shahidi and B. Davari.

7. References

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