Effect of Pulsed Stress on Leakage Current In MOS Capacitors For Non-Volatile Memory Applications

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Abstract

A detailed investigation of leakage current in MOS capacitors under pulsed electrical stress is presented. In particular the effect of pulse amplitude, pulse width, time between two pulses and stress temperature is studied. A new model of trap kinetics is discussed, based on the assumption that electrical stress induces creation of both stable and metastable states (trap precursors). The latter states are not involved in trap-assisted-tunnel transport and therefore do not contribute to stress induced leakage current (SILC). However, precursors can anneal spontaneously, if the external perturbation is removed, or convert into stable traps, if the electrical stress lasts for a sufficient time. Experimental data of SILC in pulsed regime are coherently interpreted within the frame of this model.

1. Introduction

Non-Volatile Memory (NVM) market is in continuous growth and reliability is one of the critical points in advanced technology nodes. In particular, tunnel oxide degradation after repeated write/erase cycles has been identified as the outmost responsible for the device reliability loss [1-3]. On the other hand, the need for improved performances call for lower operation voltages, larger bandwidth (meant as higher number of programmable bits per unit time) and faster programming and erase. A way to improve the memory bandwidth is to decrease the programming current. This requires to use a write mechanism different from the one currently adopted, which employs the injection of Channel Hot Electrons (CHE). This subject is receiving increasing interest and some research groups have recently reported about tunnel programming with single high and short voltage pulses [4]. As a counterpart, during tunnel the oxide experiments an increase of defects which leads to the so called Stress-Induced Leakage Current (SILC) [5-8], determining a reduction of the retention time.

The study of SILC produced under the condition of fixed charge fluence through the oxide is particularly interesting, because higher stress fields (E_{OX}) imply shorter times (t_{STRESS}) and it has been shown [9] that if t_{STRESS} is short enough SILC decreases with t_{STRESS} . Similarly, we expect that for fixed E_{OX} and injected charge, a train of pulses induces a lower leakage current than a single pulse of equivalent duration. This concept is based on assessed theories on defect kinetics in amorphous semiconductors and will be the subject of a section below.
The purpose of this work is to evaluate the possibility of tunnel programming using trains of pulses, rather than a single longer pulse, in order to find a trade-off between oxide reliability and improved bandwidth.
To this aim, we investigated the effect of Fowler-Nordheim (FN) tunnel on SILC using square waveforms at the gate. In our experiments, the stress voltage amplitude (V_{STRESS}), the pulse duration (t_{ON}), the time between pulses (t_{OFF}), the injected charge (Q_{INJ}), the number of pulses (N) and the stress temperature (T) have been varied. Of course, in the case of N pulses the programming time is longer than in the case of a single pulse of duration $N \cdot t_{ON}$. Therefore, this kind of writing technique is suitable for specific application where the writing time is not a constrain, while a large bandwidth is auspicial with a long retention time.

2. Experimental details

Experiments were performed on Flash-production quality MOS capacitors featuring 7 nm-thick tunnel oxides and 10^{-2} cm^2 device area, fabricated by ST Microelectronics (Agrate Brianza, Italy). p-doped silicon and n^+ polysilicon were used for the substrate and gate electrode, respectively. The DC stress was performed through a Keithley 236 Source Unit Measure, while the pulsed stress was performed by means of a Le Croy 9101 Arbitrary Function Generator. Current was detected by a Keithley 617

Electrometer with an overall set-up sensitivity of about 10fA.
Current measurements have been performed in condition of substrate accumulation, and the voltage values reported hereafter are referred to the substrate respect to the gate.
Steady-state SILC after the applied stress was measured, accurately avoiding transient SILC effects. Furthermore, great attention has been dedicated to calibration and testing of the experimental set-up to make sure that well formed high-voltage pulses are actually delivered at the terminals of the device after transmission over the cables connecting the sample to the pulse generator. Finally, since the capacitance of our devices is approximately 4.9nF, the RC time constant of the experimental set up is not negligible and needs to be adequately accounted for, particularly in the case of the shortest pulses.

3. Results

In fig.1 experimental data of SILC measured at V=4.5V, after injection of 0.3 C/cm^2 at V_{STRESS}=9 V, are plotted as function of the pulse duration. In this experiment t_{OFF} has been fixed at 10 µs. As one can see, decreasing t_{ON} the SILC decreases accordingly. We have verified that the same charge density injected with a single pulse gives rise to a much greater SILC (not included in the figure). Obviously, shortening the pulse duration, the number of pulses needs to be increased to inject the same charge and the injection time increases as well. This is shown in the other axis of the same figure. For practical applications, results of fig.1 indicate that oxide degradation can be reduced reducing t_{ON}, but the programming time becomes longer correspondently.

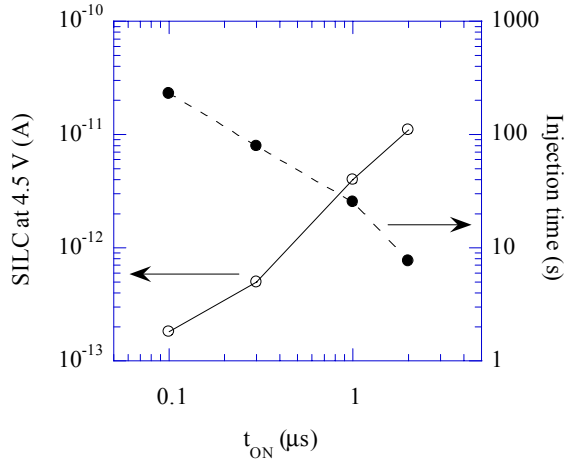

Fig. 1. SILC measured at 4.5 V as a function of pulse width (t_{ON}) after injection of 0.3 C/cm^2 at V_{STRESS}=9 V and t_{OFF}=10 µs.

In order to study the role of the pulse amplitude, in fig.2 we show the current-voltage curves obtained with Q_{INJ}=0.3 C/cm^2 varying only V_{STRESS}. In this experiment, t_{ON} and t_{OFF} are kept constant at 2 µs and 5 µs, respectively. The presence of a threshold voltage for oxide damage is clearly observed, which corresponds to oxide electric field of approximately 10 MV/cm in our samples. Then, as for the DC stress, also in pulsed condition the effect of the stress field is crucial in determining the magnitude of SILC.

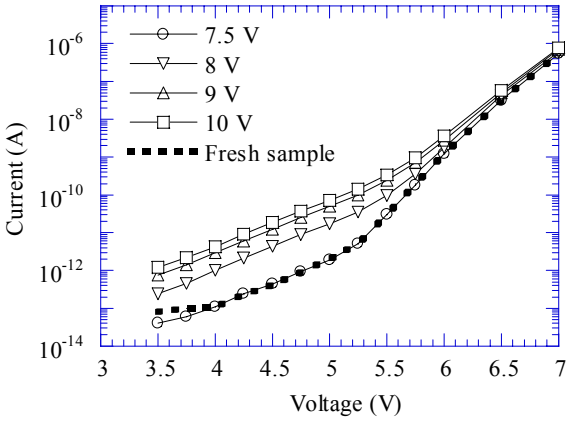

Fig. 2. Current-voltage characteristics obtained with different V_{STRESS} and Q_{INJ}= 0.3 C/cm^2. For all curves it is t_{ON} =2µs and t_{OFF}=5 µs.

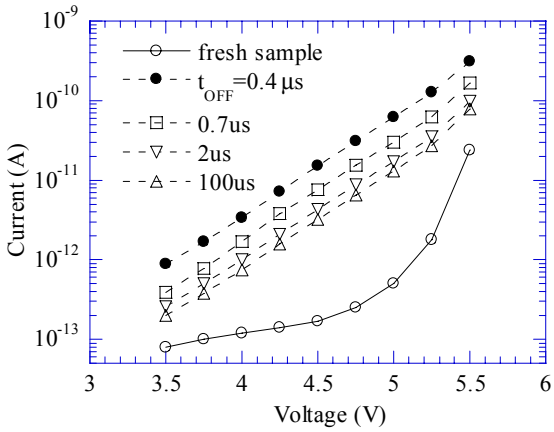

Fig. 3. Current-voltage characteristics obtained with different t_{OFF}, Q_{INJ}=0.3 C/cm^2 and V_{STRESS}=10 V. For all curves t_{ON} has been kept constant at 400 ns.

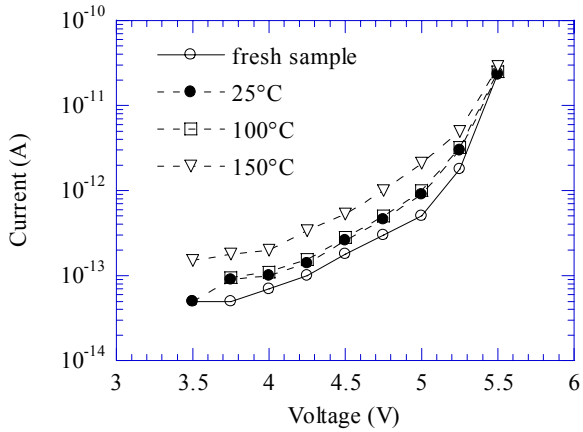

Fig. 4. Effect of the stress temperature on SILC. In this experiment it is V_{STRESS}=8V, t_{ON} =300 ns and t_{OFF}=10 µs.

Concerning the effect of t_{OFF}, we display in fig.3 data of SILC obtained varying t_{OFF} in a wide range of values. In this experiment it is t_{ON}=400 ns, V_{STRESS}=10V and Q_{INJ}=0.3 C/cm^2. The decrease of SILC increasing t_{OFF} is a novel result, which clearly indicates that also the times between pulses plays a role in SILC dynamics. In the next section an extensive discussion of this effect will be presented.

As a further investigation, the stress temperature was increased from 25°C up to 150°C. Within 100°C, we observed a negligible effect on SILC, whereas at 150°C the low-field current approximately doubles, as reported in fig.4. Therefore, SILC dynamics in pulsed regime does not change in the temperature range encountered in practical applications.

4. Phenomenological model of SILC dynamics

From experimental results of the previous section a picture of defects kinetics induced by electric stress can be drawn. First of all, SILC is given by a Trap-Assisted Tunneling (TAT) mechanism, where electrons tunnel into and out of traps located within the tunneling distance from the injecting surface. During stress, new traps are created and the concentration of newly created traps decreases with shortening t_{ON} (for fixed Q_{INJ}). During t_{OFF}, a certain degree of spontaneous annealing takes place, and a fraction of traps created during the stress (but evidently not yet stabilized) disappears. Key points of the present model are:

a) at each pulse (i.e. during t_{ON}) both stable traps and trap precursors are created;
b) during t_{OFF} a fraction of precursor traps are annealed;
c) stable traps give rise to TAT and therefore contribute to SILC, while trap precursors do not contribute to SILC;
d) during the next t_{ON} the conversion of not annealed trap precursors into stable traps can occur.

Looking at the experimental results reported above, the number of stable and metastable traps is increasing with V_{STRESS} and t_{ON}, while the number of annealed precursor increases with t_{OFF}.

The phenomenon of annealing of meta-stable states has been already widely studied in disordered semiconductors, as, for example, in hydrogenated amorphous silicon [10, 11], where the occurrence of spontaneous as well as light- or current-induced annealing has been demonstrated. Furthermore, more recently, current-induced annealing of traps has also been reported in silicon-rich oxides [12].

The oxide behavior under the condition of interest for this work (pulsed stress and fixed Q_{INJ}) poses interesting scientific problems, not yet satisfactorily tackled in the literature, particularly when both trap creation and trap annealing are simultaneously involved in trap dynamics.

In order to get a better understanding of defect creation, in fig. 5 SILC measured at 4.5V is plotted as a function of t_{ON} at different V_{STRESS} and different temperatures. t_{OFF} is kept constant at 1 µs for all curves. As expected, the number of newly created traps decreases with t_{ON}. A threshold time for creation of new stable traps (τ_{CR}) exists, that decreases with increasing E_{OX}. In our oxides, $\tau_{CR} \approx 300$ ns with 10.3 MV/cm, $\tau_{CR} \approx 100$ ns with 11.7 MV/cm, and $\tau_{CR}<100$ ns with 13.2 MV/cm. Once again the effect of temperature is almost negligible for T < 100 °C.

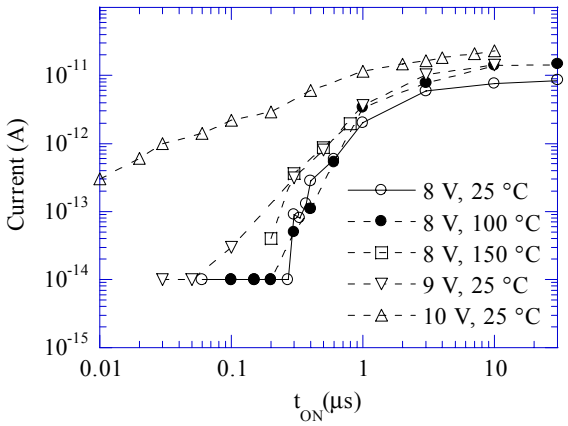

Fig. 5. Measured SILC at V=4.5 V as a function of t_{ON} at different voltage and temperatures. For all curves Q_{INJ}=0.3 C/cm^2 and t_{OFF}=1 µs.

Phenomenological consideration can be done on the role of t_{OFF} looking at fig. 6, where SILC measured at 4.5V is shown as a function of t_{OFF} at different V_{STRESS} and different t_{ON}. For t_{OFF} shorter than 1 µs we observe a fast decrease of SILC, while for longer t_{OFF} (in practice > 10 µs), all the curves tend to saturate, and SILC becomes independent on t_{OFF}. This occurs because all precursors created during a voltage pulse are completely annealed before the next pulse.

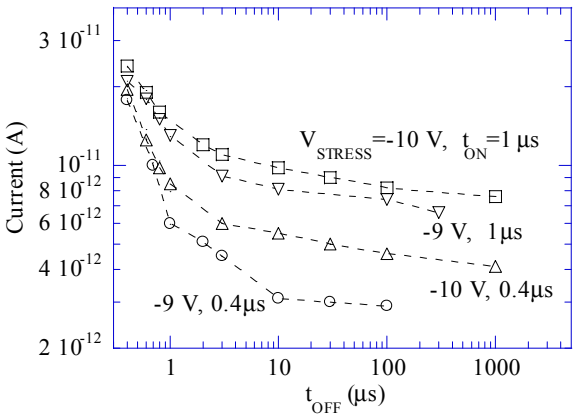

Fig. 6. SILC at V=4.5V as a function of t_{OFF} at different V_{STRESS} and t_{ON}.

5. Conclusions

A systematic study of SILC in tunnel oxides under pulsed stress has been presented. A decrease of SILC with decreasing the pulse width, the amplitude of the stress voltage and with increasing the time distance between pulses has been observed. This behavior can be interpreted referring to creation of stable traps during the application of the voltage pulse and annealing of trap precursors during t_{OFF}. The precursor not annealed during t_{OFF} can be converted into stable traps during the subsequent t_{ON}. We have found that the defect creation time is dependent on V_{STRESS}, and that for t_{OFF} longer than 10 μs all the precursors created during a voltage pulse are completely annealed before the next pulse.
From the point of view of applications, it is obvious that in order to reduce SILC induced by a train of pulses, the amount of newly created stable traps should be reduced, as well as the degree of precursor annealing should be maximized. Within the framework of tunnel programming applications, these specifications cause a programming time much longer than the one achievable by a single pulse programming, but as a counterpart a much longer retention time.

Acknowledgments

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