

Electrical Characterisation of Silicon-Rich-Oxide Based Memory Cells Using Pulsed Current-Voltage Techniques

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Abstract

MOS FET's and capacitors with a gate oxide containing a Silicon-Rich-Oxide (SRO) layer were fabricated. Memory action occurs through trapping of charge in the SRO-layer. Pulsed Current-Voltage techniques recording Id-Vg and C-V-curves have been used to determine the cell characteristics. Programming and erasing can be achieved by applying $\pm 8V$ pulses with 100ms pulse width. Faster programming and erasing can be obtained by applying e.g. $\pm 14V$, 100 μ s pulses on the gate electrode. The cells have an endurance of 10^5 cycles and an estimated retention of 10 years.

1. Introduction

The Non-Volatile-Memory (NVM) market today is dominated by floating-gate (FG) devices. According to the ITRS [1], the tunnel oxide thickness of FG devices will remain at a level of ca. 9nm for future generations. Scaling the tunnel oxide would lead to anomalous charge leakage, caused by one or two defects in the oxide [2]. Discrete charge storage bypasses this problem, hence allowing for scaling of the tunnel oxide and program/erase voltages. Reduction of the size of the charge pumps enabled by these lower voltages, as well as avoiding the double poly process required for FG devices, lowers the cost of integration especially important for embedded applications. This has triggered a renewed interest in NVM cells employing discrete, trap-like storage nodes.

Conventionally, silicon nitride is used as the charge-trapping medium [3]. Alternative storage media have been evaluated recently, including Aluminium Oxides [4] and silicon nano-crystals [5]. We have concentrated on the use of Silicon-Rich-Oxides (SRO) because of its ease of integration [6]. In this paper we present results on SRO-based memory cells integrated in a standard 0.18 μ m process.

Characterisation of memory cells requires dedicated test equipment. Usually, the threshold voltage is determined after application of write or erase pulses or after keeping the device under retention or disturb

conditions [3,7]. We are employing a simple yet versatile setup using off-the-shelf equipment. It allows not only for recording the Id-Vg curve, but also for measuring the Capacitance-Voltage curve. In this way, a more complete picture of the device operation can be drawn.

2. Processing

The memory cell consists of a conventional MOS FET, where the gate dielectric has been replaced with an Oxide-SRO-Oxide stack. The tunnel dielectric is a 2nm thermally grown SiO₂ layer and the blocking oxide is a 5nm deposited high-temperature oxide (HTO). The SRO-layer is deposited using PECVD of N₂O and SiH₄. The amount of excess silicon can be controlled by changing the gas flow ratio $R = N_2O/SiH_4$. In this experiment, a gas flow ratio of 3.5 has been used, yielding an excess silicon concentration of ca. 9.8at%, as determined by XPS. Figure 1 shows a TEM picture of the gate stack. From this figure, the SRO layer thickness was determined to be ca. 6.5nm. The TEM picture also reveals the presence of small crystalline clusters, having sizes of 1nm and less. Because of their random orientation and small size, estimation of the density of crystallites is difficult.

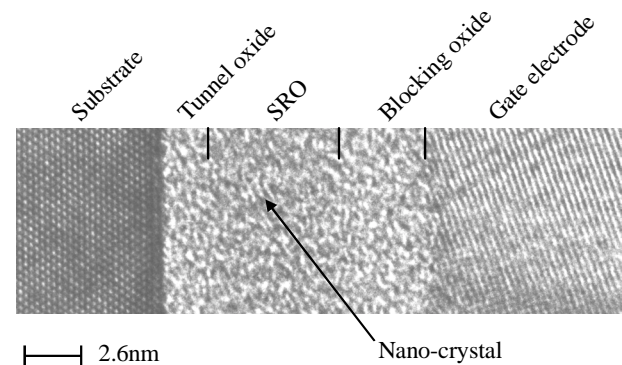


Figure 1. TEM picture of the gate oxide stack. It consists of a 2nm tunnel oxide, a 6.5nm SRO layer and a 5nm blocking oxide. A small silicon nano-crystal is indicated.

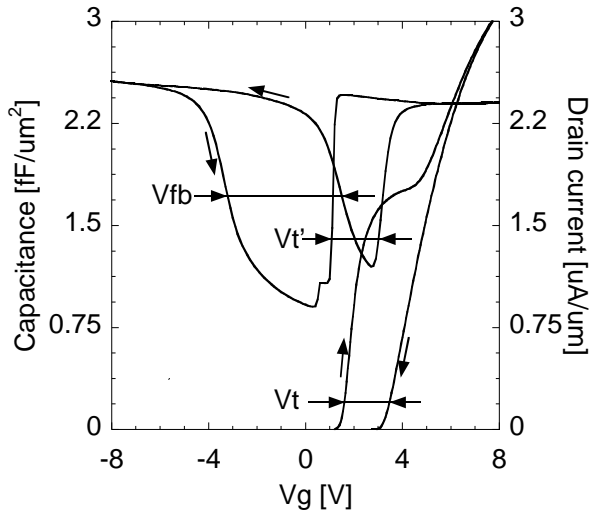


Figure 2. High-Frequency C-V measured on a large area capacitor and I_d - V_g curve measured on a $10 \times 10 \mu\text{m}$ transistor. Arrows indicate sweep direction. Memory action is apparent from the hysteresis. The large difference in V_{fb} and V_t reveals the presence of parasitic series transistors.

The process flow is based on a standard $0.18 \mu\text{m}$ CMOS process. It consists of a Poly-Encapsulated-LOCOS (PELOX) isolation scheme, gate electrode formation, extension and halo implantation, nitride spacer, HDD implantation, salicidation and SLM metallisation. Only the n-MOS transistors have been implemented. Modifications to the $0.18 \mu\text{m}$ process flow have been made in the gate electrode formation module only. This minimal deviation from the standard flow underlines the ease of integration of this memory cell.

Figure 2 shows High-Frequency C-V and I_d - V_g traces recorded in the conventional way using a HP4156A parameter analyser and a HP4284A LCR-meter. Memory action is apparent from the hysteresis in the up and down going traces. Threshold voltage shifts can be read from both the C-V and I_d - V_g traces and are seen to correspond. The flatband voltage shift read from the C-V curves, however, is definitely larger.

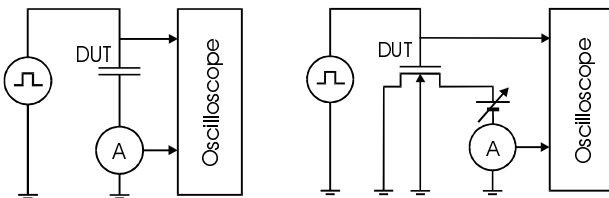


Figure 3. A schematic of the measurement setup. The setup for measuring C-V is shown at the left hand side, for measuring I_d - V_g at the right hand side.

We believe this is due to too aggressive poly re-oxidation after gate etch, consuming part of the SRO layer adjacent to the junctions. The result is a parasitic series transistor with fixed threshold voltage. When sweeping from accumulation to inversion, this parasitic transistor prohibits the supply of electrons to the inversion layer, forcing the inner capacitor into deep depletion, and cutting off the transistor current.

For the present case, correct evaluation of the cell characteristics can only be done by monitoring the flatband voltage. We employed a pulsed C-V technique described in the next section.

3. Electrical characterisation

A schematic of the pulsed C-V measurement setup is depicted in figure 3 (left hand side). An HP8112A pulse generator is connected to the gate electrode. Bulk- and source nodes are tied together and connected to the input of a fast Keithley 428 current meter. The outputs of the pulse generator and current meter are fed into a Tektronix TDS460A oscilloscope. All instruments are controlled by computer. Similar to conventional quasi-static C-V (QSCV) measurements, a sloped pulse will give rise to a current proportional to the capacitance, as shown in figure 4. Conventional QSCV measurements require slow ramp rates of the order of 0.1 V/s so as to keep the device in equilibrium. Since our devices feature a junction, minority carriers can be supplied at high rates and hence sweep rates of up to 1 kV/s can be used and current levels in the order of micro-amps are measured. Similar techniques have been used by other authors for different purposes [8, 9].

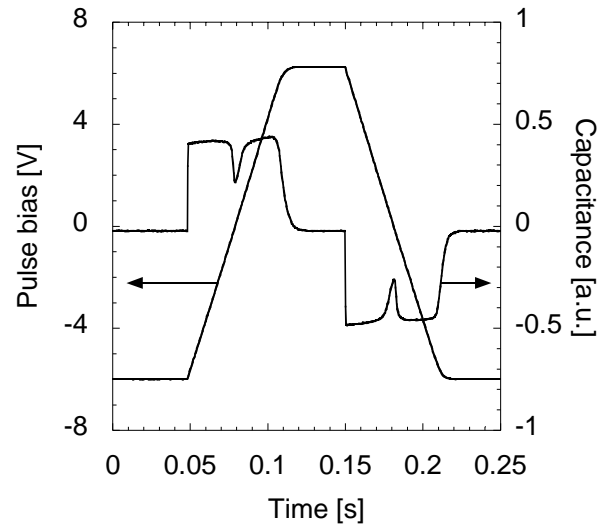


Figure 4. Pulsed C-V measurement principle. Ramping the gate bias of a MOS capacitor results in a current proportional to the capacitance. Both pulse bias and capacitance as recorded by the oscilloscope are shown.

Pulsed measurement of the I_d - V_g characteristic can be measured by only slight modification of the setup. Source and bulk are tied to ground and current is measured at the drain of the transistor. A drain bias is applied by the built-in voltage source of the current meter. A schematic is shown in figure 3 (right hand side).

The ramp rate of the pulse is practically limited to 1kV by the speed of the current meter. Fast program and erase pulses can be applied by zero checking of the current meter. This effectively shorts the input of the meter.

For the C-V measurements, large area gated diodes are used. They have an area of $1.18 \cdot 10^5 \mu\text{m}^2$. The I_d - V_g curves have been measured on $10 \times 10 \mu\text{m}$ transistors.

4. Discussion

The program and erase characteristics measured on capacitors are shown in figure 5a and 5b respectively. For erasing, the device was first prepared using a 5s, +8V pulse. Then, an erase pulse has been applied with erase voltage ranging from -2 to -14V in 2V steps. The pulse width has been varied from 1 μs to 1s, 2 points per decade. The flatband voltage has been determined by looking up the voltage at which the flatband capacitance is reached. In order to be able to compare transistor and capacitor measurements, the flatband voltage has been shifted so as to match the flatband and threshold voltage of programmed devices. Program transients have been recorded similarly.

Programming and erasing can be achieved in 100ms using voltages as low as $\pm 8\text{V}$. Faster p/e times of, e.g. 100 μs , require voltages of $\pm 14\text{V}$.

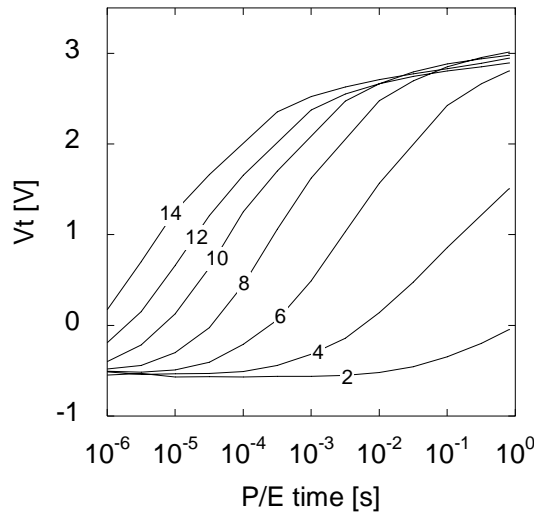


Figure 5a. Program transient characteristics measured on a capacitor. Pulse width is varied from 1 μs to 1s and p/e voltages are varied from 2 to 14V.

A peculiar feature of the erase characteristics is the reversal of the threshold voltage at larger voltages, resulting in a smaller threshold voltage window. Seemingly a drawback at first sight, this effect can be used to our advantage as a protection to over-erase.

The retention characteristic of both capacitors and transistors is shown in figure 6. The devices are programmed/erased using $\pm 8\text{V}$, 100ms pulses. The measurements have been performed at room temperature on fresh devices. Simple linear extrapolation of the capacitor curves suggests a threshold voltage window of ca. 0.7V after 10 years. In figure 6, the effect of the parasitic series transistor is apparent from the erased state of the transistor. The decay of the threshold voltage is identical for programmed transistors and capacitors. The threshold voltage of the erased transistor, however, is stable over the entire measurement range, unlike that of the capacitor. We believe the transistor threshold voltage is limited to a lower value of ca. 1.6V due to the presence of a parasitic series transistor. Measuring the flatband voltage clearly provides a more complete picture of the device operation.

Figure 7 shows endurance measurements performed on capacitors and transistors. Negligible degradation of the threshold voltage window is seen after 10^5 cycles of $\pm 8\text{V}$, 100ms pulses on both capacitors and transistors. When using +8V, 100ms and -1V, 1ms write-erase pulses, a slight widening of the window can be seen. Although widening of the window as such is beneficial, it points to degradation of the device. Future measurements will have to determine the effect of cycling on cell characteristics, most importantly retention.

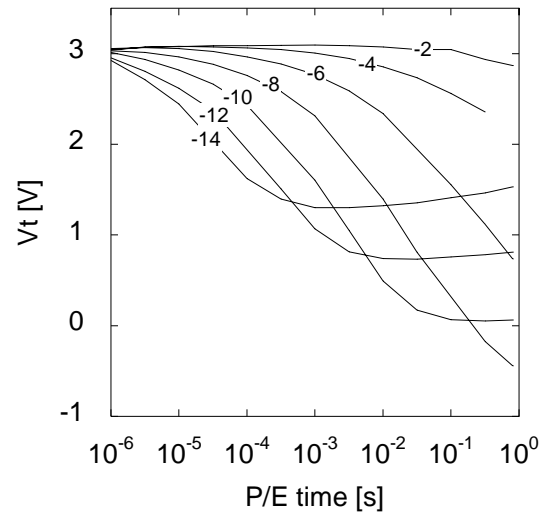


Figure 5b. Erase transient characteristics measured on a capacitor. Pulse width is varied from 1 μs to 1s and p/e voltages are varied from -2 to -14V. Note the increase of threshold voltage for erase voltages in excess of -8V.

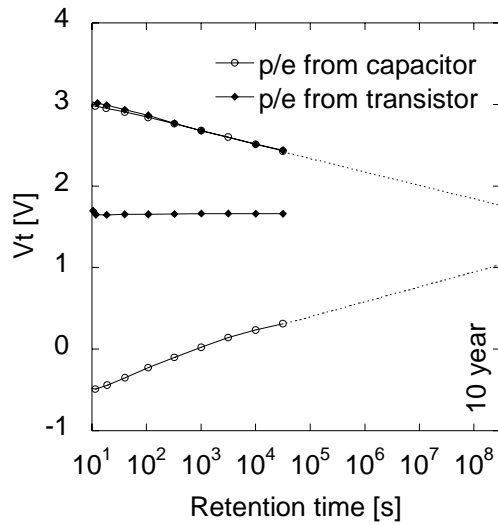


Figure 6. Retention measurement on a capacitors (open symbols) and a transistor (closed symbols). The measurements have been performed on fresh devices at room temperature.

5. Conclusions

Non-Volatile-Memory cells trapping charge in a Silicon-Rich-Oxide have been manufactured using a process marginally deviating from standard CMOS processing. The cells can be programmed and erased using voltages as low as $\pm 8\text{V}$, exhibit endurance of more than 10^5 cycles and have extrapolated data retention of 10 years. For erase voltages in excess of -8V , the threshold voltage reduces again, providing a means for over-erase protection. A simple yet versatile pulsed Current-Voltage measurement technique has been used to determine cell characteristics from capacitor and transistor devices in one and the same setup.

6. Acknowledgments

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7. References

[1] *The International Technology Roadmap for Semiconductors 2001* (ITRS), table 38a.

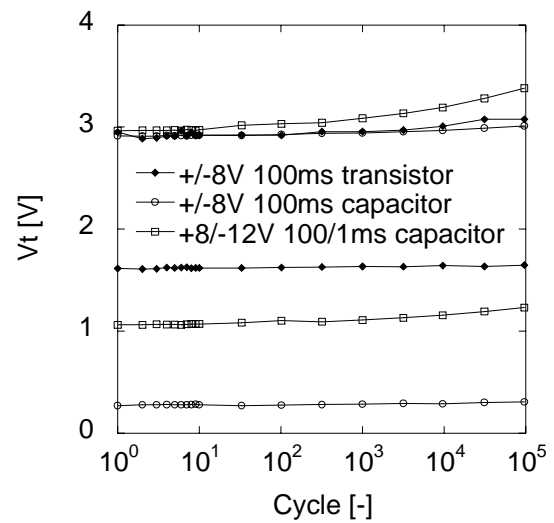


Figure 7. Endurance measurements on capacitors (open symbols) and transistors (closed symbols).

[2] R. Degraeve et al., *Analytical model for failure rate prediction due to anomalous charge loss of flash memories*, IEDM 2001, pp. 699-702.

[3] M. H. White et al., *On the go with SONOS*, Circuits & Devices, July 2000, pp. 22-31.

[4] A. Fernandes et al., *Electrical Characterisation of Memory-Cell Structures Employing Ultra-Thin Al_2O_3 Film as storage Node*, ESSDERC 2001, pp. 139-42.

[5] J. De Blauwe et al., *A novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications*, IEDM 2000, pp. 683-86.

[6] M. Rosmeulen et al., *Quasi-Non Volatile Flatband-Voltage Shift in Metal-Oxide-Semiconductor Capacitors with Silicon-Rich-Oxide Dielectric*, ESSDERC 2001, pp. 183-86.

[7] A. K. Banerjee et al., *An Automated SONOS NVM Dynamic Characterisation System*, IEEE Nonvolatile Memory Technology Review 1993, pp. 78-81.

[8] A. K. Agarwal et al., *New Results on Electron Injection, Hole injection, and Trapping in MONOS Nonvolatile Memory Devices*, IEEE. Trans. Elec. Dev., Vol. ED-32, No. 5, 1985, pp. 941-51.

[9] Z. A. Weinberg et al., *SiO_2 -induced substrate current and its relation to positive charge in field-effect transistors*, J. Appl. Phys. 59 (3), 1986, pp. 824-32.