Performance and Reliability of High Density Flash EEPROMs Under CHISEL Programming Operation

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Abstract

We demonstrate CHISEL programming operation of fully scaled high-density flash EEPROMs. Single cell program and erase characteristics show reliable operation in terms of programming disturbs and cycling induced degradation. Program and erase operation of high-density arrays show a unique post-erase operation, tight threshold voltage distribution and over 10 years of data retention even after 10^5 program/erase cycles. Results are presented showing the feasibility of CHISEL programming operation for deeply scaled high-density flash EEPROMs.

1. Introduction

CHannel Initiated Secondary ELectron (CHISEL) injection (see Figure 1) was shown to be an excellent programming mechanism for flash EEPROMs [1-7]. It offers more efficient programming (faster speed, lower power) compared to standard Channel Hot Electron (CHE) operation. Initial results of CHISEL operation on large single cells (L_{FG}>0.35μm) and relatively small test arrays of 64k-bits show highly efficient self-convergent programming, a unique recovery procedure for over erased cells [8,9], a high margin for drain disturbs as well as good endurance for programmed and erased V_T up to 10^5 program/erase cycles, leading to reliable programming operation [4-7].

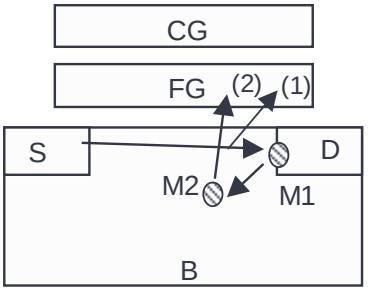

Figure 1. CHISEL injection mechanism. Channel electrons heated by lateral field undergo impact ionization M1. Holes generated from M1 flow to the substrate and undergo further impact ionization M2, which is enhanced under high transverse field (negative substrate bias). The secondary electrons (CHISEL) generated from M2 traverse towards the interface and get injected into the oxide (2) with greater energies than the lateral field heated channel electrons (1).

In this paper we demonstrate successful CHISEL programming operation of large arrays (up to 32M-bit) fabricated with fully scaled cells having L_{FG}=0.26μm. Single cell measurement results show program speed of 1.3μs at V_D=4V, V_T window closure of less than 1V and more than 10^3 program disturb margin after 10^5 program/erase cycles. Array measurement results show a unique over erase cell recovery procedure for post erase operation, tight program/erase V_T distribution and more than 10 years of data retention after 10^5 program/erase cycles. Results are presented that establish the viability of CHISEL programming operation of large arrays fabricated using scaled cells suitable for future high-density flash EEPROMs.

2. Device Fabrication

Fully scaled (W_{FG}=0.25μm) L_{FG}=0.26μm single cells and arrays (up to 32M-bit) have been fabricated using a 0.18μm process involving state-of-the art modules like STI and self aligned source/drain contacts required in high-density memories. The cells have gate coupling of 0.6 and area of 0.45μm^2. The SEM picture taken from a 32M-bit array is shown in Figure 2.

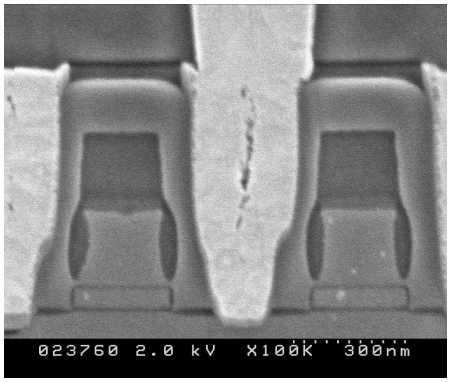

Figure 2. SEM of a 32M-bit array showing two adjacent cells. The floating (FG) and control (CG) gates and tunnel oxide (12nm) and inter poly dielectric (20nm) are shown.

3. Single cell operation

Program and erase transients of a L_{FG}=0.26μm cell before and after 10^5 program/erase cycles is shown in

Figure 3. The programming was performed at V_B=–2V with V_{CG}/V_D=8/4V while channel erase was performed at V_{CG}=–22V. Threshold voltages at programmed and erased states were fixed at 5.4V and 1.8V respectively. The measured program (T_P) and erase (T_E) times are 1.3μs and 6.3ms (initial) and 2μs and 17ms (after 10^5 cycles) respectively. Compared to CHE programming at higher V_D for identical initial T_P (not shown in this paper), CHISEL shows much lower program time degradation with slightly higher erase time degradation due to cycling.

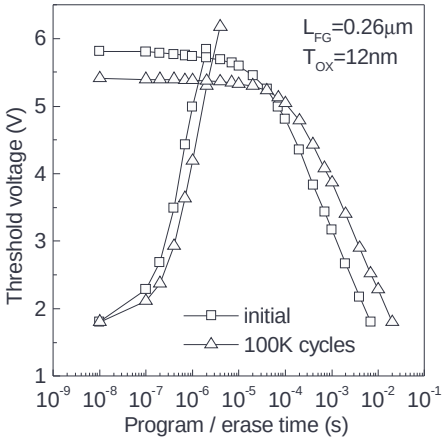

Figure 3. Program and erase transients before and after 10^5 repetitive program/erase cycles of a L_G=0.26μm flash cell under CHISEL programming operation showing 1.3μs initial programming time at V_D=4V.

Figure 4 shows V_T degradation in programmed (V_{TP}) and erased (V_{TE}) state (left y axis) and read current (right y axis) due to repetitive program/erase cycles. Programming pulse was applied for 1.3μs with $V_{CG}/V_D/V_B$=8/4/–2V. Erase pulse was applied for 6.3ms with V_{CG}=–22V. V_T was defined at V_D/I_D= 0.8V/5μA, and read current was measured at erased state with V_{CG}/V_D=4.5/0.8V.

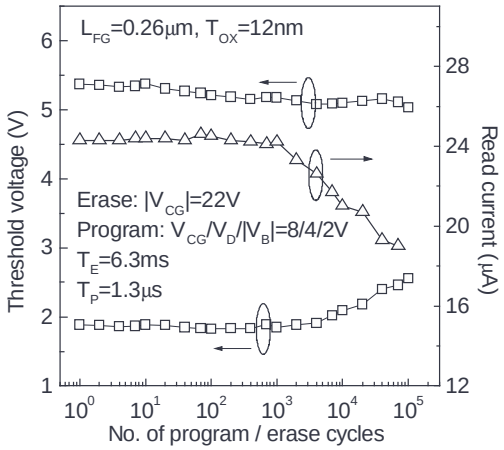

Figure 4. Cycling induced degradation in programmed and erased V_T (LHS) and read current (RHS) of a L_{FG}=0.26μm cell. Programmed and erased V_T degradation is consistent with degradation in program and erase time as shown in Figure 3.

Note that program/erase cycling creates interface and oxide defects. Charges in these defects cause read current degradation due to scattering. They also act as a barrier to charge transfer and reduce program/erase current, causing degradation in V_{TP} (hence T_P) and V_{TE} (and T_E). In Figure 4, though some degradation can be seen for V_{TE} and read current, V_{TP} shows very little degradation. This is consistent with degradation in T_P and T_E (Figure 3) – relatively smaller degradation in T_P compared to T_E. Since CHISEL mechanism populates the high-energy tail of injected electrons they can easily overcome the increase in injection barrier, which explains the relatively lesser degradation in V_{TP} (and T_P) for CHISEL operation [6]. This feature is unique to CHISEL programming operation that ensures very little overall window closure due to cycling.

Figure 5 shows charge gain and loss drain disturb measured before and after 10^5 program/erase cycles during CHISEL programming operation. Both cycling and disturb experiments were done at V_D=4V. Charge gain and loss measurements were done respectively on erased and programmed cell while V_{CG} was held at 0V.

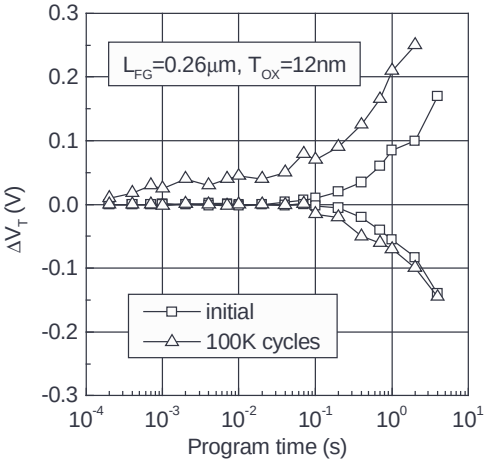

Figure 5. Charge gain and loss disturb for CHISEL programming operation of a L_{FG}=0.26μm cell, before and after 10^5 cycles. After cycling, charge gain disturb becomes greater while there is no change for charge loss disturb. Programming condition same as Figure 3.

Charge gain disturb is due to electron injection into FG, is initiated by source-drain leakage and aided by uncharged FG (positive FG potential). Charge loss disturb is due to hole injection into FG, is initiated by band-band tunneling (BBT) and aided by charged FG (negative FG potential). After cycling, charge gain disturb is enhanced, while charge loss disturb remains largely unchanged. A maximum programming time of 2μs (after 10^5 cycles) and 128 cells per bit-line leads to total disturb time of 254μs. Figure 5 shows that more than 10^3 margin is available for both the disturb modes even after 10^5 cycles – clearly indicating that drain disturb is not a serious issue for CHISEL operation. When compared to CHE operation at identical T_P (not shown), CHISEL shows much lower charge gain disturb

with slightly higher charge loss disturb. This is attributed to lower source-drain leakage (higher V_T at V_B<0) but higher BBT (higher electric field across drain junction) for CHISEL operation.

4. Array operation

Figure 6 shows the program, erase and post-erase V_T distribution measured on a 128K-bit block of a 4M-bit memory under CHISEL programming operation.

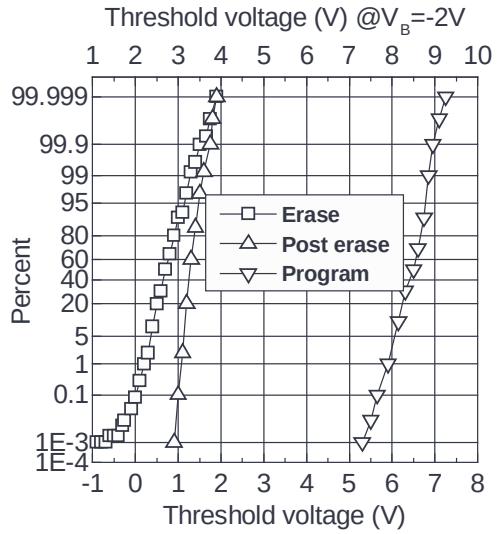

Figure 6. Program, erase and post erase V_T distribution of a 128k-bit block taken from a 4M-bit memory, made with fully scaled L_{FG}=0.26μm cells. Tight V_T distributions are obtained with CHISEL programming operation. Top x axis denotes the body effect induced V_T shift when V_B<0 is used for CHISEL programming.

Programming and post erase operations were done at V_D/V_B=6/–2V with V_{CG}=8Vand 3V respectively. To achieve identical T_P as a single cell, array operation requires higher V_D to account for the voltage drop due to bit line series resistance. Channel erase was done at V_{CG}=–22V. A 2μs programming pulse and 6.3ms erase pulse were used. Post erase operation was performed using two 10μs pulses with a single intermediate read verification scheme. The spread in V_T distribution is ~2V in the programmed state, ~3V after erase and only ~1V after post erase. The extremely tight post erase V_T distribution is obtained because of the self-converging nature of CHISEL programming which stops after the cell programs to a V_T as determined by V_{CG}=3V.

The unique recovery procedure of over-erased cells using CHISEL programming operation is described in Figure 7. Note from Figure 6 that V_T distribution after erase ("A", Figure 7) contains tail cells that are deeply over erased (V_T<0). These tail cells are difficult to recover under conventional CHE operation. However during CHISEL programming the application of a negative V_B cause V_T to increase via body effect shift (top x axis, Figure 6). The entire erased V_T distribution therefore shifts to V_T>0 ("B", Figure 7). CHISEL programming can be performed to obtain the post-erase distribution ("C", Figure 7) which reverts to true post-erase distribution at V_B=0 ("D", Figure 7).

Since CHISEL offers self convergent programming leading to tight V_T control and over erase is not an issue, cells can be programmed to relatively lower V_{TP} levels, opening up possibility for multi-level storage.

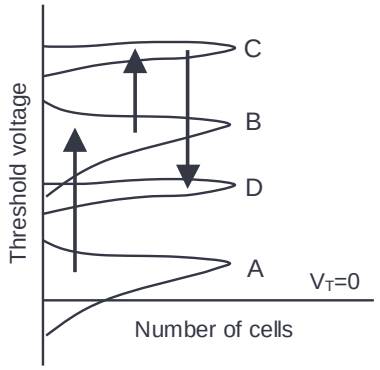

Figure 7. Over-erased cell recovery procedure under CHISEL programming operation. Body effect at V_B<0 shifts the V_T distribution from A to B. Post erase self convergent programming pushes the distribution to C, which reverts to D when V_B is set back to 0V.

Figure 8 shows the programmed and erased V_T distribution during CHISEL programming operation on a 512k-bit block of a 32M-bit memory. Measurements were performed both before and after different amount of repetitive program/ erase cycles, up to 10^5 cycles. Program, erase and post-erase conditions are identical to Figure 6, and the erased V_T distributions are shown after post-erase convergence.

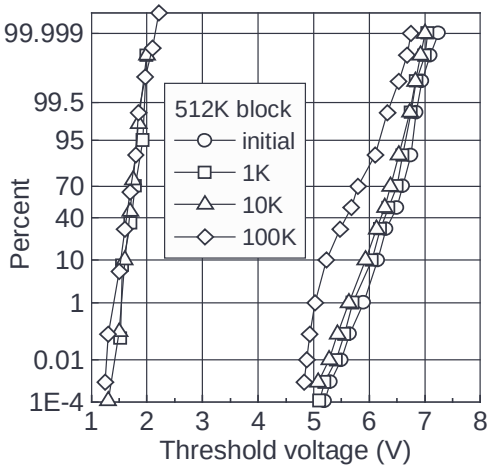

Figure 8. Cycling endurance of large array under CHISEL programming operation showing V_T distribution in programmed and erased state after different amount of repetitive program/erase cycles. Measurements were done on a 512k-bit block of a 32M-bit array. Extremely tight V_T distributions are obtained even after 10^5 cycles.

Note that even after 10^5 cycles the programmed and erased V_T distributions are tight, about ~2V and ~1V wide respectively. This proves that single cell results showing very little V_T window closure due to cycling for

CHISEL operation also holds true for large arrays. The extremely tight V_T distribution even after 10^5 cycles reinforces the possibility for multi-level storage.

5. Data retention

Data retention tests were performed on 32M-bit arrays after being subjected to 10^5 program/ erase cycles. A positive substrate bias was applied during retention test to accelerate the charge loss from floating gate to substrate. Bit-by-bit measurements were performed (with grounded substrate) to obtain the V_T distribution after each stress interval. The worst bit of the programmed V_T distribution was identified and its V_T shift was extrapolated to estimate the worst bit among 1000 chips. Figure 9 shows the accelerated charge loss for the worst bit among 1000 chips of a 32M-bit array as a function of measurement time. For comparison, the non-accelerated charge loss data is also shown. The projected data loss (by linear extrapolation) ensures that the worst bit shows no bit failure in 10 years, even after the array has seen 10^5 CHISEL program/erase cycles.

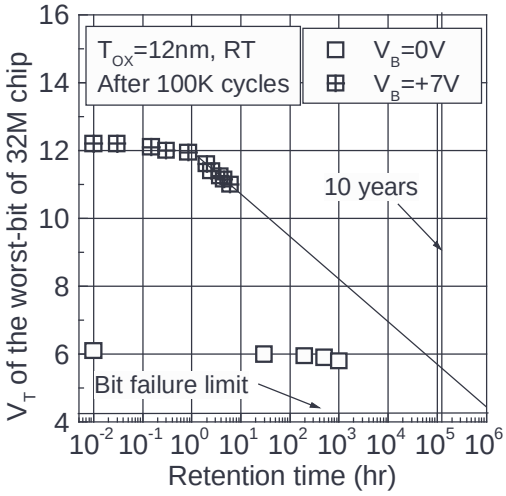

Figure 9. Estimated retention characteristics of the worst bit in 1000 32M-bit chips by using a 4M-bit test array operated in CHISEL mode. A positive substrate bias was applied to accelerate the charge loss from floating gate simulating programming to V_T=12V.

6. Conclusions

To summarize, we have demonstrated successful CHISEL programming operation on large arrays (up to 32M-bit) fabricated using fully scaled W_{FG}=0.25μm, L_{FG}=0.26μm cells (area ~0.45μm^2). The arrays were built using a state-of-the-art 0.18μm technology having advanced modules like STI and self aligned source/ drain contacts.

Single cell results show fast programming time of 1.3μs (2μs after 10^5 cycles) at V_B=–2V and V_D=4V. The reliability of CHISEL operation in terms of program/erase cycling induced degradation has been found to be extremely good. V_T window closure of less than 1V and more than 10^3 margin for programming drain disturb (for both charge gain and loss modes) have been achieved even after 10^5 cycles.

The unique over erase cell recovery procedure for CHISEL post erase operation (by employing the V_B<0 induced body effect V_T shift) has been demonstrated using array measurements. We have shown that due to the self converging nature of CHISEL programming, an extremely tight V_T distribution of ~1V can be achieved by a post erase operation involving just 2 programming steps with a single intermediate read verification. Array cycling measurements also show extremely tight V_T distribution in program and erased state, even after 10^5 cycles. Finally, charge loss experiments on large arrays show more than 10 years data retention even after 10^5 cycles. Our results demonstrate the viability of CHISEL programming operation on large arrays suitable for future large density flash memories.

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