

Impact of Tunnel Oxide Thickness on Erratic Erase in Flash Memories

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Abstract

Fowler-Nordheim erase in Flash Memories is intrinsically affected by the erratic phenomenon whose origin has physical aspects that are still obscure. This work presents new experimental results showing the impact of the oxide thickness on the erratic erase during cycling. The collected statistical results play a key role for the study of the charging/discharging properties of tunneling oxides.

1. Introduction

In the last decade Flash memories have encountered a large diffusion in the Nonvolatile memory market. Their high technological complexity has necessarily brought some new reliability problems [1, 2] with respect to more traditional nonvolatile memories. One of these, the erratic erase [3], is still far from being physically well understood.

Erratic bits are characterized by erasing dynamics exhibiting sudden and unpredictable jumps of the threshold voltage V_{TE} measured after erase (see Fig. 1).

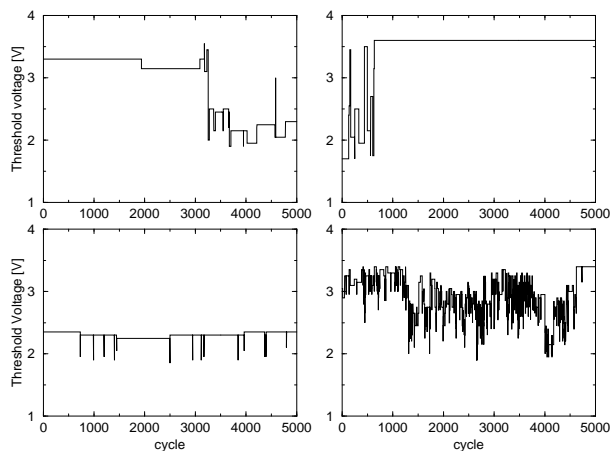


Figure 1. Threshold voltages V_{TE} measured after erase during cycling for four typical erratic behaviors: 1) erratic at the end; 2) erratic at the beginning; 3) erratic only at some cycles; 4) always erratic.

Only a tentative explanation on the nature of erratic behavior has been given in the past [3, 2]. However, a definitive confirmation of the proposed models has not been provided and some points still require further experimental and theoretical investigations.

This work presents new experimental results showing the impact of the oxide thickness on the erratic erase in Flash memories during cycling. Even if the reduction of the tunnel oxide thickness is prevented at the moment by retention limitations, the statistical analysis of the erratic behavior in Flash memories featuring thinner gate oxides and its comparison with that of today components is a powerful instrument to investigate the charging/discharging properties of tunneling oxides.

2. Experimental setup

All measurements have been performed by means of a dedicated automated test equipment [4] on single 512kbits sectors of Flash test chips. All data has been collected by tracking the V_{TE} of each cell for 10,000 program/erase cycles. Each V_{TE} measurement was performed with a quantization error of 50mV, greater than the maximum average experimental error margin that is in the order of 30mV. Erratic behaviors have been marked whenever the V_{TE} measured for a cell varied by more than ± 250 mV with respect to that measured at the end of the previous program/erase cycle.

The two considered samples differ only in their tunnel oxide thickness: 10.3nm and 7nm for samples 'A' and 'B',

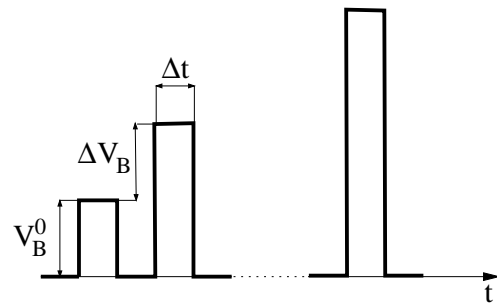


Figure 2. Sequence of bulk pulses applied during erasing.

respectively. The other technological parameters were the same.

Program was performed via Channel Hot Electron with one pulse of $10\mu s$ and a drain voltage of $4.5V$. The gate voltage was $8.2V$ (sample 'A') and $8.7V$ (sample 'B'). The source to bulk bias was $0V$ (sample 'A') and $0.5V$ (sample 'B').

Erasing was performed using the constant charge erasing scheme [5]. The cell control gates were biased by pulses with a constant amplitude ($-8V$ for sample 'A' and $-3V$ for sample 'B'), while the common bulk was driven by a sequence of 20 pulses with increasing amplitude $\Delta V_B = 0.3V$ starting at V_B^0 ($1.5V$ for sample 'A' and $2V$ for sample 'B') (see Fig. 2). The common source was kept at $0V$ and the duration of each erasing pulse was $\Delta t = 10ms$.

Program/erase operating conditions have been chosen so that comparables average electric fields during erasing [5] and similar program/erase threshold windows for both samples were guaranteed. In particular, during erasing, the average electric fields were $10.3 MV/cm$ and $10.8 MV/cm$ for samples 'A' and 'B', respectively.

3. Experimental results

Fig. 3 shows the threshold voltage distributions for the two samples after Ultra Violet exposure ($253.7nm$ for $1h$), and after a program/erase operation.

Using the constant charge erasing scheme, two separate cycling experiments have than been performed in order to find all erratic erase behaviors within the first 10,000 cycles.

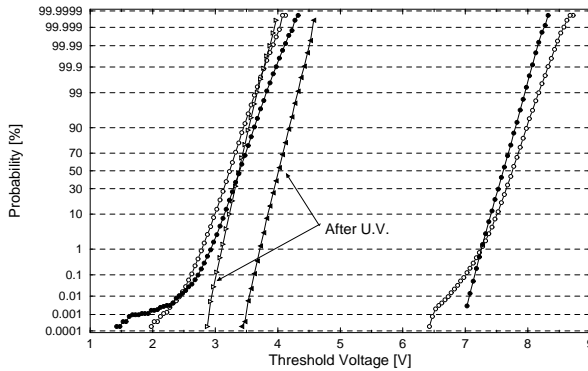


Figure 3. Distributions after program, after erase and after U.V. exposure for samples 'A' (solid symbols) and 'B' (empty symbols).

Fig. 4 shows the cumulative number of erratic events, i.e. the total number of erratic events measured starting from the first cycle.

'A' sample exhibits a larger number of erratic events. Note that the larger average value of the U.V. threshold distribution of Fig. 4 reveals that sample 'A' has yet been

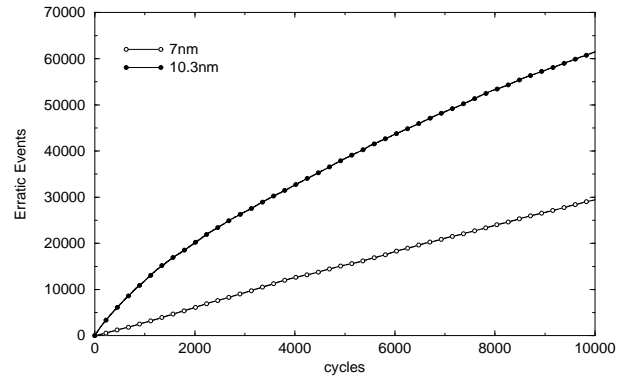


Figure 4. Cumulative number of erratic events for sample 'A' (solid symbols) and 'B' (empty symbols). It is possible to calculate an average number of ≈ 6 and ≈ 3 erratic events per cycle for sample 'A' and 'B', respectively.

cycled in the past (while sample 'B' was virgin). Oxide aging due to cycling may potentially decrease the erratic event occurrence [6]; nevertheless the result of Fig. 4 shows that this effect has a minor relevance with respect to the oxide thickness dependence.

Note also that during the first 1,000 cycles the 'A' sample exhibits an exceptionally high occurrence of erratic events. This may be due to the previous operating conditions suffered by the considered non-virgin sector. Nevertheless, on the average, the number of erratic events/cycles reaches an almost constant value (≈ 6 erratic events/cycle for sample 'A' and ≈ 3 erratic events/cycle for sample 'B').

The previous experiment only reveals the total number of erratic events suffered by a sector during cycling, without any detailed information on the number of erratic cells in a sector and on the number of erratic events suffered by those cells.

To this purpose, Fig. 5 shows the cumulative number of erratic bits, where any single erratic cell is marked when exhibiting its first erratic behavior. The larger number of erratic bits of sample 'A' is now more than evident.

Although for both samples the number of erratic bit of Fig. 5 does not seem to saturate, Fig. 6 shows that eventually their ratio reaches a constant value.

The occurrence of erratic events is not the same for all erratic bits. As shown in Fig. 7, for both samples only a small number of erratic bits gives rise to a higher occurrence. Sample 'A' exhibits a larger number of erratic bits (y axis) for each erratic event occurrence during cycling (x axis).

Finally, Fig. 8 shows the distribution of the threshold shifts marked as erratic (i.e. larger than $|250| mV$). The threshold shift distribution is symmetrically confined in the $[-2.05 V, +2.05 V]$ range for sample 'A', while that of sample 'B' is symmetrically bounded in the $[-1.35 V,$

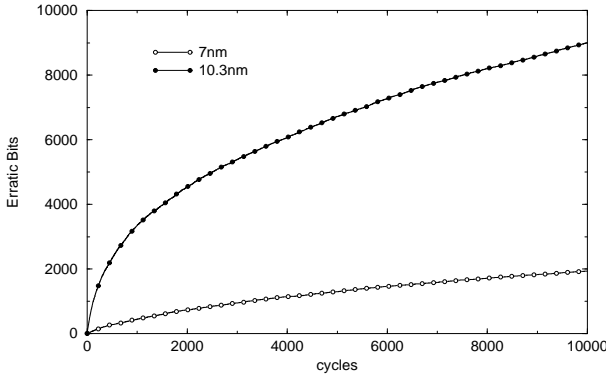


Figure 5. Cumulative number of erratic cells for sample 'A' (solid symbols) and 'B' (empty symbols).

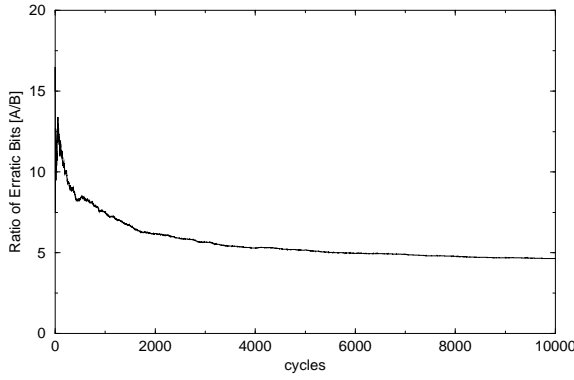


Figure 6. Ratio of the number of erratic bits of sample 'A' with respect to that of sample 'B' of Fig. 5.

+1.35 V] range, with the exception of one cell featuring a 2 V threshold shift.

4. Discussion

The experimental results reveal that the erratic event occurrence is a strong function of the oxide thickness. From the physical point of view a tentative explanation can be provided.

The first hypothesis on the erratic behavior tried to explain the erratic erase through sets of positive oxide charge clusters lowering the FN potential barrier because of their particular location close to the floating gate [2].

The major consequences of our experimental results rely on the origin of the positive charge.

As shown in this work, erratic bits are observable also during bulk erase where $V_{BS} = 0V$. Therefore the positive charge is not only related to holes created by band-to-band tunneling in the high electric field region of the source-to-bulk junction and injected into the oxide [2].

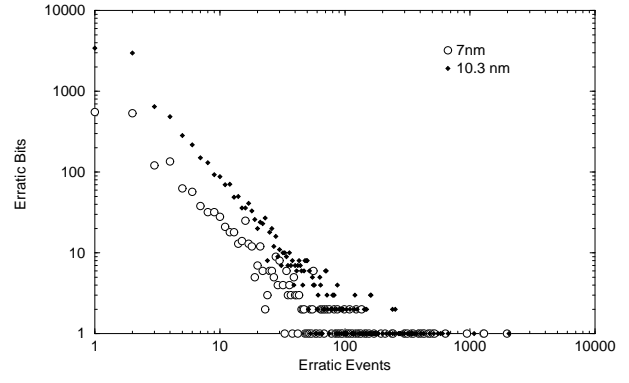


Figure 7. Distributions of the erratic bits as a function of the occurrence of erratic events during cycling. Solid symbols: sample 'A', empty symbols: sample 'B'.

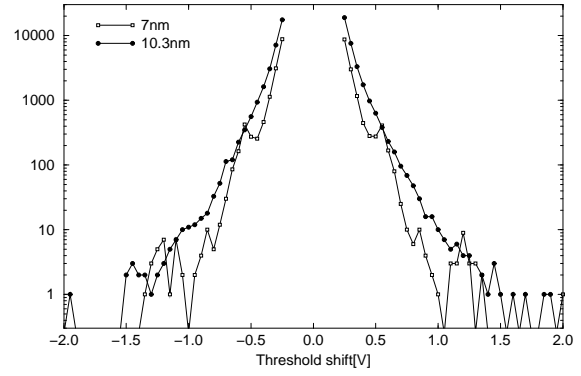


Figure 8. Threshold voltage erratic shift distributions for samples 'A' (solid symbols) and 'B' (empty symbols).

We assume that the positive charge responsible for erratic behaviors may origin from an Anode Hole Injection mechanism [7]: during erasing the FN electron current density J_n creates hole/electron pairs at the anode by impact ionization. Part of the holes tunnels back to the floating gate and some of them may be trapped into the oxide.

Using this model we suggest that the higher erratic bit failure distribution of sample 'A' (Fig. 5) may be a consequence of the hole current increase due to the increase of the tunnel oxide thickness. During erasing, with the considered tunnel oxide thicknesses and electric fields, from [7] and [8] it is possible to estimate that the fraction of hole-to-electron current density J_p/J_n is $\approx 1 \cdot 10^{-3}$ for sample 'A' and $\approx 2 \cdot 10^{-4}$ for sample 'B'.

Since ΔV_B and Δt are the same for both samples, we can also assume [5] that J_n is almost the same for both samples. Therefore the hot-hole current increase of sample 'A' with respect to sample 'B' may be expressed as

$$\frac{(J_p/J_n)_{\text{sampleA}}}{(J_p/J_n)_{\text{sampleB}}} \approx 5. \quad (1)$$

This increase in the hole-current density may be related to a proportional increase of the hole trapping probability and therefore to an increase of the number of erratic bits during cycling. The experimental result of Fig. 6 confirms the hypothesis of a correlation between anode hole current and erratic bits failure. The ratio of the erratic bit failure distribution of sample 'A' with respect to that of sample 'B' reaches a constant value that is close to the hole current ratio of Eq. 1.

5. Conclusions

Measurements and statistics on erratic behaviors of Flash memories featuring different oxide thicknesses reveal that, under the same operating conditions, thinner oxides are more robust against erratic erase.

It has been found that the ratio of the number of erratic bits for two different tunnel oxide thicknesses is a constant during cycling. The measurement of the erratic threshold voltage shifts evidences that thinner oxides have also a lower probability to exhibit larger erratic threshold shifts. Finally, a tentative explanation has also been given suggesting that the anode hole injected current during FN erase may be related to the erratic bit failure during cycling.

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