Elevated Co-Silicide for sub-100nm High Performance and RF CMOS

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Abstract

In this paper we show that the ultimate limit of Co-silicide expected for 100nm CMOS technology node can be postponed to the next generation thanks to its elevation by selective epitaxy. We demonstrate that conventional Co-silicide combined with elevated S/D can be still compatible with the junctions representative for sub-50nm CMOS devices. Moreover, elevated silicide enables reducing sheet resistance without compromising the junction leakage and degrading transistor performance. Thanks to high drive current and reduced gate sheet resistance excellent RF characteristics were obtained. 70nm NMOS devices exhibit F_T of 150GHz and Fmax of 70GHz.

1. Introduction

Co silicide has been extensively used down to 100nm CMOS technology node. In order to be compatible with the continuously decreasing junction depth and maintaining low leakage the Co-silicide thickness has been scaled down to lower silicon consumption at the expense of a higher sheet resistance. However, further scaling faces fundamental problems related to its intrinsic limitations like line width dependence and unacceptable increase in junction leakage and sheet resistance. All these limitations induce transition to nickel or platinum silicides which are still in the development phase.

The integrity of the conventional Co-silicide can be extended to the sub-100nm CMOS generations by elevated source/drain [1-3]. Silicide can be moved away from the metallurgical junction by growing selective Si epitaxial layer on top of source and drain region to provide extra Si that can be consumed during silicide formation. This approach allows using a thicker silicide that is known to have a better thermal stability on the narrow poly-Si gates. This may be a preferred approach to achieve low gate resistance due to T-shape formed by epitaxy, fig.1. Finally, this approach permits to de-couple HDD junction scaling from the silicide, reduce the spacer thickness, which determine the HDD depth, and increase the packaging density.

The effectiveness of the elevated silicides formed on the junctions representative for 0.13µm and 0.18µm CMOS technology has been already demonstrated by several authors [4-8]. In this paper we investigate the suitability of the elevated Co-silicide for sub-50nm CMOS devices where the HDD junction depth xj is expected to be below 70nm. The integrity of elevated Co-silicide modules is studied at all levels: diodes, transistors with their digital and RF performance and finally at the circuits (ring oscillators) level.

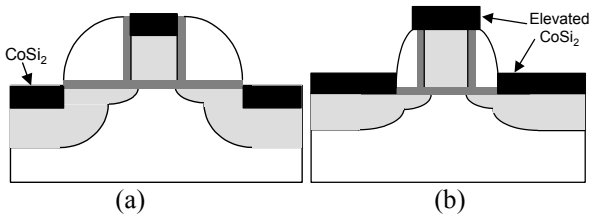


Figure 1: Schematic plot of transistor without (a) and with (b) elevated S/D

2. Device fabrication

Diodes and NMOS and PMOS transistors down to 70nm gate length were fabricated using conventional 100nm CMOS process. After well implantation 1.5nm ISSG/RPN gate oxide was grown and 150nm poly silicon gate was deposited. Low gate depletion in the NMOS gate was obtained by gate predoping followed by an annealing step. After gate patterning halos and shallow source/drain extensions (As, 5keV and B, 1keV for NMOS and PMOS, respectively) were implanted. Subsequently, 50nm nitride spacers were formed. Next, HDD junctions were implanted with the same dose and different energies: As, 4e15, 25keV and 40keV and B, 3e15, 1.5keV and 3keV. Low energy was used to simulate aggressive HDD junction of sub-50nm devices. Spike anneal at 1100°C was used to activate the dopants. Selective epitaxial growth (SEG) process was carried out *after* junction formation. 30nm or 45nm undoped Si layers were grown on S/D and gate electrode regions. In order to reduce the additional thermal budget resulting from SEG module, the pre-heating before epitaxy was processed at 800°C for 1min. The epitaxy was carried out at temperature of 810°C. Co silicidation completed the front-end process. The deposited thickness of cobalt layer was 10nm, 12nm or 15nm and the titanium capping layer was 8nm thick. These correspond to the average

silicide thickness of 25nm, 35nm and 45nm, respectively.

SEM cross-section of MOS transistor with 10nm/8nm elevated Co-Ti silicide is presented in Fig.2. The sacrificial Si epitaxial layer was 40nm. It clearly shows that despite decreased temperature of the pre-heating no facets were formed at the spacers. Silicide layer is wider than poly silicon gate due to lateral overgrowth of silicon during the epitaxy and formation of the T-shape gate.

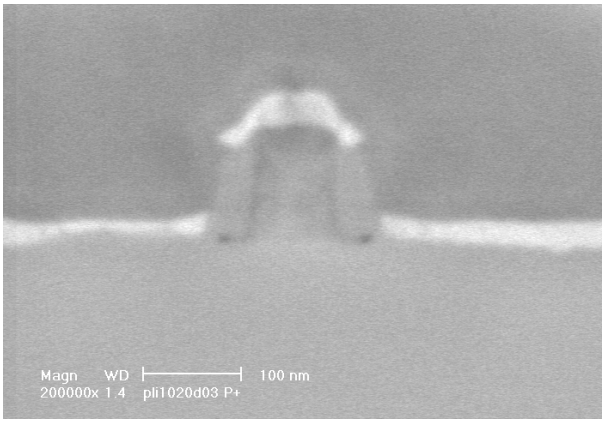


Figure 2. X-SEM photo of MOSFET with elevated S/D

3. Diode: leakage-sheet resistance trade-off

Fig.3 and 4 show the trade-off between the junction leakage and sheet resistance measured on n+/p and p+/n square diodes with various silicide and epi layer thickness. The reference devices without epi layer have thin silicide formed by 10nm cobalt deposition. In case of very shallow HDD junctions (xj~70nm) even very thin silicide (10nm Co) leads to unacceptable junction leakage. This leakage is significantly reduced for elevated silicides. Regarding shallow B (1.5keV) junction, the leakage can be reduced even by 5 orders of magnitude. Sacrificial epitaxial layer allows using thicker silicide and thus decreasing the sheet resistance up to 50% without compromising the junction leakage, fig.3 and 4. These results prove also that thanks to the elevated source/drain 15nm Co–silicide, extensively used in 0.18µm CMOS node, can be successfully integrated into sub-100nm CMOS technology. In case of n+/p junctions formed by As implant with 40keV, Co silicide formed with 12nm and 15nm Co were successfully implemented resulting in reduction of the sheet resistance by 30% and 50%, respectively. Regarding thin As (25keV) junctions, significant improvement in the junction leakage – sheet resistance trade–off has been obtained with thicker 45nm epi layer. Thickness of the sacrificial epi layer has to be compatible with the silicide thickness. Too thin epi layer results in loss of all benefit coming from elevated silicides and leads to degradation of junction characteristics. On the other hand use of too thick epi layer reduces the margin of bridging between gate and source/drain region.

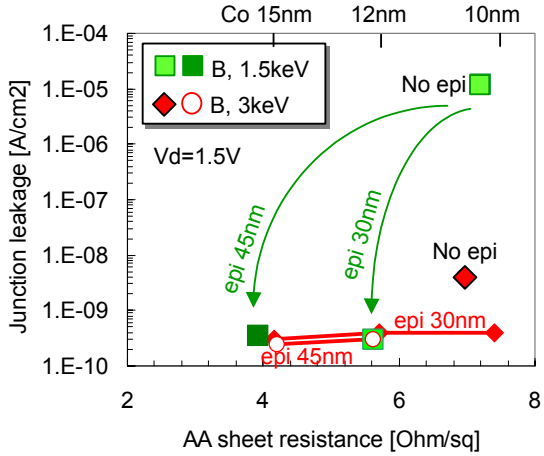


Figure 3: Junction leakage versus sheet resistance in the P+ N junction

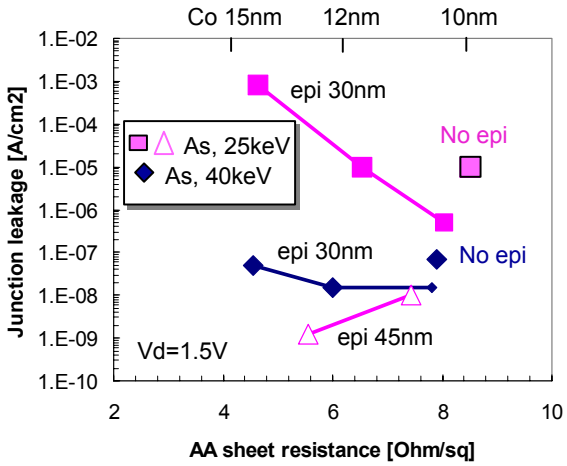
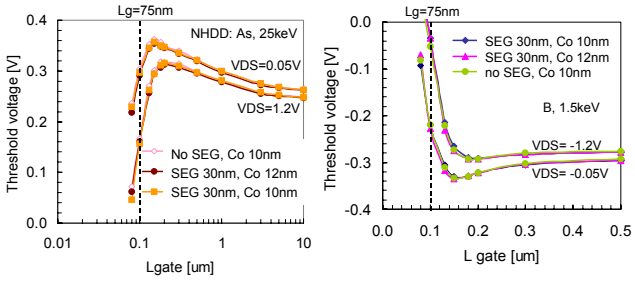


Figure 4: Junction leakage versus sheet resistance in the N+ P junction

4. Transistor performance

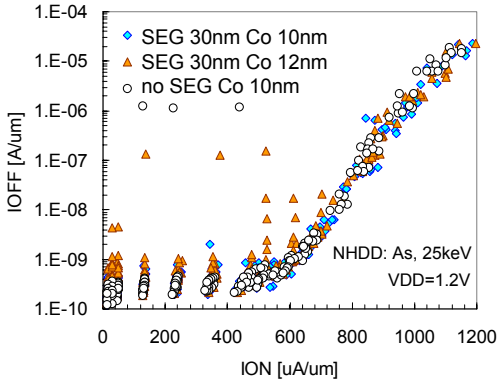
As shown in fig.5,6, SEG process prior to silicidation does not deteriorate the transistor performance. Well-controlled short channel effects and good ION/IOFF trade-off achieved with the optimised process has been maintained. At Vdd=1.2V, I_{ON}=783/352 µA/µm at I_{OFF}=13/16 nA/µm for NMOS and PMOS, respectively have been obtained. Gate predoping makes gate activation in NMOS devices independent of the epi layer thickness. In PMOS devices with elevated gate, gate predoping is not mandatory since the ION current is the same as for reference devices. It is probably attributed to strong boron diffusion in the polysilicon gate. The high spread in the distribution of the off-state current in PMOS devices with shallow HDD junction (B, 1.5keV) and conventional silicide architecture results from high junction leakage. This scattering is not present in devices with elevated silicide of the same thickness as the reference. For thicker silicide, some spread in IOFF

results from bad compatibility between epi and silicide thickness.

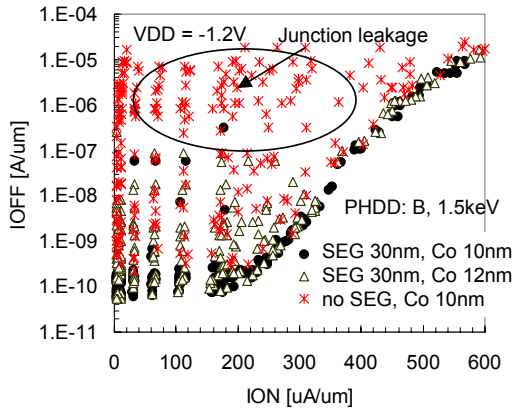


(a) (b)

Figure 5: Threshold voltage of NMOS (a) and PMOS (b) devices as a function of Ldrawn with and without elevated silicide and various silicide thickness. 100nm as drawn lines correspond to 75nm physical gate length



(a)



(b)

Figure 6: ION-IOFF trade-off plot of NMOS and PMOS devices with and without elevated silicides and various silicide thickness.

5. Gate resistance

T-shape gate formed by SEG appeared to be beneficial for the gate resistance. Fig.7 and 8 illustrate the dependence of the N+ and P+ salicided gate sheet resistance as a function of the gate length. Rs increases rapidly for thin poly lines without epi due to problems with thermal stability of thin silicide. Thanks to T-shape gate the ultimate limit of Co-silicide can be pushed to smaller dimensions. A reverse behaviour of gate sheet resistance for thinner lines is attributed to the wider silicided area provided by T-shape gate. Thicker silicide (12nm Co) enables further reduction in Rs. For 130nm wide poly lines, the sheet resistance was reduced up to 50% as compared to the reference.

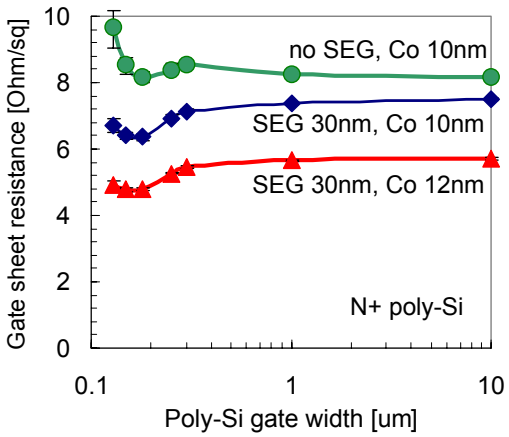


Figure 7: Gate sheet resistance as a function of N+ polysilicon line width

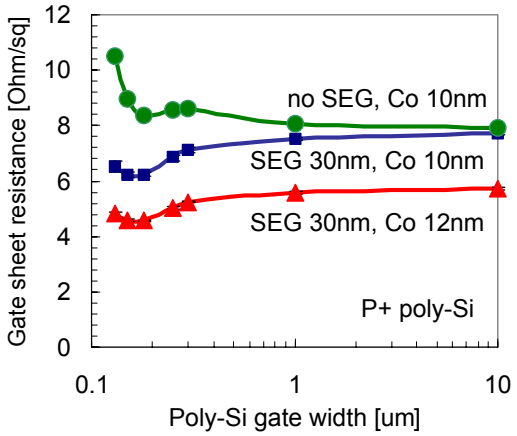


Figure 8: Gate sheet resistance as a function of P+ polysilicon line width

6. RF behaviour

High drive capability and reduced gate sheet resistance attributed to the T-shape of the gate and thicker silicide result in excellent high frequency characteristics. The maximum oscillation frequency Fmax measured at Vd=1V on 70nm two-fingers NMOS with elevated 12nm Co-silicide is 70GHz, fig.9. The 28% improvement in Fmax as compared to the reference device is mainly attributed to the reduction in the gate sheet resistance (fig.7). It has to be mentioned that this high Fmax has been measured on the structures with non-optimised RF-design (only 2 fingers, gate contacted only from one side). Optimised design is expected to deliver much higher Fmax with similar advantages of elevated silicide over conventional approach.

Contrarily to Fmax, the cut-off frequency F_T was the same for all samples since it is independent of the gate resistance, fig.10. The F_T reaches 150GHz for 80nm NMOS. These results are very competitive with the figures of merit of RF-oriented CMOS devices published in the literature [9-11].

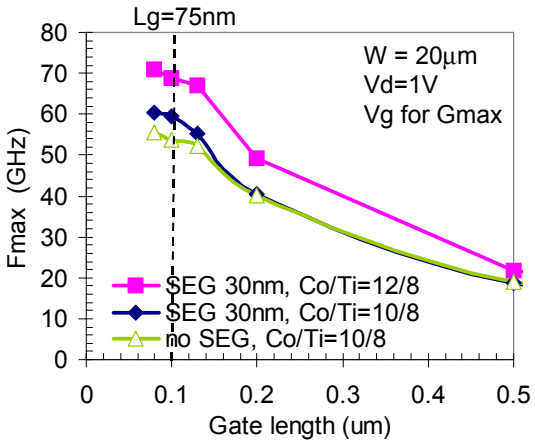


Fig.9 Maximal oscillation frequency as a function of Ldrawn for NMOS devices with and w/o elevated silicide and various silicide thickness

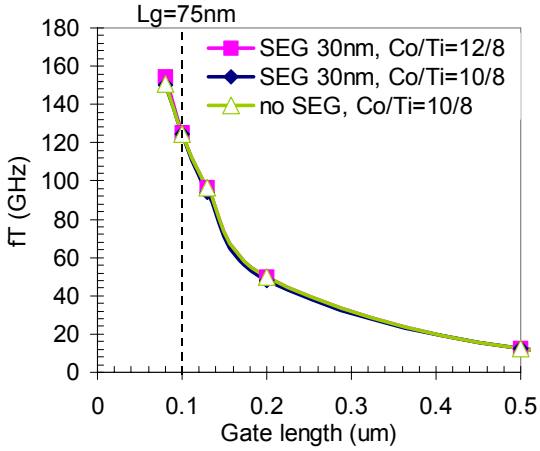


Fig.10 Cut-off frequency as a function of Ldrawn for NMOS devices with and w/o elevated silicide and various silicide thickness

7. Ring oscillator

The circuit performance of the investigated transistors is presented in fig.11. The measured ring oscillators have no load and contain 41 inverters with a gate length of 75nm. The propagation time reduces with the reduction of the gate resistance provided by the T-shape. Further decrease in resistance related to thicker silicide has minor influence on the delay time. It is because delay time is determined mostly by the parasitic capacitances which are the same for all samples. Unloaded ring oscillator fabricated with the elevated Co-silicide module has a propagation delay time of 14ps per stage at the supply voltage of 1.2V.

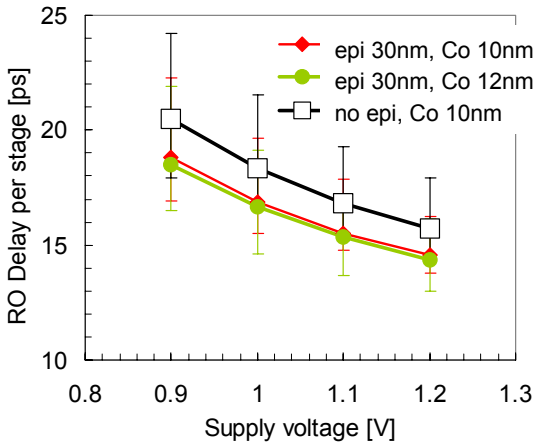


Figure 11: Gate delay of unloaded ring oscillator.

8. Conclusions

The feasibility of expanding conventional Co-silicide integrity into the sub-100nm CMOS technology node was demonstrated. The ultimate limit of Co-silicide can be postponed by its elevation using selective epitaxy. With elevated silicide the trade-off between the junction leakage and sheet resistance was significantly improved without compromising transistor performance. Thanks to reduced gate resistance attributed to elevated silicide and high drive current excellent RF characteristics were obtained. 70nm NMOS devices exhibit F_T of 150GHz and Fmax of 70GHz.

9. References

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10. Acknowledgement

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