Degradation Dynamics for Deep Scaled p-MOSFET's during Hot-Carrier Stress

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Abstract

Hot-Carrier degradation in p-channel MOSFET's is investigated comparing Hydrogen (H_2) and Deuterium (D_2) annealed devices. Two physical mechanisms are clearly recognized during low gate voltage stress ($|V_G| \ll |V_{DS}|$), namely the Hot-Electron-Induced Punch-through (HEIP) and the Interface State Generation (ISG). The dependence of the degradation dynamics on the gate oxide thickness is discussed in detail, showing that the Deuterium giant isotope effect can improve the lifetime of deep sub-micron pMOSFET's by reducing the ISG process. Finally, the accelerated stress protocol commonly used to evaluate pMOSFET Hot-Carrier reliability is critically reviewed.

1. Introduction

Reliability of deep sub-micron n and p channel MOSFET's is a mandatory issue for device scaling and many efforts have been devoted to investigate device degradation during Hot-Carrier stress. Standard protocols [1, 2] have been established and are currently applied to perform accelerated stress experiments useful to predict transistor lifetime at the operating bias. Despite these procedures have been demonstrated to be valuable tools for device characterization, their application to new sub-quarter-micron technologies must be careful verified, in the light of the microscopical mechanisms responsible for the degradation dynamics.

In this work we report a detailed experimental study of Hot-Carrier degradation in deep sub-micron pMOSFET's. Comparing the results obtained from H_2 and D_2 annealed devices the impact of two simultaneous degradation processes, namely the Hot-Electron-Induced Punch-through (HEIP) and the Interface State Generation (ISG), is highlighted during low gate voltage stress ($|V_G| \ll |V_{DS}|$). The contribution of each mechanism to performance degradation is discussed, showing that different degradation curves are obtained for different oxide thicknesses. ISG is shown to be the dominant degradation mechanism for very thin gate oxide ($t_{ox} \leq 3$ nm) pMOSFET's and the effectiveness of D_2 treatments in improving lifetime of deep scaled p-channel MOSFET's is proved. Finally, the accelerated stress procedure commonly used to evaluate pMOSFET lifetime is critically reviewed and the major issues related to the development of a new stress protocol are presented in detail.

2. Experimental

Low Voltage (LV) and High Voltage (HV) MOSFET's with gate oxide thickness ranging from 15 nm to 3 nm were fabricated in 0.25 μm CMOS technology by STMicroelectronics and Infineon. For the reference samples the annealing steps were performed in H_2 while the deuterated samples received a D_2 post-metal anneal at 430°C for 1 hour (1 atm). Standard Hot-Carrier accelerated stress procedures have been used to characterize the reliability of n and p-channel MOSFET's. The I-V curves were periodically measured in both linear and saturation regime in order to determine the threshold voltage V_{th}, the maximum transconductance g_m, and the saturated drain current I_{DS}^{sat}. The relative variation of the parameters has been evaluated according to the formula:

$$\frac{\Delta f}{f} = \frac{f_{b.s.} - f_{a.s.}}{f_{b.s.}}, \qquad (1)$$

where f is the monitored quantity, *e.g.* the saturated drain current I_{DS}^{sat}, estimated before ($b.s.$) and after ($a.s.$) stress. The effectiveness of the annealing receipt in creating an accumulation of Deuterium at the silicon surface is clearly assessed by the results obtained from n-channel MOSFET's, for which an improvement of about a factor 10 in device lifetime at the operating bias is observed.

3. Degradation Mechanisms

Fig. 1 shows the saturation current degradation for H_2 (filled symbols) and D_2 (open symbols) annealed

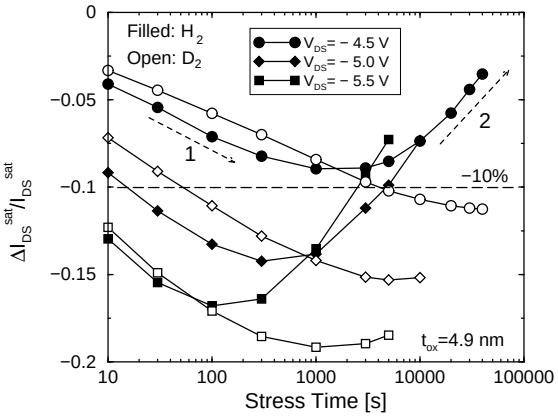

Figure 1. Saturation current degradation for H_2 (filled symbols) and D_2 (open symbols) annealed samples stressed at $V_{DS} = -5.5$ V, -5.0 V, and -4.5 V. Gate oxide thickness is 4.9 nm. At short stress time the degradation is due to the HEIP (arrow 1), while at longer stress time ISG becomes the dominant damage mechanism (arrow 2). The deuterated sample have an improved resistance to Hot-Carrier ISG.

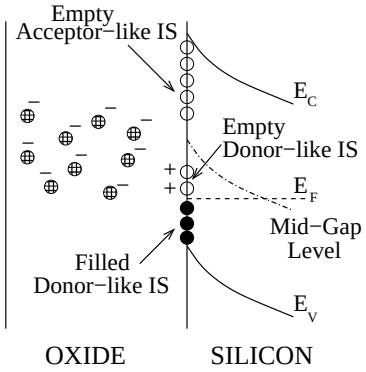

Figure 2. Schematic representation of the charge trapping mechanisms that take part in pMOSFET Hot-Carrier degradation at low gate voltages. Negative charge in the bulk of the gate oxide is a result of the HEIP mechanism whereas positive charge at the silicon surface is generated by ionization of donor-like interface states (IS) introduced in the lower part of the band gap by Hot-Carrier ISG. Note that interface states in the upper part of the band gap are acceptor-like, that is neutral when empty.

LV pMOSFET's with 4.9nm gate oxide and 0.2μm gate length. Stress was performed at the peak of the gate current and $V_{DS} = -5.5$ V, -5.0 V, and -4.5 V. The corresponding gate voltages were $V_G = -0.9$ V, -0.85 V, and -0.8 V. It is clear from this figure that at least two different mechanisms are responsible for the degradation process. At short stress times (arrow 1) the saturation current increases in accordance with a measured less negative threshold voltage (the threshold voltage absolute value $|V_{th}|$ is reduced). This shift is consistent with the HEIP process, in which a negative oxide charge is created at the drain side of the device by secondary electrons injected over the silicon-oxide potential barrier and trapped into oxide defects. At constant gate bias the negative charge in the bulk of the oxide increases the hole density in the channel and the drain current in both ohmic and saturation regime. At longer stress times (arrow 2) the saturation current decreases, causing a turn-around which could be explained by positive charge starting to overcome the shift due to the HEIP. Since the stress experiments are performed at the peak of the gate current, there is no hole injection in the oxide. On the other hand, a positive charge is created at the silicon surface by ionization of interface states introduced in the silicon band gap by Hydrogen (Deuterium) Hot-Carrier stimulated desorption. The defect centres produced by Si-H (Si-D) bond breaking introduce in fact a donor-like and an acceptor-like spurious state in the silicon band gap, the former near the valence band edge and the latter near the conduction band edge [3, 4]. These are fast interface states and their occupation follows the position of the Fermi level in the energy gap. Since in a pMOSFET at inversion the Fermi level is located near the valence band edge, the Si-H (Si-D) bond-breaking result is the generation of net positive charge at the drain side. A schematic illustration of the charge trapping mechanisms taking part in pMOSFET Hot-Carrier degradation at low gate voltages is reported in Fig. 2. Note the negative charge trapped in the oxide and the positive charge originating from the ionization of the donor-like interface states in the lower part of the energy gap. The comparison of the results obtained from H_2 and D_2 annealed devices confirms these considerations. It is well-established in fact that deuterated samples present an improved resistance to ISG [5] and this leads in Fig. 1 to a turn-around of the degradation curves at longer stress times for these devices. This result demonstrates that a contribution from the ISG in pMOSFET Hot-Carrier degradation exists and that a Deuterium treatment can be effective in improving pMOSFET lifetime.

4. Oxide Thickness Dependence

Fig. 3 shows the relative shift of the maximum transconductance g_m for H_2 (filled symbols) and D_2 (open symbols) annealed samples with different oxide thickness. Gate lengths are 0.5μm and 0.2μm respectively for the 15 nm (HV) and the 3 and 4.9 nm (LV) gate oxide devices. Stress was performed at the peak of the gate current. A turn around can still be recognized for the 4.9 nm gate oxide devices (diamonds). The devices with the thickest (15 nm, circles) and the thinnest (3 nm, squares) gate oxide show instead a monotonous degradation. The sample with the thickest oxide follow a logarithmic time dependence and the transconductance increases with the stress time. This result is consistent with the HEIP mechanism, for which a logarithmic time dependence of the transistor electrical parameter degra-

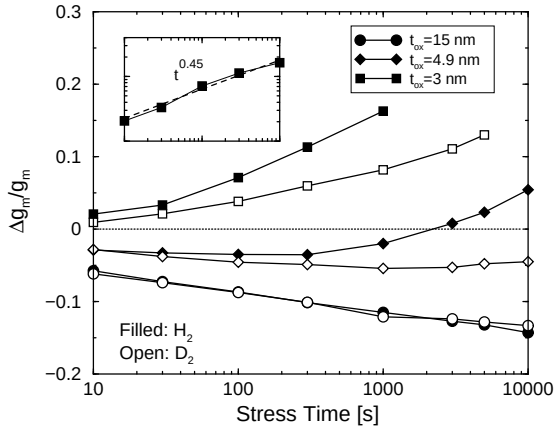

Figure 3. Maximum transconductance degradation for H_2 (filled symbols) and D_2 (open symbols) annealed samples with different oxide thickness. For the thickest gate oxide devices (circles, 15 nm) the dominant stress mechanism is HEIP and no improvement is observed from the D_2 anneal. For the thinnest gate oxide samples (squares,3 nm) the degradation is dominated by ISG and D_2 causes a lifetime improvement. The inset shows the power-law ISG time dependence observed for the thinnest gate oxide samples.

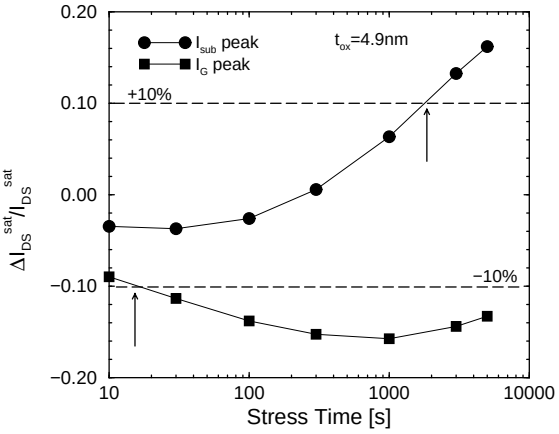

Figure 4. Saturation current degradation for stress conducted at the peak of the gate current (squares) and at the peak of the substrate current (circles). Limits for lifetime extraction are shown as dashed lines.

dation is usually observed [6, 7]. On the other hand, the sample with 3 nm gate oxide thickness shows a power-law dependence $t^{0.45}$ (see the inset of the same figure), in agreement with the commonly observed ISG time dependences [1]. In this case the transconductance is reduced, i.e. $\Delta g_m/g_m$ is positive. This result suggests that the HEIP mechanism dominates the degradation of the thickest gate oxide devices, but as the oxide thickness decreases ISG shows up causing the reduction of the electron charge trapped in bulk oxide [8]. For samples with 4.9 nm gate oxide HEIP and ISG are about of the same order and the different time dependences (logarithmical vs. power-law) lead to the turn-around of the degradation curves after a stress time of about 100 s. For the thinnest gate oxide the transconductance degradation is dominated by ISG, while HEIP contribution is now negligible.

Fig. 3 also shows a comparison of the results obtained from H_2 (filled symbols) and D_2 (open symbols) annealed samples. As the sample with the thickest oxide is characterized by the HEIP degradation mechanism, no improvement is obtained from the D_2 treatment. For the thinnest oxide samples instead, the degradation is attributed to ISG and deuteration is effective in improving stress resistance. This means that for thin gate oxide pMOSFET's ($t_{ox} \leq 3$ nm) the deuteration step can be as effective in reducing Hot-Carrier degradation as for nMOSFET's. For the 4.9 nm gate oxide transistors the behavior of the H_2 and the D_2 annealed samples is almost the same in the first part of the degradation process (dominated by HEIP), whereas a strong isotope effect appears at longer stress time (when ISG becomes dominant).

5. Accelerated Stress Procedure

The standard accelerated stress protocols developed in the past can be applied to devices with thick gate oxide, which show a monotonous degradation dominated by HEIP. However, as the gate oxide thickness decreases, ISG shows up and the worst bias conditions are no more those corresponding to the maximum gate current. Fig. 4 and Fig. 5 show that the worst stress condition (lowest lifetime) for 4.9 nm gate oxide devices is at the peak of the substrate current (where the ISG process is enhanced) when monitoring the maximum transconductance degradation, whereas it is at the peak of the gate current (where the HEIP process is enhanced) when monitoring the saturation current. The presence of a roll-off may also affect the automatic quantitative estimate of the D_2 improvement in lifetime. For example, Fig. 1 shows that the D_2 anneal shifts the turn-around of the degradation curves at longer stress time, but this can lead to a shorter lifetime if the maximum acceptable shift is reached before the turn-around (see in Fig. 1 the lifetime of the curves relative to $V_{DS} = -4.5$ V extracted from a -10% limit in the saturation current shift).

Reduction in gate oxide thickness causes an enhancement of the ISG over the HEIP, thus eliminating the turn-around of the degradation curves. Fig. 6 shows the results obtained for H_2 and D_2 annealed devices with 3 nm gate oxide stressed at the peak of the substrate current. Note the power-law dependence of the degradation curve on stress time and the improvement in the deuterated device resistance to Hot-Carrier damage. In any way, a concern must be accurately considered for low-voltage stress. In fact, despite in *accelerated* stress tests (high-voltage operating bias) the device degradation is dominated by the ISG, for *low-voltage* stress the role played by HEIP is not negligible, thus requiring an accurate estimation of the impact of both stress mechanisms. This is evident

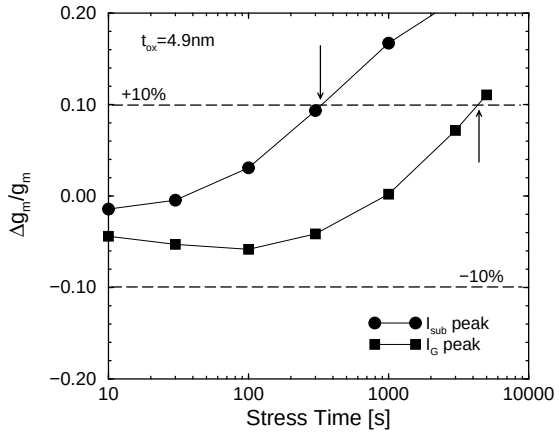

Figure 5. Maximum transconductance degradation for stress conducted at the peak of the gate current (squares) and at the peak of the substrate current (circles). Limits for lifetime extraction are shown as dashed lines.

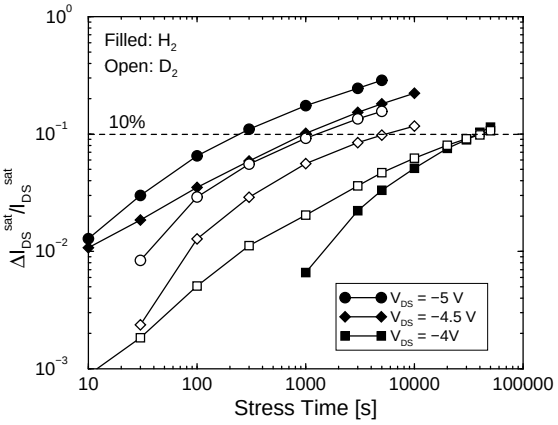

Figure 6. Saturation current degradation for H_2 and D_2 annealed devices with 3 nm gate oxide stressed at different drain voltages. The stress was performed at the peak of the substrate current.

in Fig. 6 from the results obtained at the lowest voltage, where there is no clear deuteration benefit.

The development of a standard stress protocol for the extrapolation of deep sub-micron pMOSFET lifetime is therefore limited by the possibility of controlling the degradation dynamics, strictly dependent on the oxide thickness. The standard stress procedure is still valid for thick gate oxide devices but must be modified for thin oxide transistors, for which ISG is not negligible giving rise to a mixed degradation process that does not easily allow the extrapolation of device lifetime at operating bias. Furthermore, even if in very thin gate oxide devices the stress procedure used for nMOSFET's seems to be correct at high stress voltages (because the ISG is clearly dominant), problems still exist at lower stress voltages, because the influence of the HEIP is not negligible in these conditions. In order to obtain a correct quantification of the device lifetime and of the deuteration benefits an accurate control over all these issues is required.

6. Conclusions

The mechanisms responsible for deep sub-micron pMOSFET Hot-Carrier degradation at low gate voltage have been investigated in detail comparing H_2 and D_2 annealed devices. Two mechanisms contributing to the degradation process have been clearly recognized, namely the Hot-Electron-Induced Punch-through and the Interface State Generation. The time evolution of the degradation for various oxide thicknesses has been discussed, showing that Deuterium can improve the lifetime of deep sub-micron pMOSFET's. Finally, a critical review of the standard accelerated stress protocol for pMOSFET's is presented, showing the main problems related to the lifetime extraction and the quantitative estimation of the deuteration benefits for very thin gate oxides.

7. Acknowledgments

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