

Substrate Effects on the Small-Signal Characteristics of SOI MOSFETs

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Abstract

The present paper investigates the influence of the silicon substrate on the AC characteristics of fully-depleted (FD) and partially-depleted (PD) silicon-on-insulator (SOI) MOSFETs. For the first time it is shown that the presence of the substrate underneath the buried oxide results in two transitions (i.e. zero-pole doublets) in the output conductance vs frequency characteristics, depending on the space-charge conditions at the buried oxide-substrate interface. The paper discusses the analytical device modelling to include the influence of the substrate in CAD circuit simulations.

1. Introduction

As thin-film short-channel silicon-on-insulator (SOI) technology is becoming a major contender for low-power systems-on-a-chip including microwave functions, a deep understanding of the frequency behaviour of SOI MOSFETs is needed. Previous studies, devoted to the investigation of their small-signal characteristics, mostly focused on partially-depleted (PD) transistors and on the impact of the self-heating (SH) and kink effect at high gate and drain voltages [1-5], but so far, no attention has been paid to the influence of the Si substrate on these characteristics. In this paper, we will demonstrate that electrical coupling through the substrate results in two transitions in frequency-dependent AC characteristics. In addition to the observation of a high-frequency zero-pole doublet on experimental microwave output conductance characteristics of 0.25 μm fully depleted (FD) SOI MOSFETs, our 2D device simulations demonstrate the occurrence of another zero-pole doublet at low frequencies. These effects become more important with continuous scaling down of the device dimensions and of the supply voltages. An analytical device model is proposed to explain the phenomena and include them in CAD circuits simulations for both PD and FD devices.

2. Experiment

Microwave characterization was performed on FD SOI MOSFETs from LETI 0.25 μm process with silicided source, drain and gate. Typical microwave performance at $V_D=V_G=0.9\text{V}$ are $f_T=42\text{GHz}$, $f_{\text{max}}=71\text{GHz}$, Minimum Noise Figure=0.8dB, associated

gain = 14 dB at 6 GHz [6]. The small-signal equivalent circuits element values were extracted directly from the measured S-parameters using a specific extraction procedure described in [7].

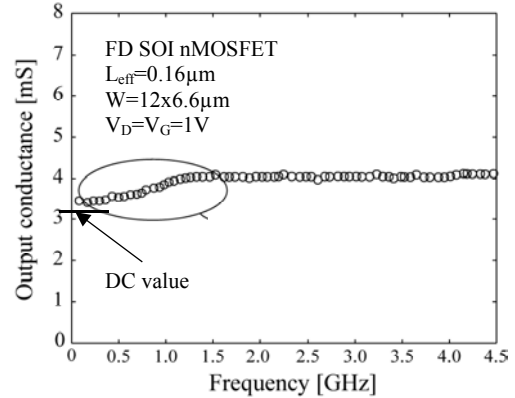


Figure 1. Total output conductance measurement.

Fig. 1 shows a typical measurement of the total output conductance from 40 MHz up to 4.5 GHz for a FD SOI nMOSFET in saturation below kink regime. The output conductance presents an unexpected variation around 1GHz which is a frequency much higher than the previously reported transitions due to floating body or thermal effects [1-5]. The latter could however explain the difference between the DC output conductance value extracted from $I_D V_D$ curve to be about 3.2 mS and the 40MHz value which is about 3.4 mS. Electrical Silvaco simulations have then been run in order to understand the physical origin of the output conductance increase.

3. Simulations

Two-dimensional numerical simulations of FD SOI MOSFETs were performed using ATLAS software. The 2D simulated structure included the extrinsic accesses. The Si film, gate and buried oxide thicknesses were 30nm, 5 nm and 400 nm, respectively. The Si film doping was $8 \times 10^{17} \text{ cm}^{-3}$. DC and AC simulations have been done for transistors with effective channel length from 0.16 to 0.91 μm . We included the underlying p-type Si substrate with a thickness of 20 μm (which was proved sufficient in our case) and doping levels of $6.5 \times 10^{14} \text{ cm}^{-3}$ for standard process and of $2 \times 10^{12} \text{ cm}^{-3}$ for low-doped (i.e. high resistivity) substrate case.

Before simulating the AC characteristics of the devices, exhaustive DC simulations were performed to

choose the correct physical models and adjust the model parameters. For all simulations, 2-carrier continuity equations were solved, the parallel and perpendicular field-dependent mobility models, SRH as well as Auger recombination and the effect of impact ionisation were included. For short-channel devices, it is also very important to include the energy balance model, which accounts for “non-local” effects such as velocity overshoot, diffusion associated with carrier temperature and the dependence of impact ionisation rate on carrier energy distribution. It is finally necessary to take into account the self-heating effect in SOI devices due to the low thermal conductivity of the buried oxide.

AC simulations were performed in the frequency (f) range from 10 Hz to 10 GHz. The conductances and capacitances between each pair of electrodes are calculated applying an AC signal in turn to each j-electrode and taking real and imaginary parts of admittance matrix between i and j electrodes, i.e. $G_{ij} = \text{Re}(Y_{ij})$, $C_{ij} = \text{Im}(Y_{ij}/\omega)$. The presented simulations were performed for FD transistors operated in the saturation regime but avoiding the influence of the kink effect. Typical simulated output conductance G_{SD} vs frequency curves are presented in figure 2. The curves usually exhibit 3 transitions, with characteristic frequencies (f_C) of about 10^2 , 10^7 and 5×10^8 Hz for transistors with effective channel length of $0.16 \mu\text{m}$. The second transition with $f_C \sim 10^7$ Hz is explained by SH effect, which was extensively examined in many papers [2-4]. We will focus on the first and third zero-pole doublets, which are caused by the feedback through the substrate and have no relation with the SH effect, as proved by the simulations either without SH, or without substrate, or with different substrate dopings (fig. 2).

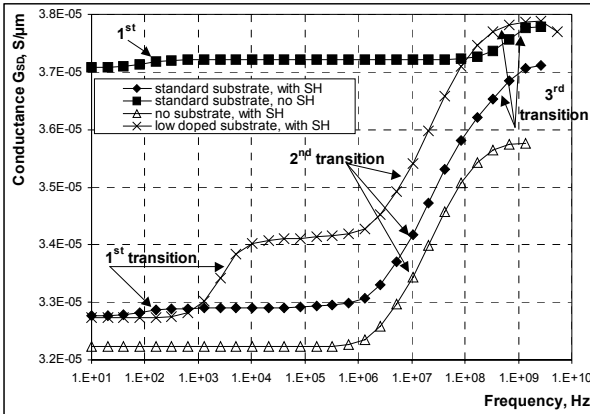


Figure 2. Simulated frequency dependence of G_{SD} . $L_{\text{eff}} = 0.16 \mu\text{m}$, $V_D = V_G = 1\text{V}$

Figure 3 presents a deeper insight on the behaviour of the first transition normalized to the 10 Hz G_{SD} value. Both the characteristic frequency (f_{C1}) and the high-plateau value are strongly dependent on the applied biases. The observed low-frequency increase of the output conductance in our FD simulations may look similar to what was previously observed in PD devices and was related to floating body [1, 5]. However, as inferred from [5], internal coupling in the thin film

device between device accesses and body node through junction impedances is not expected to show a dependence of f_C on the applied biases and substrate doping. In our case we observed such dependences (insert to fig. 3). We interpret that in our case this transition is caused by the electrical coupling through the substrate, as proved by the simulations which do not include the substrate. In this case neither 1st nor 3rd transitions are observed (fig. 2).

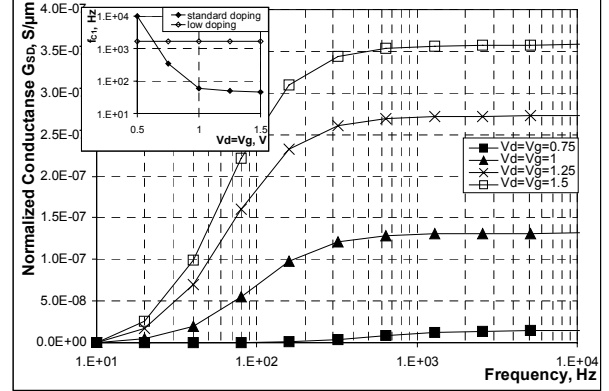


Figure 3. First transition on G_{SD} curve for different applied biases. In insert: f_{C1} vs $V_D = V_G$. $L_{\text{eff}} = 0.16 \mu\text{m}$.

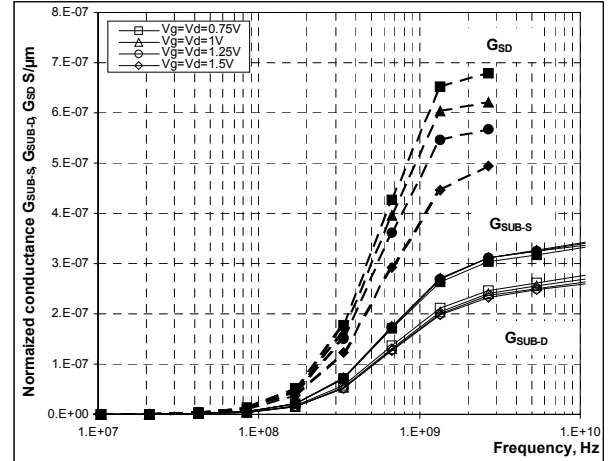


Figure 4. Normalized source-drain, source-substrate and drain-substrate conductances vs frequency for different applied biases. $L_{\text{eff}} = 0.16 \mu\text{m}$.

In figure 4, the 3rd high-frequency transition is detailed. It should be pointed out that it is not always easy to observe this transition alone, because it can be partially masked by the strong transition due to SH effect (fig. 2), especially for high gate biases and short channel lengths, and hence high drain current densities. Simulations without SH or for the conditions in which SH is small (e.g. for low gate biases) were then used to discriminate the 3rd transition. Figure 4 shows that the amplitude of this transition only slightly depends on the applied bias whereas the characteristic frequency is bias independent. Moreover, it should be stressed that this transition has the same characteristic frequency as the transition occurring in the source and drain conductances to the substrate, i.e. G_{SUB-S} , G_{SUB-D} curves presented in figure 4.

This leads to the understanding that the source and drain nodes are connected to the underlying substrate through the buried oxide. In fact, under the silicon film, we have a structure analogous to the simple MOS capacitor whose parallel capacitance and conductance are strongly dependent on the frequency and on the space-charge condition at the silicon-oxide interface. Figure 5 presents the simulated substrate-source and substrate-drain capacitances vs frequency for FD MOSFET under different bias conditions. These curves exhibit two transitions with characteristic frequencies corresponding to the frequencies at which firstly minority, and then, majority carriers are no more able to follow the AC signal. It is worth to emphasize that these frequencies are exactly the same as the characteristic frequencies of 1st and 3rd transitions on the G_{SD} curve. Moreover, the simulations performed for low-doped substrate, presented in figure 5b, demonstrate a higher value of first transition with no dependence on the bias, which agree well with simulations of output conductance (fig.2, insert in fig.3). The reason of such behaviour is that for the same bias range, the low-doped substrate is always strongly inverted from the source to the drain side, independently on the applied biases, whereas the standard doped substrate is weakly inverted only near drain and the amount of the inversion charge is strongly bias dependent. This explains why for the case of standard-doped substrate the step of 1st transition in C_{SUB-D} curve is strongly bias dependent and larger than in C_{SUB-S} , whereas for the case of low-doped substrate, these values are nearly the same and have no dependence on applied biases.

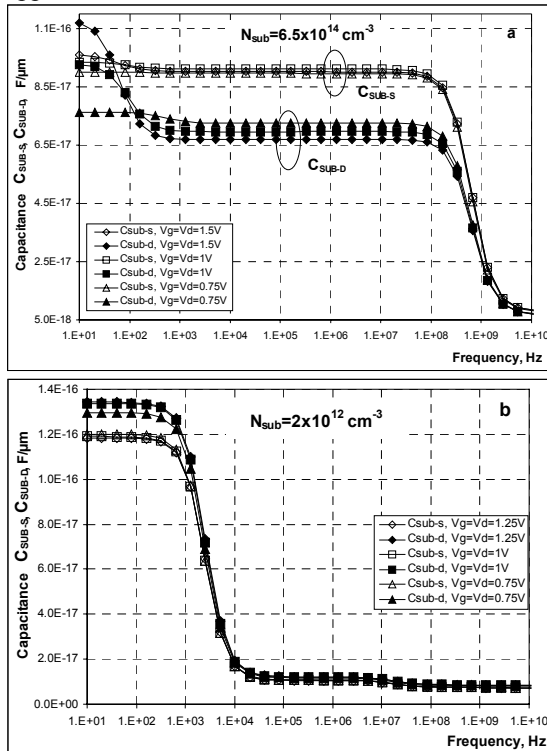


Figure 5. Substrate-source and substrate-drain capacitances vs frequency for different biases. (a) standard, (b) low-doped substrate. $L_{eff} = 0.16 \mu\text{m}$.

4. Modelling

In this section we propose a small-signal equivalent circuit which, at a first order, can model the substrate-related frequency behaviour of the drain-to-source conductance. As explained in the previous sections, a model of the substrate must be added to the classical small-signal model of the transistor. It is represented in figure 6 for both PD and FD MOSFETs, based on [8]. The indices S, D, G, B and BG respectively refer to the source, drain, gate, floating body (in PD only) and back gate (at the interface with the buried oxide). The space charge region in the substrate is modelled by a capacitance C_{SC} and an equivalent resistance R_{SC} whose values depend on bias and substrate doping. This R_{SC}/C_{SC} network introduces the frequency response of the minority carriers which, when frequency increases, cannot follow the signal variations anymore, so that C_{SC} appears in series with the capacitance connecting the drain to the substrate through the buried oxide, i.e. C_{BGD} . The capacitance C_{Si} and resistance R_{Si} model the inertia of the majority carriers in the silicon substrate. At very high frequency indeed, the capacitance of the substrate falls to a low pure dielectric capacitance value due to the finite relaxation time of majority carriers [8].

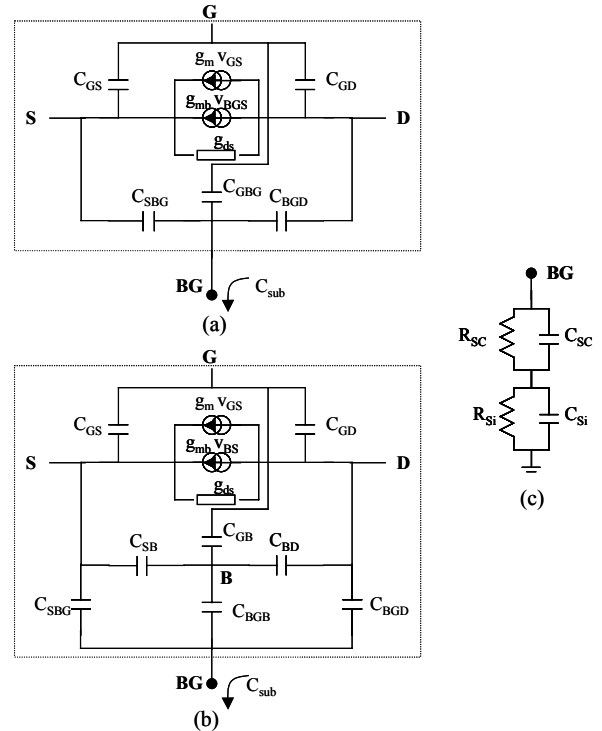


Figure 6. Small-signal equivalent circuits (a) FD; (b) PD; (c) Substrate model

When an AC signal is applied to the drain, a feedthrough appears in the substrate which leads to a variation of the back gate-to-source voltage, i.e. V_{BGS} . For FD, this variation directly results in an additional drain to source conductance component through the substrate transconductance element g_{mb} of the intrinsic device. In PD, the floating body is coupled to the back gate through the capacitance C_{BGB} , resulting in a

variation of the drain to source conductance via g_{mb} as well. To the first order, we can write

$$\begin{aligned} \text{in FD: } \Delta G_{SD} &= g_{mb} \cdot \frac{\Delta V_{BGS}}{\Delta V_{DS}} = (n_{FD} - 1) \cdot g_m \cdot \frac{\Delta V_{BGS}}{\Delta V_{DS}} \\ \text{in PD: } \Delta G_{SD} &= g_{mb} \cdot \frac{\Delta V_{BS}}{\Delta V_{DS}} \\ &= (n_{PD} - 1) \cdot g_m \cdot \frac{C_{BGB}}{C_{BGB} + C_{GB} + C_{SB}} \cdot \frac{\Delta V_{BGS}}{\Delta V_{DS}} \end{aligned} \quad (1)$$

where n_{FD} is the FD body effect factor and n_{PD} is the PD one.

Both small-signal equivalent circuits of figure 6 were simulated on Matlab. The values of the different elements were reasonably fixed according to the circuit models available for these devices, at similar bias conditions. As first approximation, the elements of the substrate model were estimated using the equations of a SOI MOS capacitance in inversion mode [8]. Similarly to ATLAS simulations without self-heating, we observe two transitions of the output conductance vs. frequency (fig. 7). These are due to the variations with frequency of the global substrate capacitance C_{sub} appearing between BG and the grounded back electrode as a combination of the elements of the substrate model of figure (6.c).

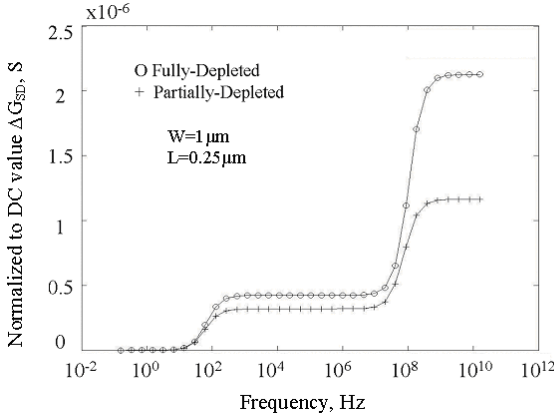


Figure 7. Matlab calculated ΔG_{SD} for FD and PD

At low frequency, in inversion, BG is almost grounded. The first zero-pole doublet is related to the C_{SC}/R_{SC} pair. When $\omega \cdot C_{SC}$ becomes larger than R_{SC}^{-1} , C_{sub} tends to C_{SC} and the potential at BG increases. As a first approximation, we can write

$$\text{in FD: } \Delta V_{BG} \cong \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{GBG} + C_{sub}} \cdot \Delta V_D \quad (2a)$$

$$\text{in PD: } \Delta V_{BG} \cong \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{sub}} \cdot \Delta V_D \quad (2b)$$

This results in an increased output conductance (eq. (1)). The high frequency transition in the conductance spectrum then appears in the dielectric node of the substrate when $\omega \cdot C_{Si}$ becomes larger than R_{Si}^{-1} , C_{sub} tending to C_{Si} .

The output conductance increases are similar in FD and in PD since the much larger value of n_{PD} ($\cong 1.2$ here), compared to n_{FD} ($\cong 1.02$), is compensated by the capacitive divider present in PD between BG and the

floating-body node (eq. 1). This indicates for the first time that a dynamic back gate coupling effect can appear in PD SOI MOSFETs through the underlying substrate.

5. Conclusions

Results of measurements and 2D numerical simulations of the small-signal characteristics of SOI MOSFETs in the frequency range up to 5 GHz are presented. For the first time, we have demonstrated that electrical coupling through the substrate results in two additional transitions in the output conductance vs frequency curves with the characteristic frequencies of $\sim 10^2$ Hz and $\sim 5 \times 10^8$ Hz both for FD and PD devices. An analytical model which includes influence of the substrate on the output conductance characteristics has been proposed. The study can be extended to the other small signal characteristics as well.

Acknowledgments

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