Reverse-Order Source/Drain (R-S/D) Combined with LDD Offset Spacer and Its Application to 50nm Physical-Gate-Length nMOSFETs

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Abstract

50nm physical-gate-length nMOSFETs were realized on the basis of the reverse-order source/drain (R-S/D) formation and the LDD offset spacer. By combining the advantages of both technologies, we could get the optimised device performance in terms of drive current and short channel effect. In addition, process steps could be reduced and simplified in comparison with other disposable sidewall processes. According to the measured and simulated results, the R-S/D combined with the LDD offset spacer can be applied to sub-50nm device fabrication and accelerate the rate of scaling-down.

1. Introduction

There has always been trade-off between drive current and short channel effect in MOS devices. The short channel effect has been one of the biggest obstacles to channel length reduction. Moreover, the situation gets worse with device scaled down to sub-50nm regime. To overcome this problem, many studies have been reported up to now. In this paper, we focus on the R-S/D formation and the LDD offset spacer.

In the first place, the R-S/D reverses the process sequence of S/D extension and deep S/D implantation. To implement this idea, the disposable sidewall process was proposed and developed [1, 2]. In conventional CMOS process, S/D extension formation is followed by deep S/D implantation and RTA (Rapid Thermal Annealing) is carried out simultaneously, which makes it hard to optimise conflicting thermal budgets. Adopting the R-S/D, we can meet the different demand in each process step at the same time: high thermal budget for gate and deep S/D can be allowed. It is reported that higher device performance is obtained using the R-S/D due to less poly gate depletion and more abrupt extension junctions [2]. However, the process mentioned above needs additional process steps and very high selective etching to remove remaining sidewall spacer completely.

Secondly, the LDD offset spacer was introduced to compensate low drive current which results from S/D extension depth reduction for short channel effect suppression [3]. In addition, it makes device design easier in the optimisation between gate delay (CV/I) and drive current (I_{ON}) [4]. There are, however, some drawbacks in this process such as drive current lowering induced by parasitic resistance increase.

In this paper, we will combine the merits of the R-S/D and the LDD offset spacer and make the process flow simpler and easier.

2. Device structure

Fig. 1 shows the key process flow to fabricate the nMOSFET with the R-S/D and the LDD offset spacer. By and large, it is compatible to the contemporary CMOS technology. The process was performed as follows. After LOCOS isolation, 1nm thick gate oxide was grown by RTO (Rapid Thermal Oxidation) as shown in Fig. 2. 100nm thick poly-Si layer was deposited on gate oxide and gate doping was done. To define 50nm gate line, we have utilized a novel lithography process: the sidewall patterning technique depicted in Fig. 3. We have already demonstrated the accurate, uniform and reproducible feature of the sidewall patterning technique [5]. Table 1 reveals the superiority of the sidewall patterning over the e-beam direct writing method. TEOS deposition and etch follows gate line patterning in order to form disposable sidewall spacer. As^+ implantation was carried out for deep S/D formation. TEOS sidewall spacer overetch was done for sidewall width reduction in proportion to the overetch ratio. The remaining sidewall acts as an LDD offset spacer. The disposable sidewall process proposed up to now claimed the complete elimination of sidewall spacer. Therefore, additional barrier layer was necessary and high selective etching was critical. However, our process needs no barrier layer and high selectivity. More than 10:1 selectivity between TEOS and Si is sufficient, which is accomplished easily in conventional reactive ion etcher. TEOS sidewall spacer overetch was followed by an annealing step. Annealing was added to activate dopant in deep S/D fully and cure damage from implantation and RIE. Annealing time and temperature can be set longer and higher, respectively, than those in conventional annealing process because no S/D

extension implantation was done before. Leaving the LDD offset spacer, we carried As_2^+ low energy implantation for S/D extension formation. With the offset spacer, we can modulate the effective channel length and gate overlap, therefore, alleviate short channel effect and overlap capacitance. To activate dopant with minimized diffusion time, RTA process was adopted and then TEOS deposition and etch could be used for silicidation. However, in this study, no silicidation process was introduced.

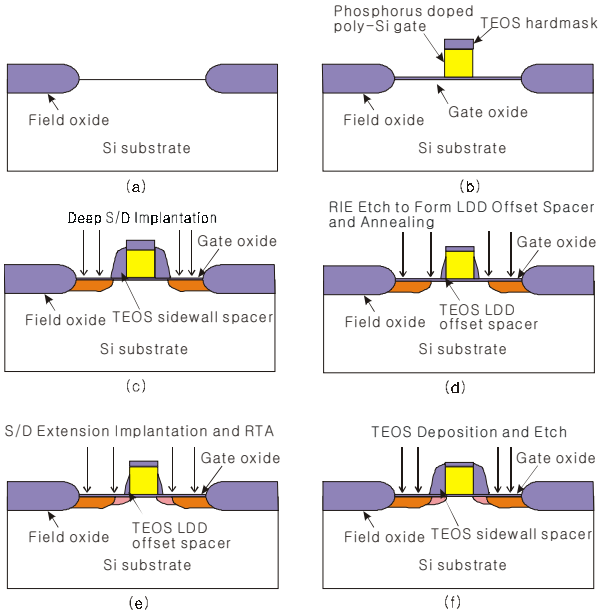

Figure 1. Key process steps for the proposed structure: (a) LOCOS isolation (b) gate oxidation and gate line patterning using RTO and sidewall patterning technique, respectively (c) deep S/D implantation with As^+ (d) TEOS overetch to form LDD offset spacer and annealing (e) S/D extension implantation with As_2^+ and RTA optimised for S/D extension (f) TEOS deposition and etch to recover sidewall spacer

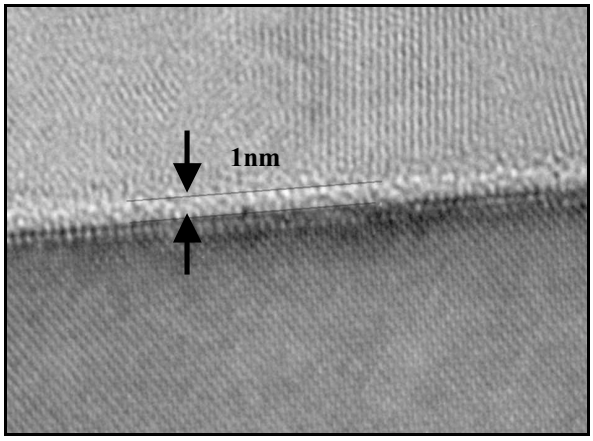

Figure 2. 1nm thick gate oxide grown by RTO (Rapid Thermal Oxidation) process

Table 1. Comparison between sidewall patterning technique and e-beam lithography

	Sidewall patterning		E-beam	
Line width (nm)	50	80	80	130
Average conductance (μS)	8.00	9.49	3.86	13.13
Standard dev.	0.27	0.14	3.02	3.88
Deviation (%)	3.38	1.48	78.24	29.55

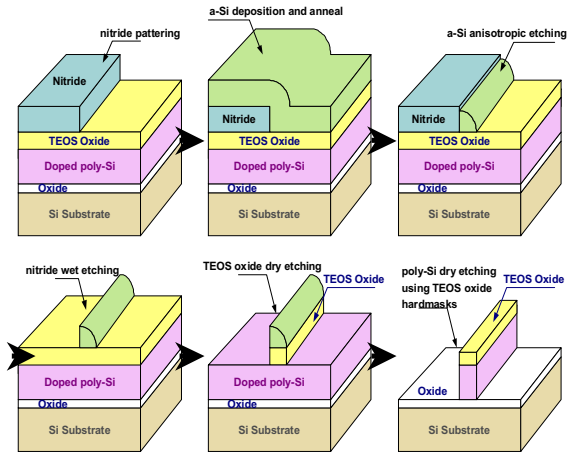

Figure 3. Process flow of sidewall patterning technique

3. Simulation results

We have compared our proposed structure with the conventional one through MEDICI simulation. The proposed structure has the same physical-gate length with the others. Table 2 illustrates the various conditions used in simulation. Unlike the conventional structure, the LDD spacer structure adopts only the LDD offset spacer while the proposed structure has both the R-S/D and the LDD offset spacer.

Table 2. Various structures used in simulation

	conventional structure	LDD spacer structure	proposed structure
R-S/D	X	X	O
LDD spacer	X	O	O
S/D extension implant	As_2^+ 5keV	As_2^+ 5keV	As_2^+ 5keV
Anneal for deep S/D	1000°C 3s (at the same time)	1000°C 3s (at the same time)	1000°C 20s
Anneal for S/D extension			1000°C 3s

Table 3 summarized the simulated electrical characteristics of the three structures explained in Table 2. As expected, there are conflicting relations between the conventional structure and LDD offset spacer structure in drive current and short channel effect. However, by adopting the proposed structure, we can achieve drive current improvement with short channel effect alleviated. Based on the simulation result, we fabricated 50nm physical-gate-length nMOSFETs following the conventional and the proposed process.

Table 3. Simulated device characteristics of the devices in Table 2

	conventional structure	LDD offset structure	proposed structure
I_{ON} (μA/μm) V_G-V_T= 0.9V	738	664	750
DIBL (mV/V)	88	48	67
SS (mV/dec)	85	67	74

4. Experimental

In the abovementioned simulation, we confirmed that the combination of the R-S/D and the LDD offset spacer improved drive current with short channel effect suppressed. Devices with the conventional structure and with the proposed structure were fabricated following the process in Table 2.

Figure 4 illustrates the transfer characteristic comparison between the conventional device and the proposed one. Since we did not apply any silicidation process, the drive current is somewhat low compared with other devices but we have no problem in analyzing the effect of the R-S/D and the LDD offset spacer.

As depicted in Fig. 4, the proposed structure which combines the R-S/D with the LDD offset spacer shows suppressed short channel effect with minimum drive current degradation. Considering the fact that it has higher threshold voltage, we can expect more drive current in the same overdrive (V_G - V_T) condition. Some electrical characteristics of the devices are summarized in Table 4. Referring to the table, we can get 10% drive current enhancement and 60% DIBL suppression by adopting the LDD offset spacer merged with the R-S/D. Finally, it is concluded that we can scale devices down to sub-50nm regime by combining R-S/D with LDD offset spacer.

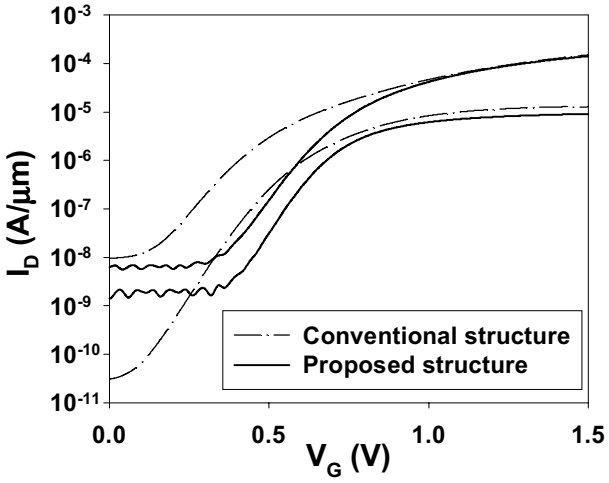

Figure 4. Transfer characteristic comparison between the conventional device and the proposed one

Table 4. Device characteristic comparison between the conventional device and the proposed structure

	conventional structure	proposed structure
V_T (mV)	450	550
I_{ON} (μA/μm) V_G-V_T= 0.95V	128	142
DIBL (mV/V)	120	50
SS (mV/dec)	100	100

5. Conclusion

In this paper, we confirmed that the LDD offset spacer merged with the R-S/D could enhance device performance: both drive current and short channel behavior. In addition, it can be achieved with relatively simple and easy process. It was found that the proposed structure enhanced drive current by 10% and suppressed DIBL by 60%. In conclusion, faster and more aggressive device scaling-down is expected by combining the R-S/D and the LDD offset spacer.

Acknowledgement

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