

# Understanding nMOSFET characteristics after soft breakdown and their dependence on the breakdown location

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## Abstract

*Identical breakdown-position dependence of normalized currents in nFETs with 2.4 nm gate oxide is observed after soft and hard breakdowns. This suggests that electron energy is conserved in the soft breakdown path. It is concluded that the observed soft breakdown is best modeled by a lowered oxide barrier in the breakdown conduction path. The static behavior of an nFET immediately after SBD is discussed and tested using the MEDICI device simulator.*

## 1. Introduction

Although the occurrence of the first gate insulator breakdown in FETs at operating conditions is still difficult to predict, the consensus grows that it will be relatively soft, because of the limited power supplied at the moment of breakdown [1-3].

In order to predict if such soft breakdown (SBD) will represent a problem from the customers' perspective, it is important to fully understand if and how SBD influences FET operation [4]. We have previously studied this question for the more pronounced case of hard gate oxide breakdown (HBD). Gaining detailed understanding of how HBD influences nFET operation allowed us to conclude that some (digital) CMOS circuits will be robust against hard breakdown [5].

In this paper we continue this research for the more relevant case of SBD in 2.4 nm gate oxide. We find that although the current through the SBD spot is highly non-linear and several decades lower than the previously studied HBD, it in many respects influences the nFET operation in a fashion similar to the HBD. We combine this knowledge and build a static model for nFET immediately after SBD. This brings us closer to answering the question as to whether such breakdowns will affect FET and CMOS circuit operation.

## 2. Experimental

Our analysis was performed on nFETs with gate length  $L = 0.18 \mu\text{m}$  and width  $W = 10 \mu\text{m}$ , and ellipsometric gate oxide thickness  $t_{\text{ox}} = 2.4 \text{ nm}$ , fabricated with an optimized  $0.13 \mu\text{m}$  CMOS process. 100 nFETs

were stressed in accumulation, with the gate (G) at  $V_G = -4.4 \text{ V}$  and with the source (S), the drain (D), and the substrate (W) grounded ( $V_S = V_D = V_W = 0 \text{ V}$ ). This stress resulted almost entirely in SBDs. As a reference, 100 nFETs were stressed in inversion ( $V_G = 4.4 \text{ V}$ ), resulting mostly in HBDs. Both these stress conditions yielded breakdowns approximately uniformly distributed along the whole length of the gate [6]. A  $10\text{k}\Omega$  series resistance was used to limit the gate current increase at the moment of breakdown and to mimic the limited current supplied by the driving FETs in real circuits [5]. The stress was stopped immediately after the first breakdown to avoid further damage generation in the oxide [7].

After breakdown, with the series resistance removed, currents at all terminals were measured in the limited range of  $V_G = -1.5 \text{ V}$  to  $1.5 \text{ V}$  and  $V_D = 0$  to  $1.5 \text{ V}$  to avoid generation of additional damage in the FET or the breakdown path. Positions of breakdown spots along the FET gate lengths were determined using the methodology reported earlier [5, 8].

Device simulations were carried out with the MEDICI v2001.4 two-dimensional device simulator. The SBD path was represented by a narrow (6 nm) region of oxide with lowered barrier. Due to the nature of this representation, the TSUPREM4  $0.13 \mu\text{m}$  process simulation results could not be used in this case and the nFET had to be "recreated" analytically within MEDICI. The calculations were carried out with the energy balance equations solved self-consistently within the device equations. Direct tunneling of electrons was included self-consistently.

## 3. Initial Observations

The effective post-breakdown resistance  $R_G$ , defined as  $V_G/I_G$  at  $V_G = 1.5 \text{ V}$  and  $V_S = V_D = V_W = 0 \text{ V}$ , is shown in Fig. 1a for the nFETs stressed in accumulation as a function of the breakdown position  $x$  (defined in Fig. 3a). For comparison, we show the same variable for devices stressed in inversion in Fig. 1b. While the stress in inversion resulted in mostly HBDs with a few SBDs in the center, the accumulation stress resulted almost entirely in SBDs [6, 8]. The magnitude of SBDs in both devices is similar.

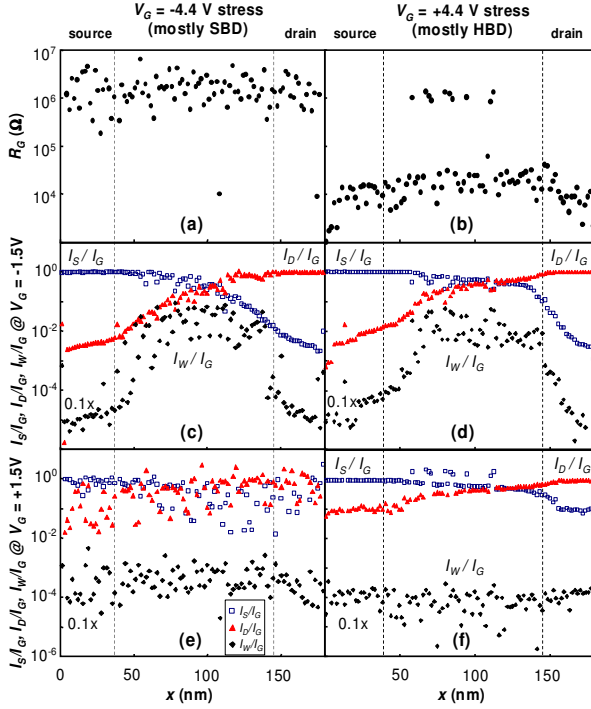


Figure 1. The post breakdown effective resistance  $R_G$  profile along the length of the nFET gate shows (a) mostly SBDs and (b) mostly HBD for devices stressed in (a) accumulation and (b) inversion, respectively. Although the BD modes and their  $I$ - $V$  characteristics are substantially different, the  $I_G$ -normalized current profiles for (c)(d) negative and (e)(f) positive measurement  $V_G$  are almost identical, suggesting the same ballistic carrier transport through both SBD and HBD paths. Note that the smaller SBD signals are inherently more noisy.

Fig. 2a then demonstrates the highly non-linear nature of the  $I_G$ - $V_G$  characteristics of a SBD spot at  $x = 0 \mu\text{m}$ , i.e., over the source extension. Note that in this case the breakdown path is surrounded by n-type regions (see Figs. 3a and c). A HBD path at the same gate position obtained on devices stressed in inversion showed purely ohmic behavior (not shown) [5].

#### 4. SBD and HBD Carrier Transport

When we, however, compare the nFET currents normalized by  $I_G$  after both SBD and HBD, we find that their breakdown-position profiles are remarkably similar (Figs. 1c-d and 1e-f). The dependence of nFET currents after HBD on breakdown position was explained previously [5]. The mechanisms are summarized in Fig. 3. At sufficiently negative  $V_G$ , for gate-to-source extension breakdown ( $x = 0L$ , Fig. 3a), hot electrons are ballistically injected from the gate through the breakdown path into the extension, where the majority of them relaxes and contributes to  $I_S$ . A small fraction of the hot electrons is able to overcome the n+/p junction between the extension and the substrate and contributes to  $I_W$  and  $I_D$ . For breakdown spots closer to the n+/p junction, the fraction of hot electrons reaching this barrier increases,

and correspondingly,  $I_W$  and  $I_D$  increase (Fig. 1d). The mean relaxation distance of hot electrons in the extension can be then directly determined from the  $I_W$  or  $I_D$  increase with  $x$  to be  $\sim 10 \text{ nm}$  [5]. The holes created by impact ionization flow through the breakdown path back into the gate.

For gate-to-substrate breakdowns at negative  $V_G$  (Fig. 3b), hot electrons are injected directly into the substrate, where they either recombine, contributing to  $I_W$ , or are collected at the source and the drain as  $I_S$  and  $I_D$ , with the weight shifting from  $I_S$  to  $I_D$  as the breakdown spot moves from the source to the drain (Fig. 1d). Again, the characteristic length scale of this process can be directly extracted from the figure to be  $\sim 100 \text{ nm}$ . The native substrate holes flow through the breakdown path back into the gate.

At sufficiently positive  $V_G$ , a conductive channel is created in the substrate. Hot electrons are ballistically injected from extensions (Fig. 3c) or the channel (Fig. 3d) into the gate. The decrease of  $I_S$  and the increase of  $I_D$  with increasing  $x$  (Fig. 1f) are given by the relative conductances of the paths between the source and the drain contacts and the breakdown spot. The substrate current is caused by backflow of holes created by electron impact ionization (Fig. 1f).

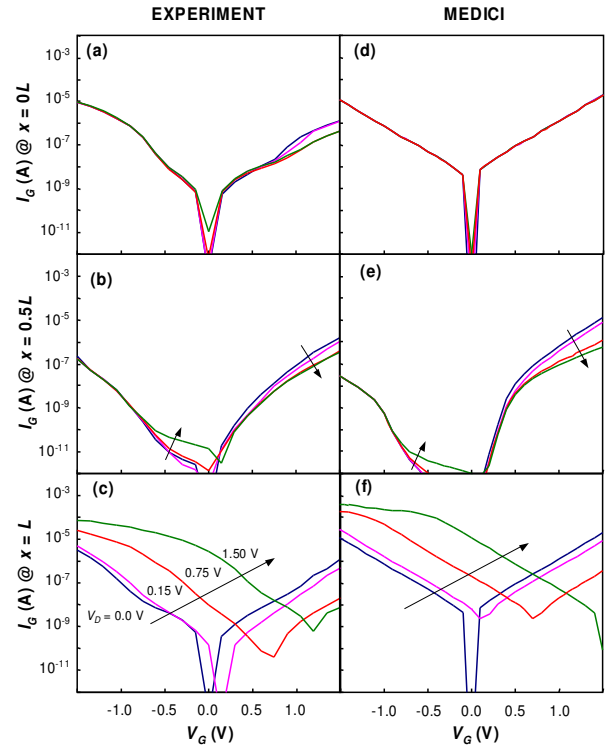


Figure 2. (a)-(c) Post-breakdown characteristics obtained on nFETs stressed in accumulation with SBD located at (a)  $x = 0L$ , (b)  $x = 0.5L$ , and (c)  $x = L$  as a function of  $V_G$  and  $V_D$ . The resulting characteristics are highly non-linear. The increasing influence of  $V_D$  with increasing  $x$  is apparent. (d)-(f) MEDICI calculation ( $W = 10 \mu\text{m}$ ) for corresponding positions well reproduces the main features of the measured characteristics.

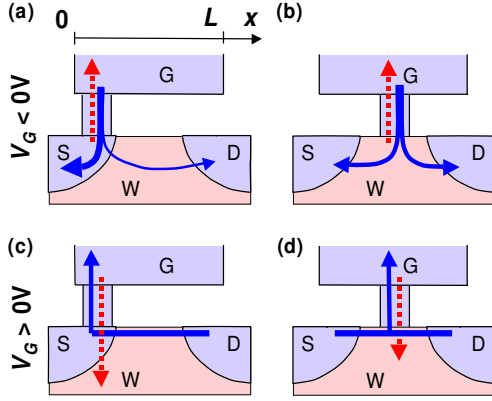


Figure 3. Summary of electron (solid arrows) and hole (broken arrows) flow in nFET after (a)(c) gate-to-extension and (b)(d) gate-to-channel oxide breakdowns for (a)(b) negative and (c)(d) positive gate voltages. The definition of breakdown position  $x$  is given in (a).

From the above it is apparent that the exact ratios of  $I_S$ ,  $I_D$ , and  $I_W$  and their variations with  $x$  depend strongly on the transport mechanism through the breakdown path. The strong resemblance of the SBD and HBD normalized-current profiles (Figs. 1c-f) therefore leads us to conclude that the electron transport via the observed SBD paths has the same properties as the HBD case, i.e., *the energy of electrons moving through the SBD path has to be conserved*.

As a side comment, we note that the data presented in Figs. 1c-f are slightly asymmetric, centered about  $x = 0.6L$ . This could be caused either by asymmetric junctions or by the oxide being slightly weaker at the source side, resulting in more BDs in that region. We propose that the above-described methodology can be a valuable tool for evaluating e.g. process effects on device geometries or oxide uniformity [6].

Also, since the effect of SBD and HBD on the nFET are similar, the equivalent circuit constructed previously for HBD can be reused for SBD, with a non-linear resistor representing the oxide breakdown path [5, 9].

## 5. SBD Modeling

We have previously established that the HBD path is well simulated by a direct, narrow semiconducting contact between the nFET gate and the substrate [5]. In contrast to that, the non-linear  $I_G$ - $V_G$  characteristic (Fig. 2a) after SBD suggests that even though oxide integrity at the SBD spot has been corrupted, a partial oxide barrier still exists for electrons in the breakdown path. i) Thinning (Fig. 4a) and ii) lowering (Fig. 4b) of the original oxide barrier have been proposed to describe the partial barrier controlling the transmissivity  $Tr$  through the SBD path [10-12]. To determine which of the two effects will better describe the steep  $\log I_G$ - $V_G$  SBD characteristic in Fig. 2a, we now discuss the effect of  $V_G$  on  $Tr$  for both cases (the combination of barrier lowering and thinning is neglected for simplicity). For that we

employ the fact that the current flowing through the SBD spot is simply proportional to  $Tr$  at higher  $V_G$ 's.

Fig. 4c shows that both thinning and lowering of the original barrier indeed result in increased transmissivity  $Tr$  at  $V_G = 1$  V. The switching rate of the barrier, given by  $\Delta \log Tr / \Delta V_G$ , depends, however, on the shape of the barrier [13]. For the same  $V_G$  increase, the area of the thinned barrier (Fig. 4a) decreases less than the area of the lowered barrier (Fig. 4b) resulting in a smaller increase in  $Tr$  (Fig. 4d). We therefore conclude that the slope of the measured  $\log I_G$ - $V_G$  SBD curves (2-3 decades / 1 V, see Fig. 2a) can be best achieved by *lowering* the oxide barrier in the SBD path. This approach is used in our MEDICI simulations.

We also note that the similar backflow of holes for SBD and HBD at  $V_G = +1.5$  V ( $I_W / I_G$  in Figs. 1c and d) suggests that only a very small barrier exists for holes in the SBD path. This is consistent with Ref. [11].

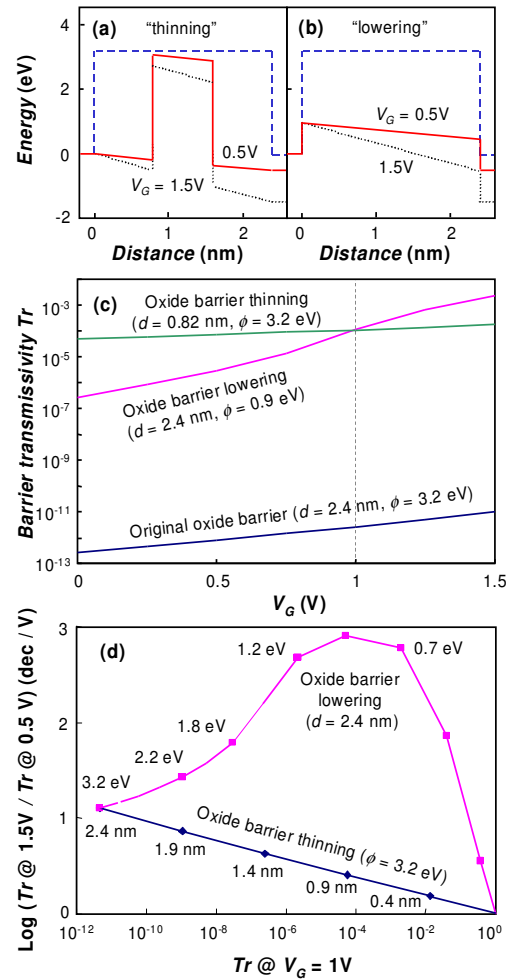


Figure 4. (a) (b) Illustration of two approaches to modeling SBD: the original gate oxide barrier (dashed line) of thickness  $d$  and height  $\phi$  is reduced by (a) oxide barrier thinning and (b) oxide barrier lowering. (b) The lowered barrier decreases more than (a) the thinned barrier between  $V_G = 0.5$  and  $1.5$  V. (c) (d) For given WKB tunneling probability  $Tr$ , oxide barrier lowering produces steeper  $Tr$ - $V_G$  dependence than barrier thinning.

## 6. MEDICI Modeling Results

The MEDICI calculation results with the oxide barrier lowered to 0.9 eV in a narrow region of the gate oxide representing the SBD path are shown in Figs. 2 and 6. Both figures show that all major currents are well reproduced by the calculations. Some discrepancy can be accounted by the fact that the nFET had to be constructed in MEDICI and the real device is therefore not fully represented in the calculation. For example, the doping concentration levels at both sides of the SBD path will influence the symmetry of the  $I_G$ - $V_G$  curves.

Fig. 6 further shows that some secondary effects, such as  $I_W$  and  $I_D$  for the  $x = 0L$  case and  $I_W$  and  $I_S$  for the  $x = L$  case at  $V_G < 0V$ , are not reproduced by the calculation. This is because the present version of MEDICI used in our calculations does not include transfer of energy of carriers during tunneling through the oxide. Consequently, electrons injected into the extensions do not have sufficient energy to enter the substrate and contribute to  $I_W$  and  $I_D$  (in the  $x = 0L$  case) or  $I_W$  and  $I_S$  (in the  $x = L$  case). For the same reason the calculation does not reproduce  $I_W$  at  $V_G > 0V$ —electrons tunneling into the gate are not sufficiently energetic to create holes responsible for  $I_W$ . This incompleteness of the calculation therefore further supports the proposed picture where the conduction through our SBD path has to occur ballistically to correctly reproduce our data.

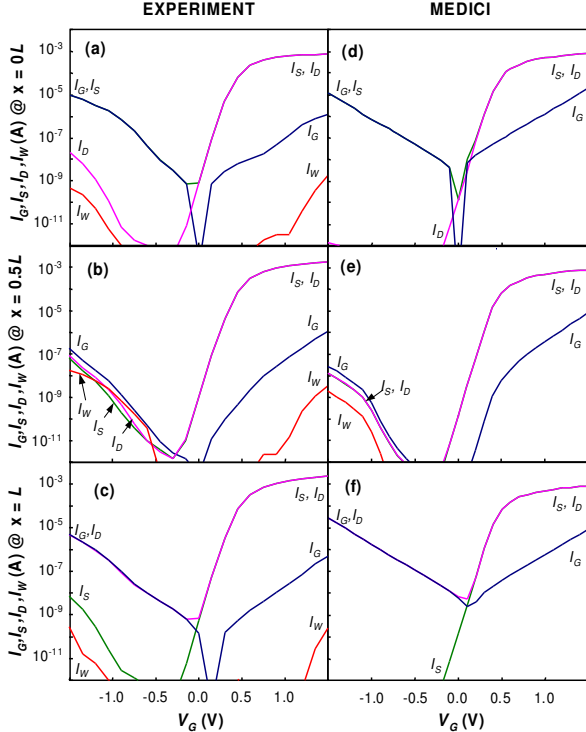


Figure 6. (a)-(c) All nFET currents for the same 3 samples as in Fig. 2, measured at  $V_D = 0.15V$  and  $V_S = V_W = 0V$  and (d) - (f) the corresponding the MEDICI calculation. Major effects are correctly reproduced by the calculation, while secondary effects are not due to non-conserved energy during tunneling.

## 6. Conclusions

We constructed a simple model for SBD and used it to discuss the static behavior of nFET immediately after SBD. We concluded that the SBD in our case is best modeled by a lowered oxide barrier in the SBD conduction path. This approximates well the non-linear  $I$ - $V$  curve behavior, while it allows for electron energy conservation in the SBD path, so that the same current-breakdown position dependencies as in the HBD case are reproduced.

## 7. Acknowledgements

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