Raised Source/Drain on 50nm CMOS Circuits : Propagation Delay and Dynamic Power Optimizations

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Abstract

Based on 50 nm experimental n-pMOSFETs processed with 1.4 nm oxide thickness, simulated raised source/drain have been evaluated in terms of propagation delays and dynamic power consumptions. Circuit simulations were carried out with BSIM4.1 model putting forward that a special care has to be paid to parasitic capacitances to keep reasonable dynamic consumptions while improving propagation delays.

1. Introduction

CMOS Ultimate Integration will soon require ultra shallow junctions in order to keep control of short channel effects [1]. However such thin junctions lead to an increase of parasitic resistance, detrimental to transistor performance. Moreover, salicidation process carried out on these junctions is an issue and may induce larger diode leakage in the vicinity of silicide/silicon interface. Raised source/drain (RSD) and spacer thinning are known to be a satisfactory solutions to these problems [2]. Nevertheless, they also enlarge gate to source/drain capacitances which degrade dynamic performances [3]. In this work, starting from DC BSIM4.1 model card extracted on 50 nm non-elevated n-pMOSFETs, the impact of simulated RSD on simple circuit performances is studied. This approach is more relevant than studies which only deal with Ion-Ioff trade-off [4] since it emphasizes on dynamic parasitic elements.

2. Device description and parameter extraction

50 nm n-pMOS transistors were fabricated following a conventional CMOS process. After isolation and channel implantations, a 1.4 nm thick gate oxide was thermally grown by Rapid Thermal Oxidation at 800°C. Both N+ and P+ gates were pre-doped in order to reduce gate polysilicon depletion and to optimise separately gate and source/drain. Gates were patterned using e-beam/Deep-UV hybrid lithography followed by a mixed dry and wet hard mask etch [5]. BF_2 (Arsenic) pockets were carefully implanted in n(p)MOSFET to ensure better short channel effect control and low junction capacitance degradation. After dopant activation, fabrication was completed with a conventional metallization process. As these devices feature a good control of short channel effects (figure 1), BSIM4.1 DC parameters were extracted following a strategy essentially based on local optimizations [6]. This compact model includes a gate direct tunnelling current, poly-depletion and quantum mechanical effects [7]. Main parameters are gathered in table 1.

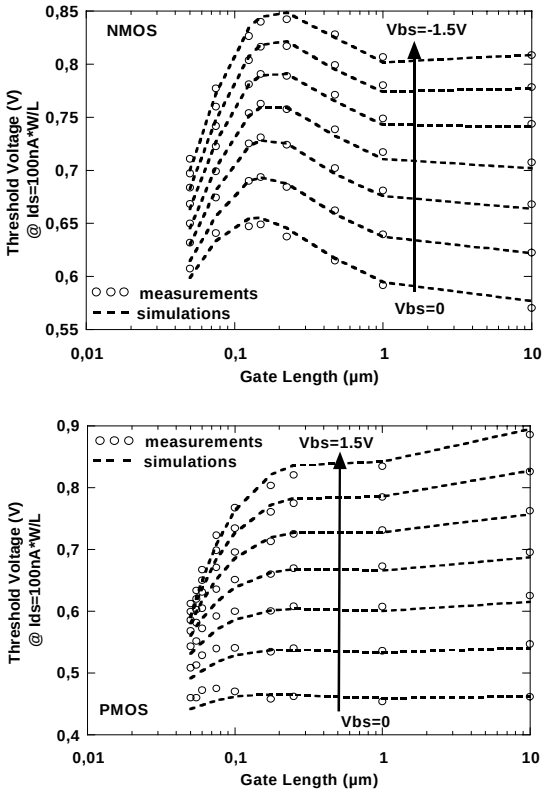


Figure 1. n-pMOSFET threshold voltage dependence on the gate length (W=10µm)

Electrical oxide thickness was set up at 1.67 (1.7) nm for n(p)MOS to take into account quantum mechanisms. High parasitic resistances were extracted on these devices since source/drain were not silicided. Simulations of 50nm n-pMOSFETs currents are put side by side with measurements on figure 2.

Table 1. 50nm n-pMOSFET parameters

	NMOS	PMOS
Physical oxide thickness (nm)	1.4	1.4
Electrical oxide thickness (nm)	1.67	1.7
Poly-silicon gate doping (cm^{-3})	7.10^{19}	8.10^{19}
Threshold voltage (V)	0.59	-0.43
Low-field mobility (cm^2/Vs)	196	63
Parasitic resistance (Ω.µm)	1580	1020
Area junc. capacitance ($fF/\mu m^2$)	1.92	1.9
Miller capacitance (fF/µm)	0.44	0.41

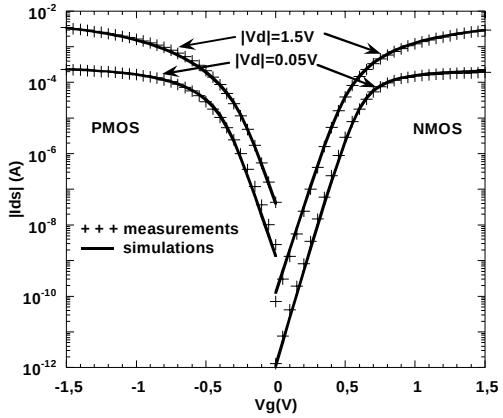


Figure 2. 50nm n-pMOS drain current versus gate voltage at Vd=0.05, 1.5V (W=10µm)

Roll-up and roll-off are well reproduced on a wide range of gate lengths for both nMOSFET and pMOSFET (figure 1).

3. Raised source/drain simulations

Two dimensional process and device RSD simulations were carried out with Silvaco's softwares: ATHENA-ATLAS™. The structure is represented on figure 3 : the 50nm gate is surrounded by a 7nm oxide liner and a 30nm nitride spacer in this case.

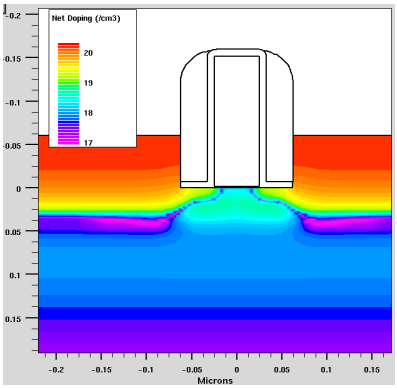


Figure 3. 50nm pMOS structure with a 60nm silicon epitaxial layer

Low Doped Drain and pocket implantation parameters were not altered. No epitaxial layer was deposited on the gate and no epi-facets were reproduced. A Design of Experiments (DOE with ECHIP™) has been performed with six input parameters : epitaxial layer thickness, nitride spacer width, HDD dose and energy. An implantation called Middle Doped Drain (MDD) described by its dose and energy, was added to avoid junction capacitance degradation induced by pockets. These parameters were altered between the limits indicated in table 2.

Table 2. DOE input parameters

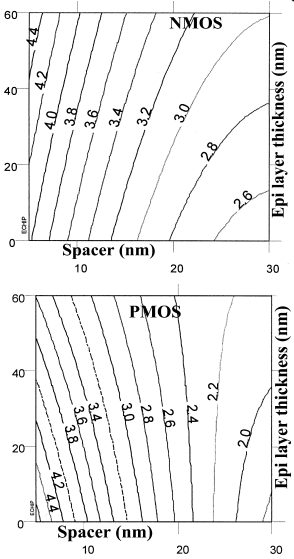
	NMOS	PMOS
Epi layer thickness (nm)	0 - 60	
Si_3N_4 sidewall spacer (nm)	5 - 30	
MDD dose (cm^{-2})	**Phosphorous** 10^{13} - 10^{14}	**Boron** 5.10^{12} - 10^{14}
MDD energy implant (keV)	5 - 30	1 - 10
HDD dose (cm^{-2})	**Arsenic** 5.10^{14} - 3.10^{15}	**Boron** 10^{14} - 3.10^{15}
HDD energy implant (keV)	8 - 20	1 - 5

Four electrical characteristics were particularly monitored : area junction capacitance (Cj), gate to drain capacitance at low drain voltage (Cg), parasitic resistance (Rp) and off-current (Ioff). In CV simulations, Cj was carefully separated from linear junction capacitance. In the NMOS case, electron concentration and electron mobility were extracted from the source contact to the source/channel junction in order to calculate Rp. These simulations were carried out at 1.2V and two models (NMOS and PMOS) depicting the four responses were therefore obtained.

Both n(p)MOSFET Cj increase with the epi thickness when HDD and MDD parameters are fixed. The latter's do not counter balance the pocket doping peak, leading to large junction capacitance degradation. Cj's behaviour was checked with HDD and MDD parameters : they normally decrease as doses and energies are raised.

Cg consists of three components: inner fringing, gate to drain overlap and outer fringing. The latter becomes a predominant part by raising the epi layer and reducing the spacer width [8]. Therefore, gate to drain capacitance was expected to increase. It was indeed observed for NMOS transistors (figure 4). But pMOSFETs had a different behaviour. It was noticed a decrease in Cg with enlarging epi layers as the spacer width is less than 25nm. It could be explained by a shallower HDD junction leading to a reduction of short channel effects. Inner fringing capacitance is also drastically decreased and is not enough counter balanced by outer fringing capacitance increase [9]. Moreover, pMOS Cg increases

with thicker silicon epi layers as spacers are larger than 25nm because of outer fringing capacitance raises.



MDD
Dose = $5.5.10^{13}$ cm^{-2}
Energy = 17.5 keV

HDD
Dose = $1.75.10^{15}$ cm^{-2}
Energy = 14 keV

MDD
Dose = $5.25.10^{13}$ cm^{-2}
Energy = 5.5 keV

HDD
Dose = $1.55.10^{15}$ cm^{-2}
Energy = 3 keV

Figure 4. Cg versus epi layer thickness and spacer width (n-pMOSFETs) (arbitrary units)

4. RSD impact on propagation delay and dynamic power consumption

Unloaded linear CMOS inverter chains with 0.12µm design rules were simulated with ELDO™. N-pMOS threshold voltages were tuned to get equivalent off-currents : 30nA/µm at Vds=1.2V and Vgs=0V. Transistors widths were adjusted to balance pull-up and pull-down delays. Propagation delay (τ_P) and dynamic power (P_{dyn}) of non-elevated *reference* circuits were respectively evaluated to 22.5ps and 36.4nW/MHz/gate from DC BSIM4.1 model card extracted on experimental 50nm devices.

From DOE results, we optimized MDD and HDD parameters for each spacer width - epi thickness couple *keeping* off-currents *constant* at 30nA/µm. Two optimization criteria were retained : minimizing Rp (option A) and minimizing (Rp, Cj, Cg) with the same weight (option B). All results were determined by response surface methodology Then circuit simulations were performed with BSIM4.1 model cards which were obviously modified to take into account Cj, Cg and Rp extracted values.

Option A : as τ_P is inversely proportional to saturation currents, we first tried to improve them by reducing Rp. In this option, Cj and Cg were extracted after having determined the lowest Rp. On figure 5, we observe that better τ_P (compared to reference) can be achieved as the epi thickness is between 10 and 20nm depending the spacer width (20-30nm). They could be lowered by 17% thanks to HDD and MDD implant optimizations. Rp is mainly reduced by the former whereas MDD additional implants avoid Cj degradation and are even able to reduce Cj. Hence, gains on τ_P are noticed as no epi layer is deposited, putting forward that low dose and high energies source and drain implants are mandatory to keep reasonable performances. With thinner spacers, no τ_P improvement is pointed out because Rp is higher than in the initial case. Low HDD dose and energy were necessary to keep Ioff constant leading to higher access resistances. Better performances would be achievable working on pocket and/or LDD implants, which is beyond the scope of this study.

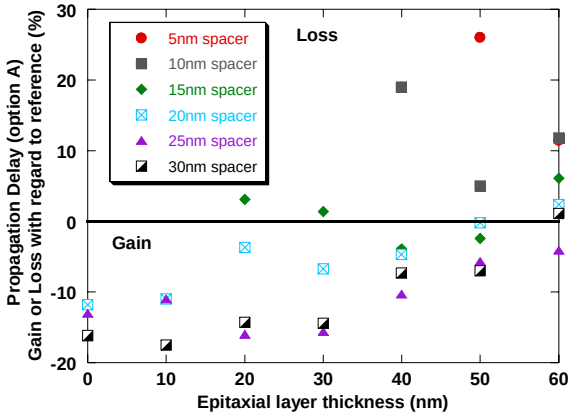


Figure 5. Propagation delay optimization
Option A

Concerning P_{dyn} enhancements (figure 6), they are smaller than τ_P's because Rp has a negligible impact on P_{dyn}. Only a maximum of 9% gain is obtained (compared to 17%). Miller capacitance increases are also responsible for this weak gain : higher MDD and HDD doses induced by low Rp degrade Cg. We also notice that dynamic powers are often degraded when 30-40nm of silicon are deposited on the side of 15-20nm spacers whereas propagation delays are improved. It is attributed to the increase of outer fringing capacitances.

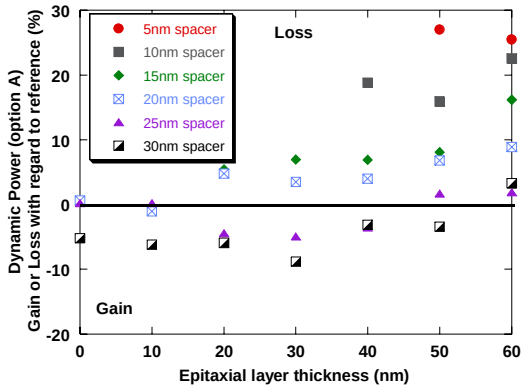


Figure 6. Dynamic power optimization
Option A

Option B : we decided to address low-power circuits with RSD by trying to get an optimal response. On the following figures (7-8), propagation delays compared to option A are a little bit lowered for 25-30nm spacers. Cg

improvements are sometimes balanced by Rp raises. Nevertheless, gains on P_{dyn} are more important because Cg degradation is reduced by HDD and MDD optimizations.

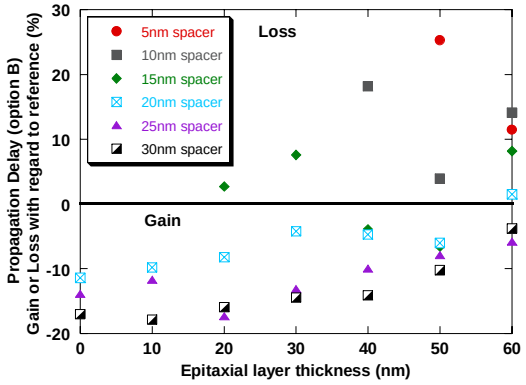


Figure 7. Propagation delay optimization *Option B*

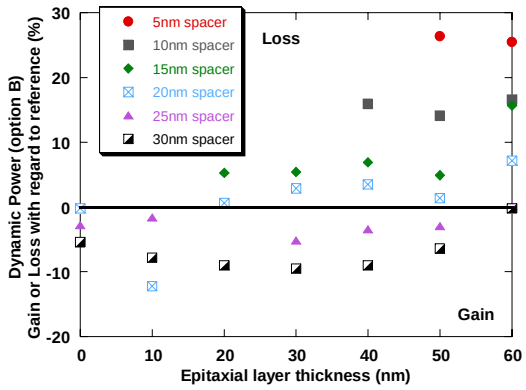


Figure 8. Dynamic power optimization *Option B*

A comparison between options A and B is presented on table 3 for each spacer width – epi thickness couple. The first symbol indicates a possible improvement with τ_{P_B} compared to τ_{P_A}. The second concerns P_{dyn} in the same way. We notice that performances are in most case enhanced as MDD and HDD parameters were optimized to limit Cg degradation.

Table 3 : comparison between options A and B

Epi th (nm) / Spacer	0	10	20	30	40	50	60
5 nm						+ +	0 0
10 nm					+ +	+ +	+ +
15 nm			+ +	- +	0 0	+ +	- +
20 nm	- +	- +	+ +	+ +	0 +	+ +	+ +
25 nm	+ +	+ +	+ +	- +	0 0	+ +	+ +
30 nm	+ +	+ +	+ +	0 +	+ +	+ +	+ +

5. Conclusion

Starting from BSIM4.1 simulations performed on 50nm CMOS inverter chains, raised source/drain clearly improve propagation delays by 17% with a 10-20nm epi silicon layer and 20-30nm nitride spacers. But, these better τ_P are not always accompanied by improvements in dynamic power consumptions. Hence, a trade off between parasitic resistance and gate to drain capacitance has to be found : MDD and HDD technological parameters have to be optimized following circuit's purpose.

6. Acknowledgments

This work has been performed in the frame of the CEA-LETI/CPMA collaboration with PLATO teams and tools. The authors wish to thank the Silicon Technologies Department for lot processing and testing. P. Rivallin, P. Scheiblin and T. Poiroux are warmly thanked for their support to this study.

7. References

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