Channel Engineering Study for 50 nm P-Channel MOSFET

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Abstract

This paper discusses the optimisation of low cost 50 nm physical gate pMOSFET devices focusing on channel engineering. An extensive comparison of 50 nm pMOSFETs processed with either conventional or with retrograde channel profiles is presented. Except for Arsenic channel implants and annealing, the other pMOSFET design parameters such as gate oxide (2.2nm), pre-doped polysilicon gate with Boron, gate patterning with hybrid lithography, LDD, pocket architecture with nitride spacers and HDD implants with BF_2, are similar. Gate lengths down to 45 nm have been processed. Furthermore, the impacts of annealing conditions (RTA or spike) are investigated. It is demonstrated that retrograde channel provides lower gate length sensitivity and wider process window with a drive current of 390 µA/µm at a specified Ioff of 70nA/µm despite thick gate oxide.

1. Introduction

As MOSFET scaling continues, not only ultra-shallow junction but also channel profile optimisation are essential for device performance improvement and short channel effect (SCE) control. On the contrary of high permittivity gate dielectric, the pure gate oxide cannot be scaled with gate length for stand-by gate current consideration [1]. Therefore, retrograde profiles with epitaxial undoped Si growth [2] or with heavy ion [3] have been proposed to minimize SCE. On the other hand, device drive current degradation is usually observed with retrograde channel profiles [4]. Recently conventional and retrograde n channel MOSFET have been compared in the literature for 0.1µm generation [5] and 50 nm [6], but these theoretical studies were only based on simulation. In this paper, we propose an experimental and extensive evaluation of three channel profiles implanted in a 50 nm pMOSFET core process with a relatively thick gate oxide (2.2 nm). The comparison is based upon the following criteria :

- SCE control and sub-threshold swing
- Drive currents
- Gate length and process sensitivity

2. Device fabrication

These transistors were defined for a 1.5 V power supply voltage, a nominal gate length of 50 nm and a gate oxide of 2.2 nm. After isolation formation and retrograde well definition using a high implantation energy of Phosphorus, the channel doping profile was defined with one Arsenic implant. Three different channel energies and dosages were applied. Two conditions of retrograde channel profiles were investigated : one with lower dose in order to obtain the same Vt than the conventional architecture and the other one with higher dose. The simulated channel profiles of respectively conventional architecture (low dose and energy) and retrograde approach (low (LD) and high dose (HD)) are shown in figure 1. The 2.2 nm thick gate oxide was thermally grown at 700°C under O2 + HCl. The 150 nm fine-grain columnar poly-Si was then deposited and pre-doped with high dose of Boron performed before gate patterning. This additional dose was necessary in order to reduce P+ gate poly depletion and to optimise separately gate and source/drain [7].

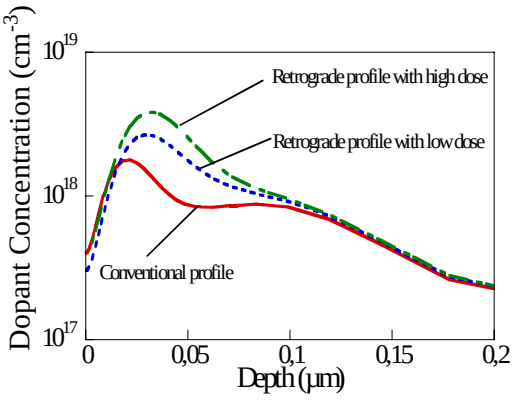

Figure 1. Comparison of channel doping profile

The gate was patterned with hybrid lithography using SUMITOMO NEB 22A resist. Structures with geometries greater than 0.35 µm were exposed with DUV while smaller patterns were exposed with electron beam. An example of gate length electrical measurements is shown in figure 2 : the 50 nm gate

length design is well controlled : the average value is 51nm with a low standard deviation of 4 nm. This good gate length definition is essential to evaluate performances of each channel architecture.

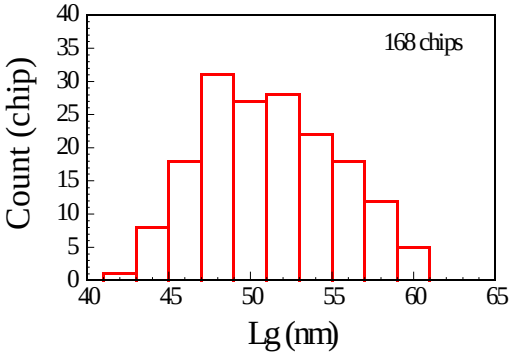

Figure 2. Electrical gate length measurements of 50nm nominal gate

Based on a LDD structure defined with low energy BF_2 ion implantation, a pocket architecture with an Arsenic ion implantation and 45° tilt angle was achieved. The extension depth is 20 nm according to SIMS profile measurement. A 25 nm nitride spacer was then formed. Source and Drain are defined with a high dose of BF_2. Two annealing activation conditions were evaluated : the first with rapid thermal annealing (RTA) at 950°C 15s and the second with 1050°C spike annealing (SA). This spike process has a ramp-up and a ramp-down rate of 80°C/s. Many studies have demonstrated the reduction of the TED phenomenon of Boron with the use of a spike anneal. However, the higher anneal temperature with spike, results in a 7 nm deeper junction depth and a more abrupt profile (Figure 3). Fabrication was completed with the conventional metallization process including tungsten plug and chemical-mechanical polishing.

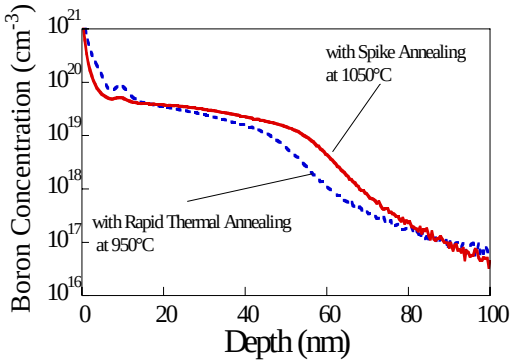

Figure 3. Comparison of SIMS profiles of source/drain with either RTA or SA.

3. Experimental results

To carry out this channel engineering comparison, pMOSFETs with physical gate lengths down to 45 nm were fabricated and characterized. The effective channel length (Leff) was evaluated using Shift and Ratio method and figure 4 shows an example of the Vt dependence with Leff in the case of the conventional channel profile with RTA at 950°C.

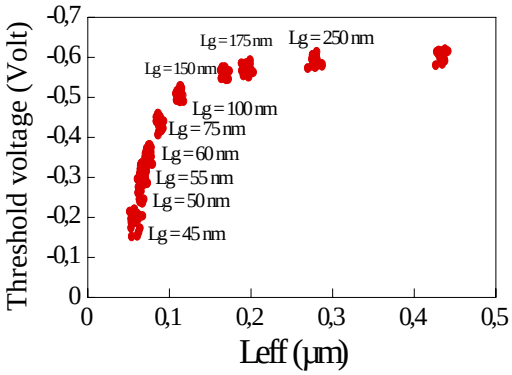

Figure 4. Vt (Leff) characteristics measured on the conventional channel profiles.

Figure 5 shows the threshold voltage dependence on physical gate length for three channel implant splits and two anneal conditions. Deeper source/drain junction and higher lateral extension with the higher temperature of the spike anneal lead to an increase of the short channel effect whatever channel profiles are. Furthermore, this figure indicates a 30 mV threshold voltage shift with SA measured on 10 µm gate length devices due to a better gate activation : the equivalent gate oxide is reduced from 3.61 nm to 3.54 nm. We observe a better control of the roll off with retrograde profile whatever annealing conditions are. This behaviour is emphasized with the highest dose of the channel implant. An example of better SCE control with gate oxide scaling (Tox=1.4nm) is also given on this figure. This advantage is paid by a four decade increase of gate current density.

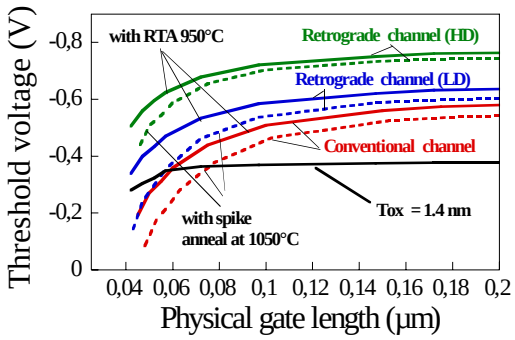

Figure 5. Comparison of the threshold voltage dependence on the gate length for conventional and retrograde profiles with either RTA (solid line) or SA (dashed line).

The DIBL and above all the subthreshold slope dependence versus gate length which are plotted on figures 6 and 7, confirm these behaviours. There is no

significant increase of the swing at Vd = -1.5 volt for pMOSFETs defined with retrograde channel and high dose for physical gate length down to 42 nm with either RTA or spike anneal .

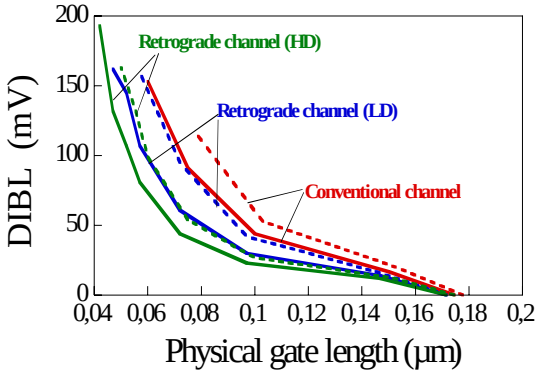

Figure 6. Comparison of the DIBL dependence on the gate length for conventional and retrograde profiles with either RTA (solid line) or SA (dashed line).

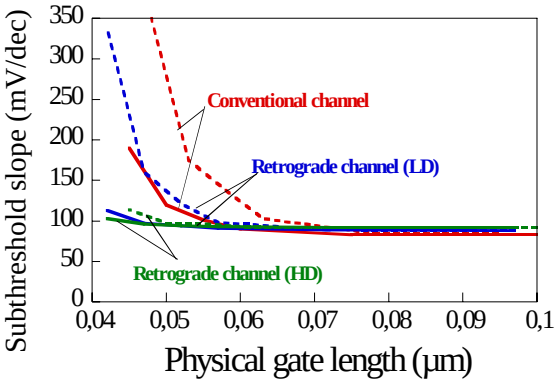

Figure 7. Subthreshold slope dependence on the gate length measured at Vd = -1.5 V for conventional and retrograde profiles with either RTA (solid line) or SA (dashed line).

From the comparison between 950°C RTA and 1050°C spike anneal shown in figure 8, the drive current (Idsat) at a given off current (Ioff) increases with SA. This result, which is related to conventional channel on this figure, is caused by both a 300 Ohm µm decrease of the parasitic resistance and a 6 nm shorter effective channel length. This higher current with SA can also be attributed to better gate activation. On the other hand, the physical gate length at a specified Ioff of 10 nA/µm increases from 62 nm to 75 nm with SA due to short channel effect degradation. This behaviour is also observed on retrograde channel architecture but with less emphasized than with conventional channel due to a better SCE control. The gate length shift between RTA and SA for a 10 nA/µm Ioff, is only 6 nm with retrograde profile and high dose of the channel implant.

Figure 9 shows Idsat versus Ioff performances of either conventional or retrograde channel with low dose. The same basic performances in terms of trade-off between Ioff and drive current are reached. However, the gate length of the retrograde channel can be 10 nm shorter due to better roll-off control.

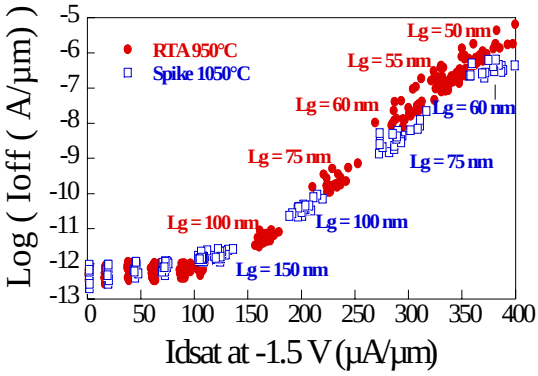

Figure 8. Ioff-Idsat characteristics as a function of annealing process for conventional channel architecture.

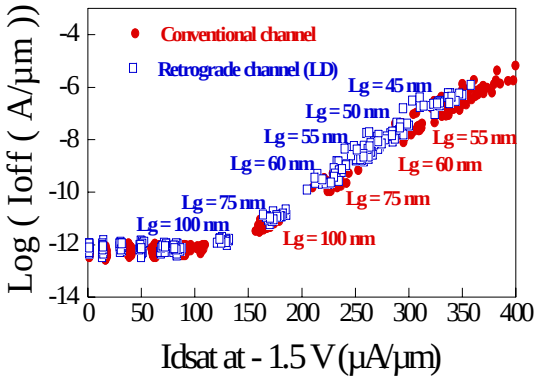

Figure 9. Ioff-Idsat characteristics as a function of channel architecture for either conventional or retrograde channel (LD) .

Figure 10 presents the operating domain Idsat-Gate length of both RTA and SA for each channel architecture with an Ioff of 70 nA/µm. This Ioff is the new leakage current specification of the high performance 45 nm physical gate length device of the ITRS roadmap [8]. The drive current Idsat of pMOSFETs is lower with retrograde channel than in conventional architecture whatever annealing conditions are. This can be attributed mainly to the higher threshold voltage and the larger body effect : the body factor γ measured on 0.15 µm gate length, increases significantly from 0.495 $V^{1/2}$ (conventional channel) to 0.720 $V^{1/2}$ (retrograde channel with LD) or 0.878 $V^{1/2}$ (retrograde channel with HD). Indeed, the '' pinch-off '' of the retrograde channel, with this high body factor, occurs at a smaller drain bias. The maxima of the transconductance are equal for both

conventional and retrograde channels : these channel architectures were not optimised to increase mobility which is dominated by surface scattering. These retrograde profiles were studied to improve short channel effect which is the main issue if the scaling of the gate dielectric is limited to 2.2 nm. The improved SCE with retrograde profile which results in gate length scaling, is not sufficient to compensate higher Vt and body effect. Consequently, retrograde profiles yield to lower Idsat. On the other hand, for a low power application with a more severe Ioff constraint, the retrograde profile with reduced gate length and thermal budget sensitivities is a good candidate. Furthermore, this channel architecture is essential if the gate dielectric cannot be scaled with gate length.

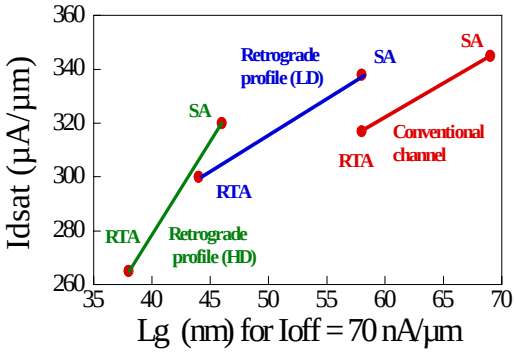

Figure 10. Comparison of the operating domain Idsat- Lg for a 70 nA/µm Ioff leakage current.

In this study, the saturation currents are degraded by a high parasitic resistance (Rsd) because the devices were not silicided. Rsd will be significantly reduced with silicidation from of 1300 Ohm-µm to 600 Ohm-µm. Simulations were performed [9] and a summary of expected saturation drain currents by using a silicide process is shown in table1. A high current of 390 µA/µm can be reached on a 46 nm p-channel MOSFET gate length with a retrograde profile optimised with a high dose.

Table 1. Comparison of expected Idsat for a 70nA/µm Ioff leakage current

	RTA		Spike Anneal	
Profile	Lg (nm)	Idsat (µA/µm)	Lg (nm)	Idsat (µA/µm)
Conventional	58	387	69	421
Retro. (LD)	44	366	58	412
Retro. (HD)	38	323	46	390

4. Conclusion

The gate dielectric cannot be scaled forever due to high stand-by gate current and its impact on the functionality of CMOS circuits. Consequently, the short channel effect control with relatively thick gate oxide (2.2 nm) is one of the main issue of the gate length scaling. Therefore, we have compared a conventional and two retrograde channel profiles on a manufacturable 50 nm gate length p channel MOSFET. These transistors were fabricated with standard process steps except hybrid lithography for gate definition. The main advantage of retrograde channel profile is to reduce gate length and thermal budget sensitivity due to a better control of the short channel roll-off. This wider process window is paid by a lower drive current performance attributed to a larger body effect and higher threshold voltage. In conclusion, the retrograde channel architecture, which allows to scaled down pMOSFETs into the 40 nm regime with a low cost process and a 390µA/µm drive current, is essential.

5. Acknowledgements

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6. References

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