Comparison of the Gate Tunneling Current in Ultrathin−Oxide Inversion and Accumulation MOSFETs

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Abstract

The goal of this work is to demonstrate that buried −channel accumulation (BCA) and surface−channel accumulation (SCA) MOSFETs can be designed to provide lower gate currents, thus better I_{off} control and minimal I_{dsat} degradation than conventional surface−channel inversion (SCI) devices. The specific case of the device design which lies on the border between BCA and SCA operation (Fermi−FET®) is compared with an SCI device, and is shown to provide signifi−cantly reduced gate current for ultrathin oxides.

1. Introduction

According to the current ITRS roadmap, the pro−jected trends in CMOS technologies call for comple−mentary SCI MOSFETs with ultrathin effective gate dielectric thicknesses (X_{OX}) scaling below 2 nm. As is well known, oxides at such thicknesses no longer represent a classical barrier to gate conduction. Quan−tum mechanical tunneling of carriers from both the conduction and valence bands on each side of the oxide becomes an important physical mechanism which sig−nificantly affects transistor properties, specifically the *I−V* characteristics. With a large gate current present, both the on and off−state characteristics of the MOSFET are degraded. Developing alternative gate dielectrics is one solution to the problem, however, this work suggests that alternative channel structures should also be considered to reduce gate tunneling current while providing enhanced performance.

2. Device structures

The device structures simulated in this work are shown in Fig. 1. Uniform doping is used in each case, with a metal−like ideal gate electrode and simple (non−LDD) shallow source/drains. The structures are geo−metrically identical except for the counter−doped channel in the BCA/SCA structure as found in tradi−tional buried−channel devices. However, the doping in this structure is set to provide a nearly zero oxide field at V_T. This special case device structure is designated

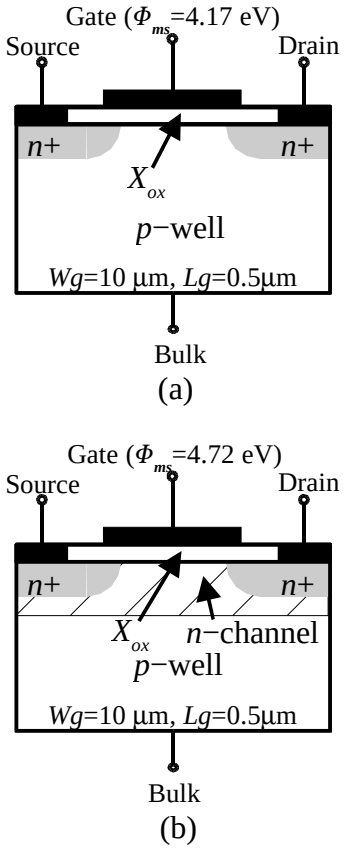

Figure 1. Planar simulation structures for (a) SCI MOSFET and (b) BCA/SCA MOSFET (Fermi−FET).

the Fermi−FET [2]. Using a channel profile such as this provides some interesting properties as well as performance enhancements [3][6]. One characteristic of this design is that the V_T is very nearly independent of oxide thickness X_{OX}. This was experimentally observed during a buried−channel device study by Parillo, et. al. [1], although the authors did not explore the reason for their observation. Another important characteristic of the Fermi−FET is the reduction of internal fields within the device throughout all regions of operation.

Note the difference in gate workfunctions specified

in Fig. 1(a) vs. Fig. 1(b). The Fermi−FET devices were simulated assuming a mid−bandgap refractory metal such as tungsten for the gate. Using a material such as this allows the Fermi−FET channel doping to be lowered, thus reducing internal fields and capacitances while enhancing low−field mobility. The resulting workfunction difference allows the V_T to be set to about 0.45 V at these doping levels. Table 1 provides a sum−mary of the properties of the two structures for V_{DS} = 0.05 V. Note the relatively constant V_T for the Fermi−FET over the range of oxide thicknesses used.

Table 1. Fermi−FET and SCI device properties.

Fermi−FET			
X_{OX} (nm)	Doping (cm^{-3})	V_T (V)	Max. g_m (μS/μm)
1.1	$1.0x10^{17}$	0.458	96.0
1.3	$1.0x10^{17}$	0.463	88.8
1.5	$1.0x10^{17}$	0.462	79.6
1.7	$1.0x10^{17}$	0.460	71.8
SCI			
X_{OX} (nm)	Doping (cm^{-3})	V_T (V)	Max. g_m (μS/μm)
1.1	$6.4x10^{18}$	0.406	14.8
1.3	$4.5x10^{18}$	0.413	26.7
1.5	$3.4x10^{18}$	0.414	28.5
1.7	$2.7x10^{18}$	0.413	28.1

The SCI and Fermi−FET structures were simulated using Tunnel−PISCES [4] which provides a self−con−sistent solution of the drift−diffusion transport in the substrate and gate regions and tunneling in the gate dielectric via the independent electron tunneling model. Relatively long−channel devices were simulated (L_g =0.5μm). Oxide thicknesses of 1.1 to 1.7 nm were studied at V_{DD} =1.0 V, based upon the 100 nm high−performance node in the ITRS roadmap. Both devices were *n*−channel MOSFETs. In order to provide a basis for comparison, the SCI MOSFET's channel doping was adjusted for each X_{OX} to yield devices with sub−V_T characteristics similar to those of the Fermi−FET devices. The V_T variation over all of the devices is less than 2%. Table 1 shows the doping used for each device at each X_{OX}, along with the V_T and maximum g_m. Note that the channel doping for the Fermi−FET devices is the same for each oxide thickness, but the channel doping level for the SCI MOSFETs must increase as X_{OX} is thinned, thus the sub−V_T and g_m characteristics are degraded. The simulation tunneling parameters used are based upon calibration against the data of Momose, et. al. [5] as in [4]. Only conduction band tunneling is con−sidered in this work.

3. Simulation results

Figs. 2 to 5 show the dependence of the gate and drain currents on V_{GS} and X_{ox} for the Fermi−FET and the SCI MOSFETs at V_{DS}=0.05 and 1.0 V. Comparing Figs. 2 and 3 (at V_{DS}=0.05 V), it can be seen that at low gate

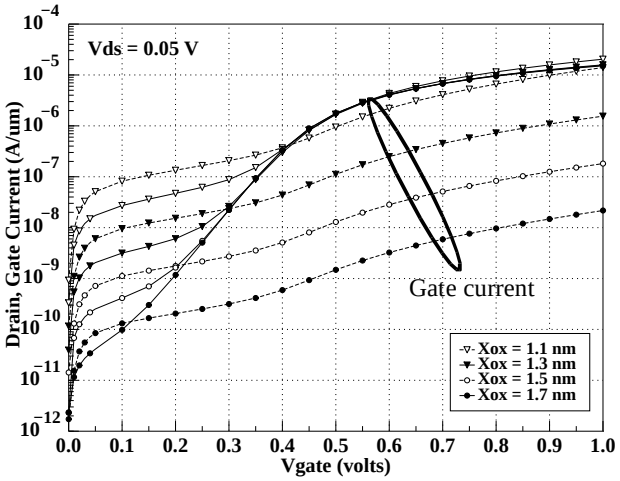

Figure 2: Drain and gate current characteristics for *n*−channel SCI device at V_{DS} = 0.05 V.

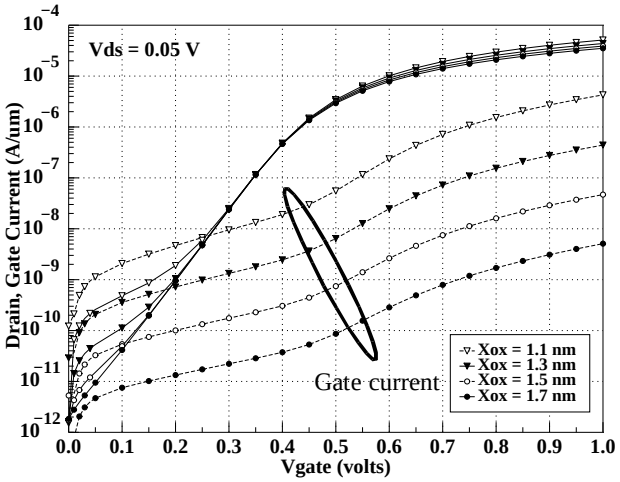

Figure 3: Drain and gate current characteristics for *n*−channel Fermi−FET device at V_{DS} = 0.05 V.

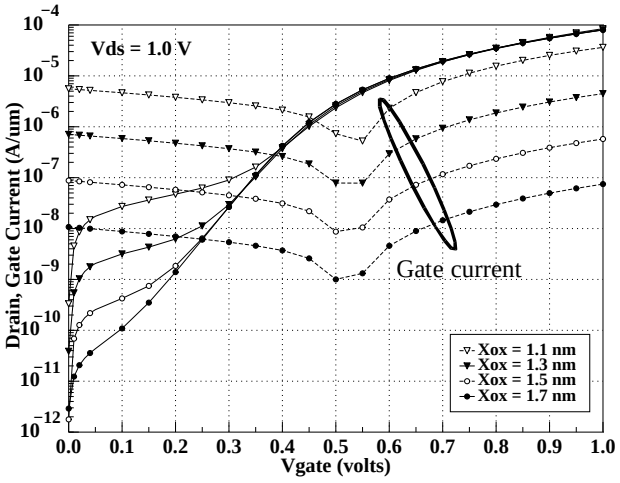

Figure 4: Drain and gate current characteristics for *n*−channel SCI device at V_{DS} = 1.0 V.

bias the Fermi−FET gate current is lower than that of the SCI device by about 25−40x. For V_{GS} > 0.5 V, the gate current ratio is reduced to about 3−4x at V_{GS} = 1.0 V. Comparing Figs. 4 and 5, at a high drain bias of V_{DS} = 1.0 V, the gate current reduction ratio is about 3x, independent of gate bias. An explanation for the re−

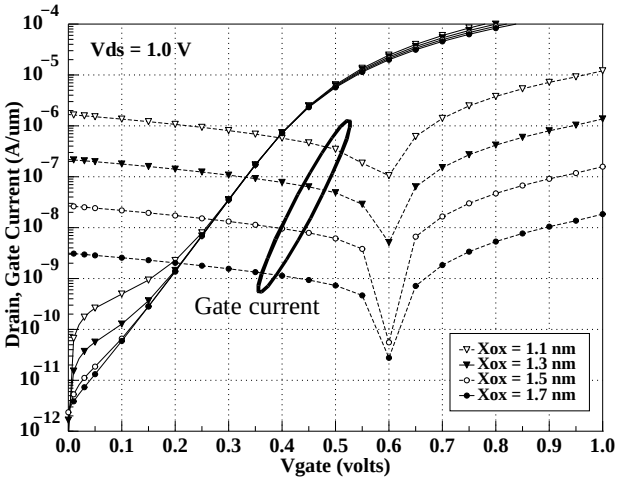

Figure 5: Drain and gate current characteristics for *n*−channel Fermi−FET device at V_{DS} = 1.0 V.

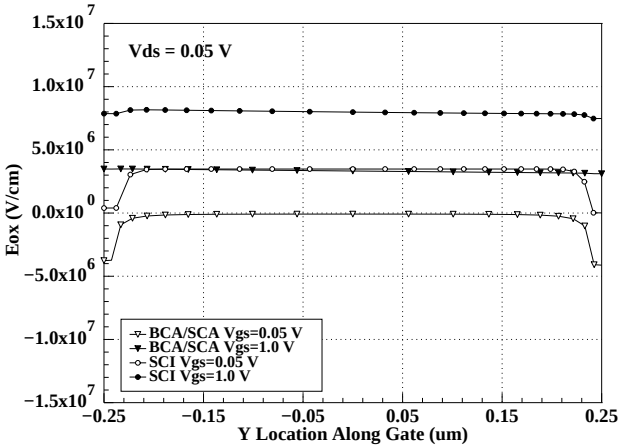

Figure 6: Oxide field along the gate for Fermi−FET and SCI devices at V_{GS} = 0.05 and 1.0 V. X_{OX} =1.1 nm. V_{DS} = 0.05 V.

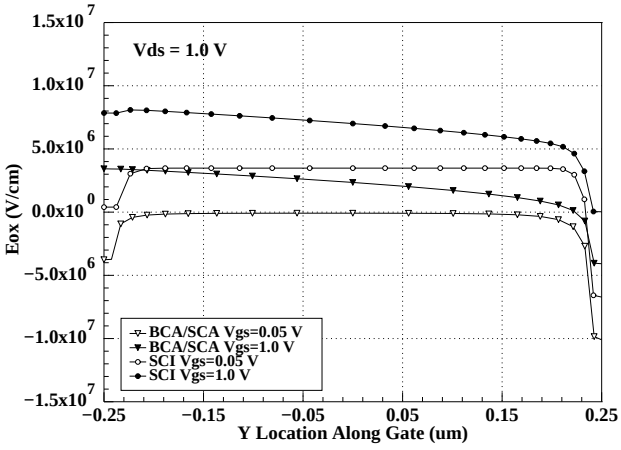

Figure 7: Oxide field along the gate for Fermi−FET and SCI devices at V_{GS} = 0.05 and 1.0 V. X_{OX}=1.1 nm. V_{DS} = 1.0 V.

duced gate current for the Fermi−FET device is simply that the field across the oxide is reduced in both the on and off states due to the channel design and gate workfunction differences, as seen in Figs. 6 and 7.

Figs. 8 and 9 show the Fermi−FET to SCI gate

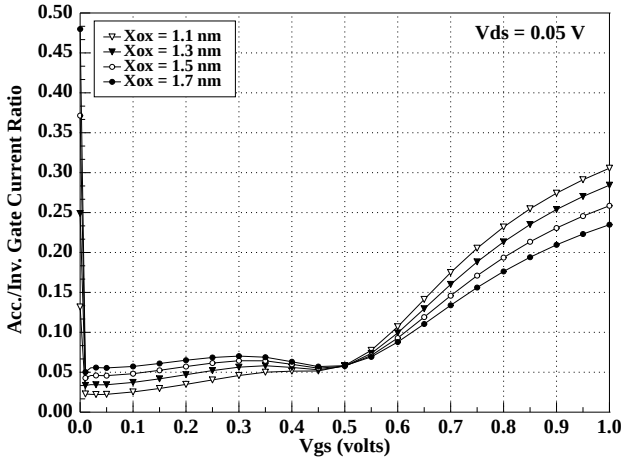

Figure 8: Ratio of Fermi−FET to SCI gate currents as a function of X_{OX}. V_{DS} = 0.05 V. Fermi−FET gate current is significantly lower than SCI gate current for low V_{GS}

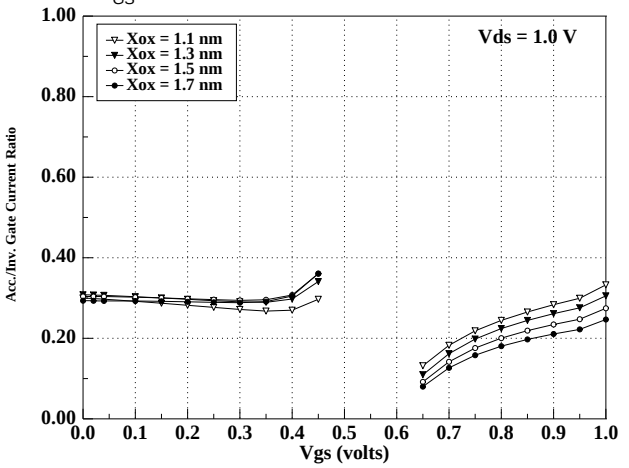

Figure 9: Ratio of Fermi−FET to SCI gate currents as a function of V_{GS} with X_{OX}. V_{DS} = 1.0 V.

current ratios at V_{DS} = 0.05 and 1.0 V, respectively. In Fig. 8, the ratio is significantly low for V_{GS} < 0.5, rising to 0.25 to 0.3 at V_{GS} = 1.0 V. This rise is due to the larger increase in I_G as a function of V_{GS} for the Fermi−FET device. In Fig. 9, a gap is shown in the simulation results near V_{GS} = 0.5 V due to a reversal in direction in the gate current. The gate current for both devices is less than zero for approximately V_{GS} = 0.5−0.6 V and the zero crossing is independent of X_{OX}, although the zero crossing occurs at a different V_{GS} for the Fermi−FET versus the SCI device. The meaning of the gate current ratio in the bias range from V_{GS} = 0.45 to 0.65 V is not clear because of the change in sign. It can be seen that the ratio at V_{DS} = 1.0 V has a much weaker dependence on V_{GS} than at V_{DS} = 0.05 V.

Figs. 10 and 11 show the ratio of gate to drain current for each device at X_{OX} = 1.1 and 1.7 nm. The purpose of these plots is to show that the reduction in gate current is not at the expense of the drain current. In fact, because of the oxide−independent V_T for the Fermi−FET device, the thinner gate oxide leads directly to a higher g_m and higher drain currents. For V_{DS} = 0.05 V, this ratio is on the order of 10x, while it is smaller at

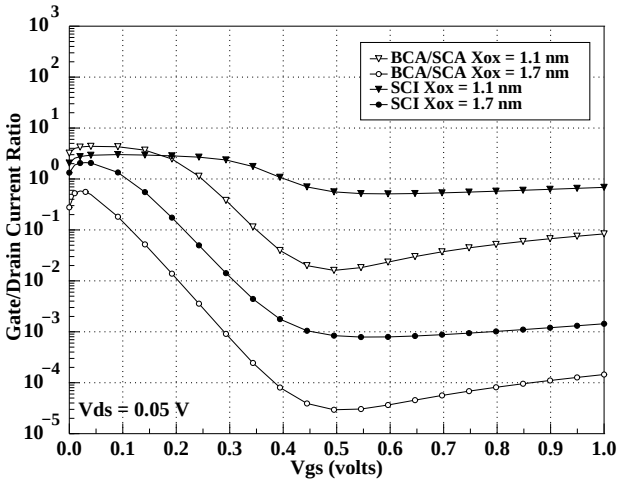

Figure 10: Comparison of gate/drain current ratios (I_G/I_D) for the Fermi−FET and SCI devices as a function of V_{GS}. V_{DS} = 0.05 V.

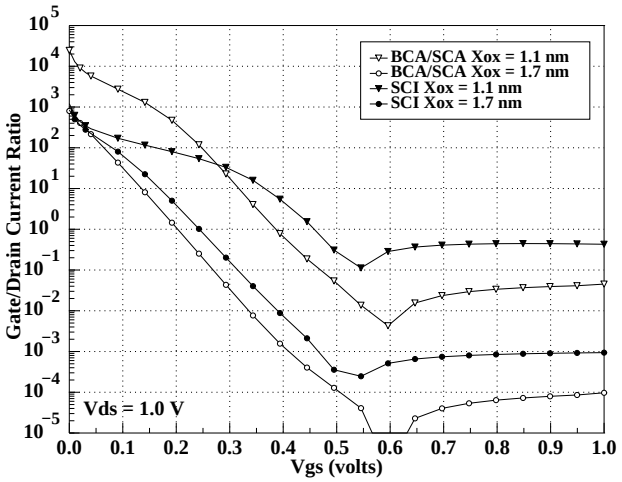

Figure 11: Comparison of gate/drain current ratios (I_G/I_D) for the Fermi−FET and SCI devices as a function of V_{GS}. V_{DS} = 1.0 V.

V_{DS} = 1.0 V. The Fermi−FET device shows higher gate/drain current ratio for X_{OX} = 1.1 nm at low V_{GS}, which is an indication of the lower sub−V_T slope and I_{off} current.

4. Conclusions

Tunnel−PISCES [4] simulations indicate that ultra−thin−oxide BCA and SCA accumulation MOSFETs, and specifically Fermi−FETs, have gate and drain char−acteristics superior to those of SCI MOSFETs. With proper gate and channel engineering, this suggests that the Fermi−FET architecture should allow the oxide to be scaled more aggressively than for conventional SCI devices due to the reduced internal field distributions, and the resulting reduced gate current. The reduced in−ternal fields of the Fermi−FET also provide advantages with respect to device reliability as well as perform−ance, particularly for micropower applications [3]. There are other interesting properties of this structure which have been reported elsewhere [2][3][6].

5. References

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