A Novel CMOS Compatible Top-Floating-Gate Flash EEPROM Cell.

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Abstract

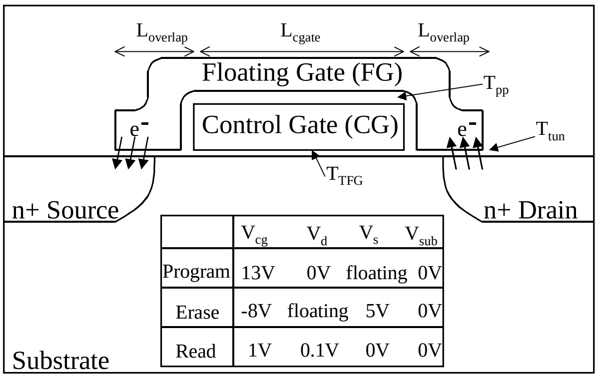
A novel nonvolatile memory (NVM) Top-floating-gate (TFG) flash device is demonstrated in a CMOS technology which can be implemented as a stand alone device, or with additional benefit as an embedded device. This device differs in both structure and operation to typical split-gate or stacked-gate approaches. The TFG device uniquely offers low development cost, low power compliance and high reliability. It can be fabricated using routine CMOS processing making it clearly competitive to options typically used in the industry. The structure and operation of this novel device structure is described. This is followed by a description of the processing required and electrical results.

1. Introduction

Embedded flash nonvolatile memory (NVM) [1] provides data storage on chip with CMOS logic devices. In attempting to embed an NVM option three features must be analysed. These are development cost, CMOS compatibility and with the advent of mobile applications, suitable low power operation. Two of the standard approaches to implementing embedded NVM are the spit-gate [2,3] and stacked-gate [4,5] devices. The split-gate device suffers from large power consumption, whereas the stacked-gate device requires a complicated stack etch and suffers from over-erase issues. We present in this paper a novel structure which is low power compliant, has low development costs, and doesn’t suffer from over-erase. With the evolution of the portable applications market, the possibility of a nonvolatile data or code storage facility on chip with these advantages makes the Top-Floating-Gate (TFG) device [6] a rival to typically used embedded NVM options. In the following sections, we describe the structure and operation of the device and conclude with a macro-model which accurately describes the read operation of the device.

2. Device Structure and Operation

The TFG device shown in figure 1, is a symmetrical device in which PolyI constitutes the control gate (CG) with PolyII comprising the floating gate (FG) in a direct inversion of typical stacked or split-gate options. The TFG cell is designed with the FG surrounding the CG in the lateral direction and equal to the active area in the width direction thereby greatly enhancing the gate coupling ratio (α_{cg}) allowing a small area cell and avoiding the use of expensive z-direction extensions. The program and erase functions of this device involve charge transfer to and from the FG by Fowler-Nordheim (FN) tunnelling across T_{tun}. Typical bias conditions are shown in the table in figure 1 while figure 2 shows a SEM micrograph of the fabricated TFG cell.



	V_{cg}	V_d	V_s	V_{sub}
Program	13V	0V	floating	0V
Erase	-8V	floating	5V	0V
Read	1V	0.1V	0V	0V

Figure 1. Schematic cross-section representation of the TFG EEPROM cell including biases for each memory operation

Programming of the TFG is achieved with a high positive pulse applied to the CG, the source region floating and the drain and bulk silicon held at ground. This couples a positive bias to the floating gate and initiates FN tunnelling from the drain region beneath the FG, setting the device to its logic"0" state. Induced negative charge (Q_{fg}) on the FG causes depletion of carriers in both source and drain regions beneath the FG region while simultaneously causing accumulation of carriers in the channel area which is controlled by the FG.

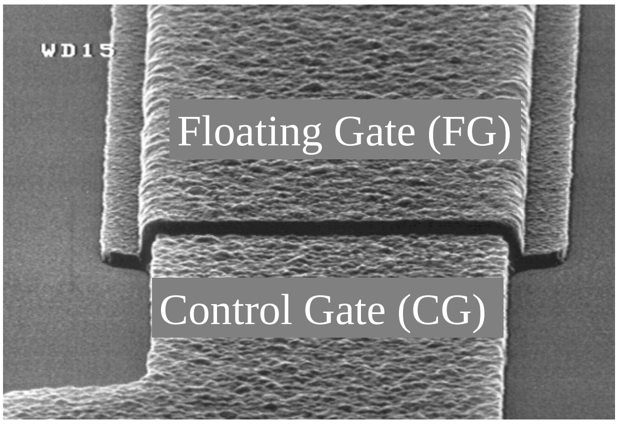


Figure 2. SEM micrograph of the fabricated TFG cell

Bitwise low power erasing is completed by applying a negative pulse to CG, positive bias to the source region while leaving the drain floating and the bulk grounded. This reverses the direction of tunnelling from FG to bulk silicon now through the source region and returns the TFG cell to its erased ("1"logic) state. Using alternate regions for tunnelling has the advantage of improved reliability.

The distinction of 2 memory states is achieved due to a threshold voltage (V_t)-shift and a transconductance (g_m) change, allowing a large $I_{read\ (HI)}$ /$I_{read\ (LO)}$ ratio. As there is a native transistor controlled solely by the CG overerase is not an issue for this cell

Critical dimensions of this cell, L_{cgate} and $L_{overlap}$ are defined by lithography steps, thus making manufacturing straightforward and the cell highly CMOS compatible.

3. Fabrication Results

The TFG device was fabricated in a double-poly double-metal 1.5µm CMOS technology within the NMRC Silicon Fabrication laboratory. Fabricating the TFG in a double-poly CMOS process is possible using two additional standard processing steps, namely an oxide strip after PolyI patterning and a high quality thermal oxidation for a target Tunnel (T_{tun})/Interpoly (T_{pp}) oxide of approximately 80Å and 140Å respectively. Re-oxidation before the Source/Drain implants is modified to allow for the new tunnel oxidation cycle while maintaining the baseline thermal budget. Subsequent processing follows the standard CMOS flow including a standard self-aligned Source/Drain implant.

Defining the FG is performed using standard lithography techniques thus avoiding embedding difficulties associated with the complicated stack-etch processing used for stacked-gate structures. Since PolyI constitutes the CG salicidation is not possible for the TFG and an extra masking step protecting TFG areas will be required in the case of a baseline technology using salicidation. However, given that the FG only fully covers the CG in one direction polycide formation on an extended CG is possible to reduce WL resistance problems but which would incur masking and area costs. As with all cells using Fowler-Nordheim tunnelling, both PMOS and NMOS high voltage transistors are required to transfer the programming voltages to the cell.

4. Electrical Results & Discussion

Electrical chacterisation was carried out on a TFG device with a W/L of 2.5µm/1.5µm and a $L_{overlap}$ of 0.3µm. Figure 2 shows the transient program and erase operations as a function of the pulse width applied. Programming is achievable within 800µs with V_{CG} of 13.0V. Erasure is possible within 500µs with V_{CG} of -8.0V and V_{DS} of 5.0V.

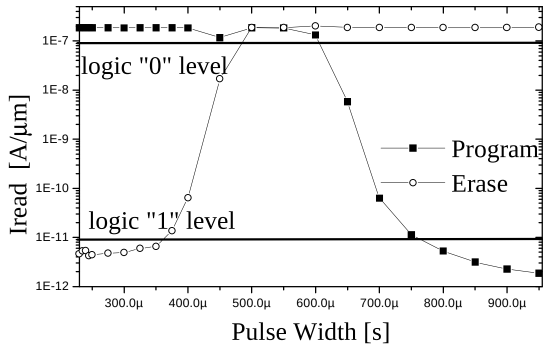


Figure 2. Measured transient program and erase characteristic. Read out current, I_{read} is at V_{CG}=1.0V and V_{DS}=0.1V. A pulse rise/fall time of 500•s is used.

Figure 3 shows the measured read characteristic on a linear and log scale for both memory states with the g_m and V_t effect clearly observed. I_{DS} at a specified V_{CG} and V_{DS} is used as the read variable because both V_t and g_m are modified when charge is on the FG. Through this novel combination of g_m- and V_t- based operation an $I_{read\ (HI)}$ /$I_{read\ (LO)}$ ratio greater than 5 orders of magnitude is possible.

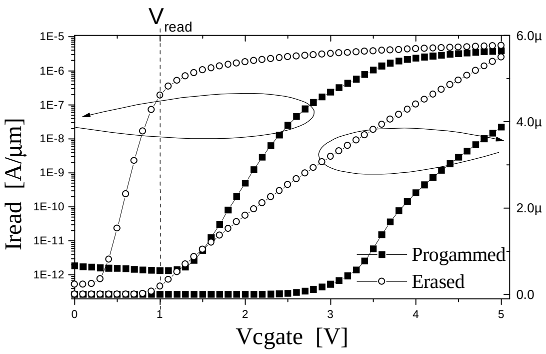


Figure 3. Measured programmed and erased states for the TFG cell. The TFG cell is programmed for 3ms and erasure is carried out with for 3ms. A pulse rise/fall time of 500•s is used

The endurance capability of the TFG device has been demonstrated through the cycling test shown in figure 4 with a program operation using V_{CG} of 13.0 V for 3ms and a V_{CG} of –8.0 V and VS 5.0 V for 3ms for the erase operation. This endurance characteristic demonstrates only 3.5% degradation of the operating window in excess of 10^5 W/E cycles.

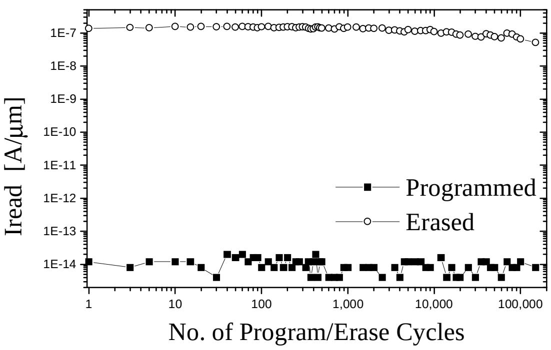


Figure 4. Measured cycling characteristic. Programming is performed for 3ms and erasure is for 3ms. A pulse rise/fall time of 500•s is used.

To confirm the inherent large α_{cg}, a new coupling ratio extraction methodology was developed [7]. To model the read operation of the TFG, the structure may be divided into three regions, the source-side FG (S) region, the channel (C) region (controlled directly by the CG electrode) and the drain-side FG (D) region. With such an arrangement the cell is made up of three MOSFETs, M_S, M_C and M_D with an interpoly cpacitance C_{pp} between CG and FG as depicted in figure 5.

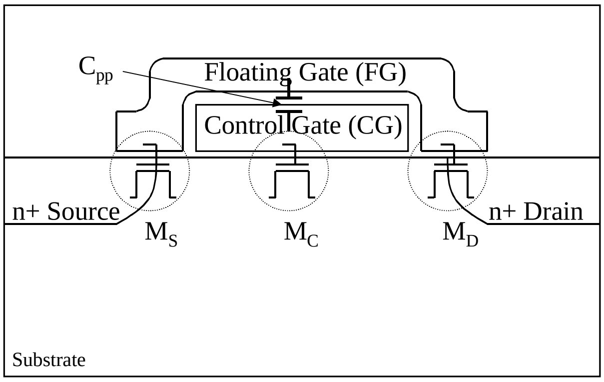


Figure 5. Model of operation for the TFG cell

M_S and M_D are equivalent to stacked-gate cells with CG controlling the channel through coupling onto FG via C_{pp}. M_C is a standard MOSFET controlled by CG directly. In the erased (low V_t) state with a positively charged FG the turn-on operation is determined by M_C, it being the higher V_t transistor in this case. It is the V_t of this native CG transistor M_C that determines turn-on of the cell.

With negative Q_{fg} on FG in the programmed state, again the higher V_t transistor, now M_S, dominates and defines the turn-on for the TFG cell.

It is this ability, in the programmed state, for M_S to control the turn-on or subthreshold region of operation which allows the subthreshold method of extraction [8] to be applied as the TFG is now analogous to a stacked-gate cell.

Using measurements from a TFG cell and TFG dummy cell a α_{cg} value of 0.86 was extracted. This compared to a designed α_{cg} of 0.79. This is to be expected as the extracted gate coupling ratio using the subthreshold method is known to be approximately 10% larger than the layout value due to a reduction in the C_{total} value from a depletion capacitance in the subthreshold regime [9].

5. TFG Macromodel

Using the previously described model of operation for the TFG (see figure 5) the device can be divided into three transistors, each represented by a BSIM3 MOSFET model. With the addition of a capacitor network to represent the floating gate voltage, the macromodel shown in figure 6 can accurately represent the read characteristics of the TFG cell [10].

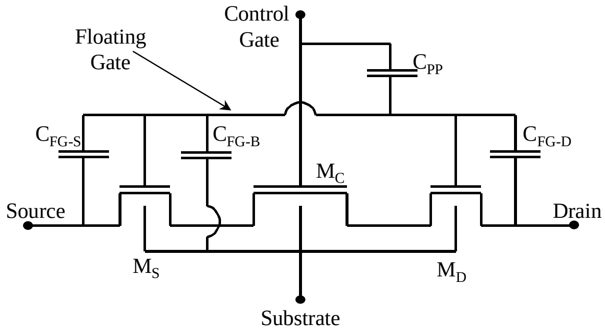


Figure 6. Three transistor macro model for the TFG cell

Figure 7 compares the measured and simulated results using the macromodel. It is observed that the model accurately represents both the V_t-shift and the g_m change for various states of program and erase.

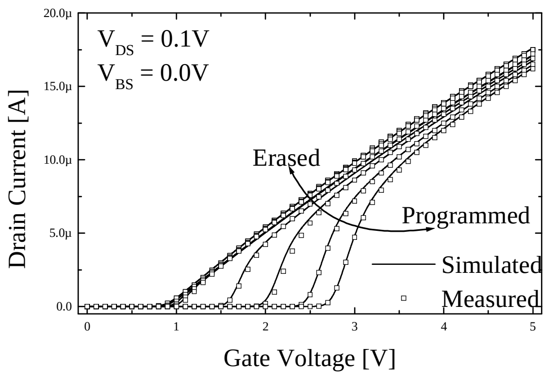


Figure 7. TFG characteristic in various states and the macromodel fit

6. Summary

A novel TFG NVM cell structure has been presented which is low power, reliable and easy to implement in a standard CMOS technology. It possesses an inherently high gate coupling ratio which is advantageous for low voltage Fowler-Nordheim operation. A macromodel of the cell was proposed which accurately represents the read characteristics of the cell.

7. References

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