Temperature-Dependent Characteristics of an n^+-InGaAs/n-GaAs Composite Doped Channel (CDC) Heterostructure Field-Effect Transistor

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Abstract

The temperature-dependent characteristics of an n^+-InGaAs/n-GaAs composite doped channel (CDC) heterostructure field-effect transistor have been studied. Due to the reduction of leakage current and good carrier confinement in the n^+-InGaAs/n-GaAs CDC structure, the degradation of device performances with increasing the temperature is insignificant. Experimentally, for a 1×100 μm^2 device, the gate-drain breakdown voltage of 24.5 (22.0) V, turn-on voltage of 2.05 (1.70) V, transconductance of 161 (138) mS/mm, output conductance of 0.60 (0.60) mS/mm, and voltage gain of 268 (230) are obtained at 300 (450) K, respectively. In addition, the studied device also shows good microwave performances with flat and wide operation regime.

1. Introduction

Practically, there is a growing need for higher temperature tolerance in aircraft, automotive, space technology, and other applications [1], [2]. However, due to poor Schottky characteristics and an increase of substrate leakage path, leakage currents increase considerably with increasing the temperature. Therefore, when the temperature is increased, the degradation of device performance includes: (i) the increase of leakage current, output conductance, and threshold voltage, and (ii) the decrease of breakdown voltage, output current, transconductance, and voltage gain are found. In addition, in GaAs based HFETs, it is favorable to use an InGaAs layer to replace the GaAs as a channel layer due to its higher mobility, peak electron velocity, and lower effective mass [3], [4]. However, the lower InGaAs energy gap may induce impact ionization in the InGaAs layer under high electric field [5]. Therefore, the device performance including leakage current, output conductance, voltage gain, and breakdown voltage are degraded considerably. To overcome these disadvantages, a novel device using an InGaAs/GaAs composite doped channel (CDC) structure is proposed to achieve high device performances and high-temperature operation capability. Experimentally, low leakage current, low output conductance, high voltage gain, high breakdown voltage, and good performances at higher temperature regimes are obtained.

2. Experiments

The studied device was grown by a low-pressure metalorganic chemical vapor deposition (LP-MOCVD) system on a (100)-oriented semi-insulated (SI) GaAs substrate. The epitaxial layers consisted of a 0.5-μm thick undoped GaAs buffer, a 500-Å thick undoped $In_{0.49}Ga_{0.51}P$, a CDC structure including a 150-Å thick doped GaAs ($n=5 \times 10^{17}$ cm^{-3}) and a 50-Å thick doped $In_{0.2}Ga_{0.8}As$ ($n^+=4 \times 10^{18}$ cm^{-3}) channel, a 300-Å thick undoped $In_{0.49}Ga_{0.51}P$, and a 500-Å thick doped GaAs ($n^+=4 \times 10^{18}$ cm^{-3}) cap layer. The drain-source ohmic contacts were formed on n^+-GaAs cap layer by alloying evaporated AuGe/Ni metals at 400 °C for 1 minute. The n^+-GaAs cap layer was removed and then the gate Schottky contact was achieved by evaporating Au metal on the undoped $In_{0.49}Ga_{0.51}P$ layer. Finally, materials underneath the gate feeder were completed removed by using wet etching to develop the airbridge gate structure which includes multiple piers between gate pad and active region. The used gate dimension is 1 × 100 μm^2.

3. Results and Discussion

The corresponding band diagram of the studied device is illustrated in the Fig. 1. The undoped wide-gap $In_{0.49}Ga_{0.51}P$ (~1.92 eV) material is used as Schottky gate and buffer layer. The upper $In_{0.49}Ga_{0.51}P$ layer can provide good Schottky characteristics. The lower $In_{0.49}Ga_{0.51}P$ layer is used to suppress the substrate leakage current through the substrate leakage path [1], [2]. The n^+-$In_{0.2}Ga_{0.8}As$/n-GaAs layers form the CDC structure. The narrow InGaAs layer is used to introduce the channel quantization effect [6], [7]. Thus, the effective energy-gap of InGaAs ($E_{g,InGaAs}+\Delta E$) channel can be increased. The n-GaAs channel can improve the operation capability under higher electric field. Hence, the impact ionization effect can be avoided and the leakage current minimized. In addition, the large conduction band discontinuity (ΔE_C) at the

$In_{0.49}Ga_{0.51}P/In_{0.2}Ga_{0.8}As$ and $GaAs/In_{0.49}Ga_{0.51}P$ interface can provide better carrier confinement in the channel. It is believed the device performance can be improved even at higher temperature.

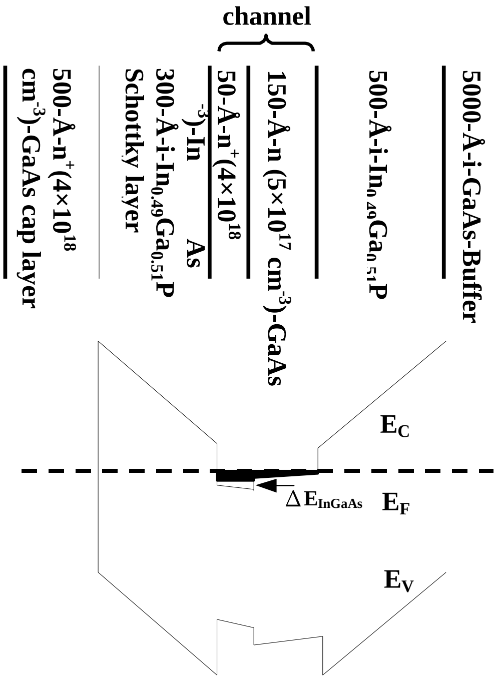

Figure 1. The schematic cross section and corresponding band diagram of the studied device.

The measured gate-drain current-voltage (I-V) characteristics of the studied device at room temperature is illustrated in Fig. 2. The reverse gate-drain breakdown voltages BV_{GD} and forward turn-on voltage V_{on} as a function of temperature are revealed, respectively, in the upper and lower inset of Fig. 2. BV_{GD} and V_{on} are defined at a gate current level of 0.5 mA/mm. BV_{GD} (V_{on}) values are 24.5 (2.05), 23.9 (1.97), 23.4 (1.93), 23.0 (1.85), 22.6 (1.79), and 22.0 (1.70) V at the temperature of T=300, 330, 360, 390, 420, and 450 K, respectively. Due to the increase in the tunneling current and reduction in energy-gap, BV_{GD} and V_{on} decrease with increasing temperature. However, the device still shows high BV_{GD} and V_{on} at high temperatures and the rates of decrease with temperature are only on the order of 6.8×10^{-4}/K (BV_{GD}) and 1.14×10^{-3}/K (V_{on}). It is believed that these temperature-dependent characteristics are attributed to: (1) the properties of wide-gap InGaP gate insulator, (2) the reduced sidewall leakage current and impact ionization current, and (3) good carrier confinement in the n^+-InGaAs/n-GaAs CDC structure. In addition, the studied device shows relatively high V_{on} values. This indicates the forward leakage current is reduced and the large forward gate-source voltage swing can be obtained.

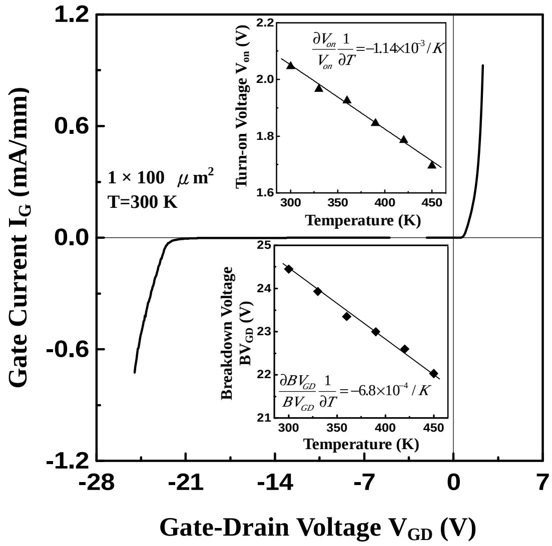

Figure 2. Measured gate-drain I-V characteristic of the studied device at room temperature. The upper and lower insets show V_{on} and BV_{GD} versus temperature, respectively.

Figure 3 shows the common-source I-V characteristics of the studied device measured at various temperature. All I-V curves show good pinch-off and saturation characteristics. The maximum applied gate-source voltage is +1.5 V and no significant gate leakage current is found. This indicates that the high turn-on voltage associated with good Schottky behavior and good carrier confinement are obtained in the studied device.

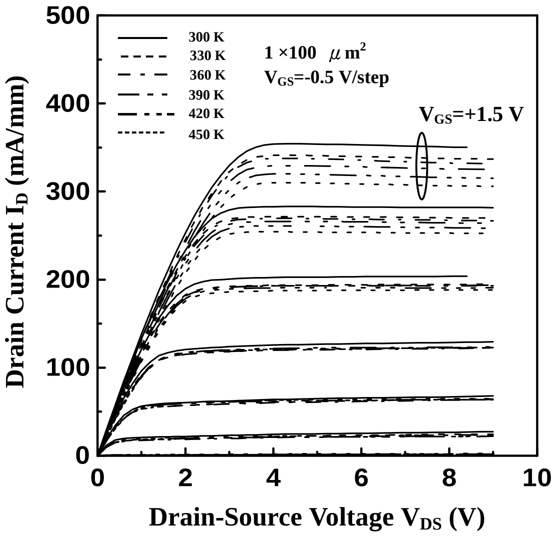

Figure 3. The common source I-V characteristics of the studied device at different temperatures.

Figure 4 shows the gate current I_G versus gate-source voltage V_{GS} at room temperature and 450 K at V_{DS}=4.0 and 8.0 V, respectively. The gate leakage currents are less than 1.6 and 22 μA/mm at room temperature and 450 K under the typical biased condition from V_{GS}=+1.0 to -2.0 V. The undesired bell-shaped behavior, usually found in InGaAs channel FET [4], is not observed. As seen from the schematic band diagram in the Fig. 1, the studied device can provide good carrier confinement and increase the effective energy-gap of the InGaAs layer to eliminate the impact ionization effect. Therefore, the leakage current can be reduced significantly at room temperature and even at higher temperature.

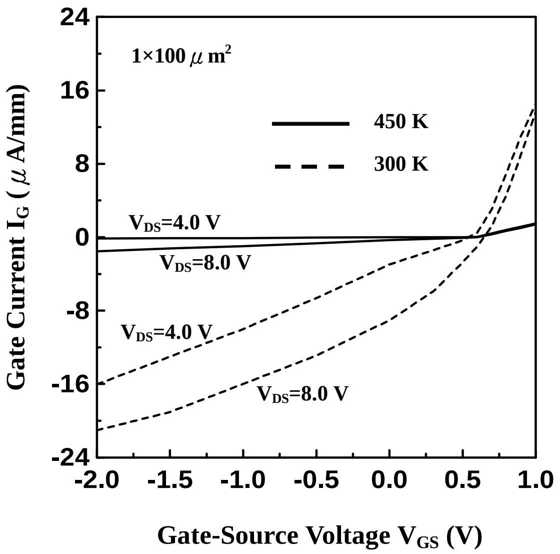

Figure 4. The gate current I_G versus gate-source voltage V_{GS} at room temperature and 450 K at V_{DS}=4.0 and 8.0 V, respectively.

Figure 5 shows the A_V (g_m/g_{ds}), g_m, and g_{ds} as a function of temperature at V_{DS}=6.0 V and V_{GS}=+0.5 V. g_{ds} values are 0.60, 0.61, 0.61, 0.61, 0.60, and 0.60 mS/mm at 300, 330, 360, 390, 420, and 450 K, respectively. It is found that g_{ds} shows low values and is insensitive to an increase in temperature. This indicates that the increase of leakage current with increasing the temperature is insignificant. The corresponding g_m values are 161, 155, 151, 147, 141, and 138 mS/mm. Therefore, high A_V values of 268, 254, 248, 241, 235, and 230 are obtained at 300, 330, 360, 390, 420, and 450 K, respectively. In addition, the studied device shows good microwave characteristics. The unity current gain cut-off frequency f_T and maximum oscillation frequency f_{max} are 15.9 and 30.5 GHz, respectively, under the bias condition of V_{GS}=+1.0 V and V_{DS}=6.0 V. Furthermore, device also maintains 80% of its f_T and f_{max} peak values over a large range of drain current between 30 to 360 mA/mm.

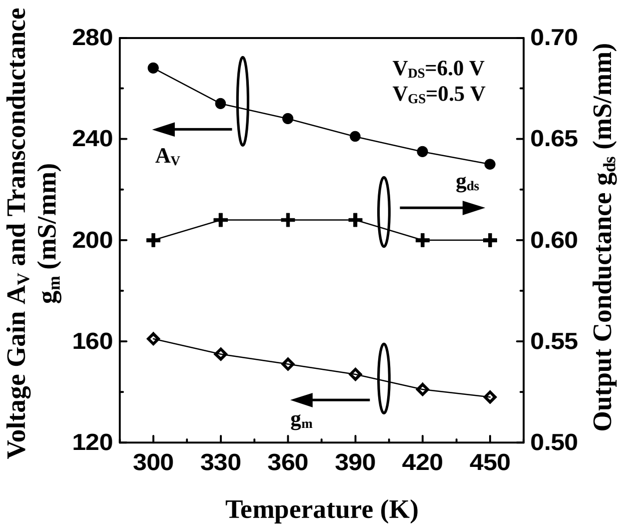

Figure 5. The measured voltage gain A_V, transconductance g_m, and output conductance g_{ds} as a function of temperatures at V_{DS}=6.0 V and V_{GS}=+0.5 V.

4. Conclusion

The temperature-dependent characteristics of an n^+-InGaAs/n-GaAs CDC heterostructure field-effect transistor have been studied and reported. The n^+-InGaAs/n-GaAs CDC structure is used to reduce the leakage current and hold good carrier confinement in the channel. Experimentally, it is shown that the degradation of device performance with increasing temperature is insignificant. For a 1×100 μm^2 device, the gate-drain breakdown voltage of 24.5 (22.0) V, turn-on voltage of 2.05 (1.70) V, transconductance of 161 (138) mS/mm, output conductance of 0.60 (0.60) mS/mm, and voltage gain of 268 (230) are obtained at 300 (450) K, respectively. In addition, the studied device also shows good microwave characteristics with flat and wide operation regime. Therefore, the studied device is suitable for high-temperature and microwave circuit applications.

References

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