

Knowing the Key Factors in RF Power Amplifier Design

Stephan Weber

Infineon Technologies, Balanstr. 73, 81541 Munich, Tel. +43-89-23428722

stephan.weber@infineon.com

Abstract: The key factors of narrow-band RF power amplifier design are presented. The design procedure is demonstrated on a new 1st 1W-2.4GHz PA in Silicon technology and new supporting software tools.

1. Introduction

Although radio and amateur radio are a bit old-fashioned, today a lot of engineers have to deal with RF, e.g. on topics like cordless telephones, mobile phones or wireless LAN. For some main-stream systems like GSM or AMPS, complete RF power amplifiers are available from module manufacturers. That eases the application, because they normally have 50 Ω RF IO's. But such modules are quite expensive, MMIC's are often cheaper, especially in Silicon technology. For some systems even a discrete solution might be competitive. In these cases - or for module or chip design - a much more detailed know-how is needed.

2. Design

On system level such things as RF TX power at the antenna, power-time template and spurious signals are specified. So the best way to design an RF PA is starting with a level diagram. From this you get the output power of the PA. After designing the final output stage with its matching networks you get the input power needed to drive the last stage. Step-by-step you can go backwards to the first PA stage which is normally connected to a modulator, VGA or VCO. S-parameters are only a good characterization for small signal circuits. Power amplifiers are often very nonlinear and the S-parameters will depend on power level. Despite this S-parameters measured at the input port at the power level also used in the application are a very good starting point for the design of the input matching network. Even more critical is the output of an RF power amplifier. Power match based on small-signal S-parameters will result in highest small-signal power gain but for RF power amplifiers the output power itself and the efficiency (normally specified by the so-called power added efficiency $PAE = (P_{out} - P_{in}) / P_{DC}$) are much more important. So the question is: What impedance Z_{Lopt} should be applied at the amplifier output to get a given output power with best efficiency? Many people are using an impedance tuner

to search for the best match in the lab by hand. This will lead to a complete different design procedure then typical used in small-signal amplifiers! Also here with some theory a faster way is possible.

The New 2.4GHz PA

Let us consider a concrete design problem: Design a matching network for a ISM 2400MHz power amplifier (free band for *industrial-scientific-medicine* applications). In the USA up to 1W (30dBm) antenna power is allowed for this frequency band. In reality some loss occurs after the PA, e.g. in the TX low-pass or band-pass filter and the antenna switch, so the PA is allowed to deliver app. 31dBm. Because you need some safety margin for component tolerances, temperature drift, changes of supply voltage and RF input power, a PA with a nominal output power of 29dBm will be well-suited. On the market there are not so much low-cost PA's which are able to deliver such high output power at 2.4GHz. For instance Infineon has a 1.9/2.4GHz Silicon PA family starting from a 22dBm Bluetooth PA up to the largest 29-30dBm device. The latter is the World's first integrated 1W 2.4GHz PA in Si technologie. All these devices are balanced PA's with push-pull input and output stage, featuring also system level functions like power ramping and power level selection. The balanced input eases the connection to the often also balanced transceiver output. To save board space and external components many system functions are included in these PA devices, such as power ramping and antenna switch drivers. A nice feature is the power select function. With two digital pins you can select four different output power levels, e.g. according the distance between handset and base station. For the balanced output we need a balun (*balanced-to-unbalanced*) to convert the push-pull signal to the normally used single-ended signal (e.g. for filters, PIN diode switches and monopole antenna).

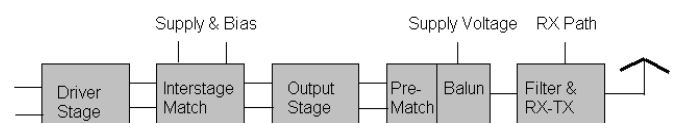


Figure 1 : Focused 2-stage PA system topology

The Optimum Load Impedance

The output power depends not only on the PA device but also on supply voltage V_{CC} (due to $P = V_{rms}^2/R_L \approx V_p^2/2R_L$) and best efficiency PAE can be expected if the PA is deep in the compression (in this case app. 40%). This operation is allowed for systems like DECT (digital enhanced cordless telephone), HomeRF or Bluetooth (both new standards for general-purpose RF interfaces, WLAN's, etc.), because they use modulation schemes (in these cases frequency shift keying) with constant RF envelope. In compression the PA output transistor (two for push-pull PA's) act nearly as a switch, i.e. it carries either a high current and has a low voltage drop or it needs to withstand a high voltage without carrying current. In both cases the dissipated power is low, which results in high over-all efficiency, if the transition between the two states is fast enough. For non-constant envelope modulation schemes like QPSK or 8PSK (e.g. IEEE801.11b or UMTS), you should look at the peak power, not the average power. This is needed because a PA in compression would create too much adjacent channel leakage power. The device is fabricated in a 4V-25GHz Silicon process, so for 29dBm the recommended supply voltage is 3.1V. Direct operation at two NiCd/NiMH cells is possible, because the supply voltage range starts at 1.9V. With this information we can calculate the optimum load impedance Z_{Lopt} . A nice program to do this is the AdLab tool ANPASS [1]. It uses the formula $R_{Lopt} \approx V_p^2/2P_{Wanted} \approx (V_{CC} - V_{sat})^2/2P_{Wanted}$, which is pretty accurate for (non-distorted) class-A operation.. There are some uncertainties: 1st We can only guess the saturation voltage, which should be close to app. 0.2V, because it's a low-voltage bipolar design. 2nd We operate in deep compression, so the class-A approximation is not valid. For instance for class-E [2] the voltage swing is not $2 \cdot (V_{CC} - V_{sat})$ but app. $3.5 \cdot (V_{CC} - V_{sat})$. For the class-A approximation and $V_{sat}=0.2V$ ANPASS delivers $R_{Lopt}=4.9\Omega$ for a single-ended PA and 19.6Ω for the balanced topology. This shows a clear advantage of the push-pull output, its impedance is already closer to 50Ω , so the amount of impedance transformation is lower. The result is a *reell* value for the impedance (19.6Ω , so 9.8Ω for each side) which is not truly realistic with real world transistors and finite package inductances. So ANPASS delivers the correct value for an idealized PA. For compressed class-B operation a higher value of R_{Lopt} is a bit better for higher efficiency (say 11Ω , for class-E operation ANPASS delivers 5.64Ω for single-ended configuration). Using another AdLab tool called CSMITH we can start with the corrected value as the generator impedance and we can add the transistor output capacitance (app. 3pF with some series resistance representing losses in the Silicon substrate) and

the bond-wire inductance (app. 0.4...0.5nH and a small package capacitance) by hand.

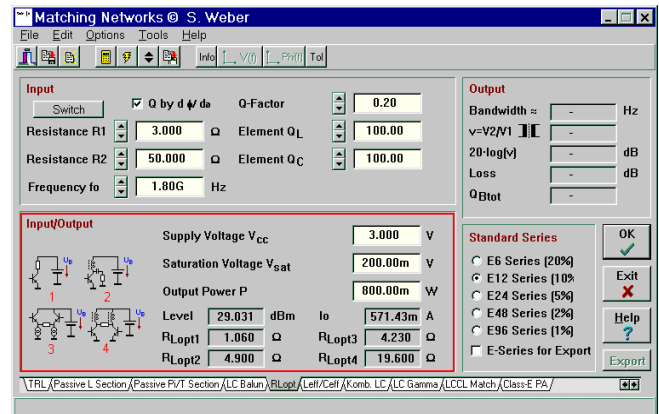


Figure 2 : Calculating R_{Lopt} via ANPASS

Note that CSMITH is able to use realistic element models with all major parasitics like series resistors or inductances, also a frequency sweep with graphical output for gain, MAG, return loss, etc. is available.

Matching Considerations

What we need now is a match from the transistor output to the balun. Because we need a DC-feed a L-type low-pass structure (high-impedance transmission line acting as a series-L followed by a shunt-C) is the easiest solution. In other situations a high-pass might be a better choice, e.g. in the interstage match where a DC-break is needed or some compensation of the drop of the transistor gain at higher frequencies is needed. A balun generally transforms a differential signal to a single-ended one (which is normally 50Ω) and vice versa. A standard LC balun can be designed using ANPASS. One open question is the intermediate balun input impedance. It's a good idea to take an intermediate impedance value (say 35Ω) so that the match is distributed over the first prematching network and the balun. This often gives the largest bandwidth and low tolerances. Other types of baluns are well-known (e.g. with transformers or $\lambda/4$ -transmission lines), but the LC all-pass is preferred here because it is very compact. Note, one balun capacitor could be merged with the shunt-C of the prematch.

Measurement Results

The resulting circuit is very close to what we have achieved in the lab. Of course in reality some tweaking is always needed in GHz circuits due to component parasitics and modeling inaccuracies. Also the impedances at the harmonic frequencies are not unimportant due to large signal operation. This behavior is known as harmonic matching, but it is not

easy to get advantage from this behavior at a GHz power amplifier.

For higher output power levels the impedances become very low (e.g. typically 2Ω at GSM levels) and a single-step matching network would result in a small bandwidth, and more important in tolerance problems. In these cases you need a multi-step match. In principle such a matching network can be designed in the same manner using the Smith chart, although it is not easy to optimize both losses and bandwidth. The main problem is that in the Smith chart you normally calculate at one frequency, so you often don't get the bandwidth advantage of more complex circuit structures like Chebyshev filters. In CSMITH you can do such a design, because Monte-Carlo analysis, frequency sweeps and also optimization (in conjunction with the general-purpose simulator APLAC [4]) are available.

Figure 6 shows the results of a 3-segment matching network. In the Smith chart, one key for getting large bandwidth is to stay close enough to the real axis. For a one-step match exactly the opposite occurs and you will "travel" along a long way, first to the outer regions and then to the desired center. The MAG (upper curve) shows that the element losses increases at higher frequencies, so it's not easy to get a true flat response. For the one-step match the bandwidth can be easily estimated by overlaying the constant-Q circles. For multi-step matching networks there is another more theoretical bandwidth limit by Fano, but the Fano-limit can be seldomly reached in practical RF circuits.

Technology Aspects and Parasitics

Currently we only look very roughly at the transistor. In fact, so far we only look at its saturation voltage, its current and voltage capabilities and its output capacitance. Of course other parameters such as feedback capacitance, transition frequency f_T , maximum frequency of oscillation f_{max} , maximum available gain MAG, stability factor k , current gain B , etc. are important - but not so much for the output match. Often a carefully chosen compromise is needed. For instance transistors with high f_T and f_{max} (like the new Silicon-Germanium technologies) have a high power gain G , which is advantageous for high PAE and getting a low number of RF stages. But these transistors tend to have low breakdown voltages and might be less stable. As a rule of thumb the supply voltage should not exceed the transistors V_{CEO} , although breakdown behavior also depends on the impedance at the transistor base ($V_{CEO} < V_{CER} < V_{CES}$). Your transistors should be stable at the operating frequency ($k > 1$), so the MAG is a good indicator for the achievable gain. If the device is not stable you need damping elements (e.g. series resistor at the base) or series or shunt feedback. In this case the achievable gain is close to the maximum stable gain MSG.

Not only the transistor is important but also all layout parasitics, like emitter-ground inductance, parasitics of SMD components and also on-chip parasitics [3]. Many chip designers think only the parasitic capacitances and series resistances are critical for their layout, but this is completely wrong for low-impedance RF circuits, such as PA's. Even small metal traces within the interstage match are critical. A typical $300\mu\text{m}$ metal trace will have an inductance of app. 0.3nH and a series resistance of 0.5Ω . Note that at 2.4GHz the inductance corresponds to $j4.5\Omega$, so the reactive part might influence the match and the frequency response seriously.

Most important is the ground inductance of the emitters (or sources for field-effect transistors) and in some cases ($f > 2\text{GHz}$, $P > 2\text{W}$, low V_{CC}) only chip vias (available in many GaAs or LDMOS technologies) or a balanced concept will help. For a GSM PA the peak-to-peak current is in the range of 4A , so even 100pH will cause a ripple of $2.26V_{pp}$ at 900MHz . This is a non-negligible part of the supply voltage and will reduce power gain dramatically and influences also PAE and stability. On the other hand some emitter inductance can help if the input impedances become too low (e.g. $< 1\Omega$), which will cause matching problems. The bipolar transistor input impedance is app. $Z_{in} \approx Z_E \cdot \beta(f)$ with $Z_E \approx U_T/I_C + R_E + j\omega L_E$ and $\beta(f) \approx f_T/jf$. For high power RF amplifiers this will become $Z_{in} \approx 2\pi f_T \cdot L_E$. This is a nice result, because it is a real value which can be adjusted easily. Due to $P = I^2 R$ the input power is proportional to L_E/f_T , hence the power gain increases linearly with f_T/L_E . The other parameters are less important but e.g. base resistance r_{BB} and feedback capacitance C_{BC} have still a strong influence, especially on stability factor k and isolation.

Careful biasing and supply bypassing is needed because any RF PA will not create trouble only at the operation frequency. Especially at lower frequencies they often become unstable. In practice the transistor should "see" no too extreme impedances at all his 3 terminals all over its entire active frequency range. Often damping resistances are necessary and can be part of the bias network. It is very interesting to see that bypassing with high-Q capacitors is in many frequency regions much worse compared to caps with lower Q, hence larger series resistors. Very important is the minimization of any series inductance, sometimes you need 3 or 4 capacitors with well-chosen values.

3. Conclusion

Some people say simulating RF power amps is nearly impossible, but this is clearly not true. With careful modeling you can increase accuracy step-by-step. The remaining errors should be finally smaller than 1dB in output power and gain. To not overlook any aspect you should always ask yourself is what you calculate really

close enough to reality. Even circuits synthesis techniques will be applicable in the near future,

because the circuit topology catalog is limited and well-defined.

- [1] <http://www.weberconnect.com/adlab2.htm> - AdLab EE tool collection consisting of 11 programs
 [2] Class E - a New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifier, N.O. Sokal, A.D. Sokal, IEEE JSSC, vol. SC-10, no.3, pp. 168-176, June 1975
 [3] Modeling for Si-Bipolar Power Amplifiers, S. Weber, AACD Copenhagen 1998
 [4] <http://www.aplac.com>
 [5] <http://www.noblepub.com>

Table 1 : Summary of key factors in modeling for RF power amplifiers

Topics	Influence	Comments
Transistor models	May have a large influence, especially on interstage matching!	Gummel-Poon may be sufficient for Si, but high current/low voltage region is critical, also quasi-saturation and breakdown!
Capacitances to substrate	Often low influence (not for transistor or MOS-C capacitances)	This is different to low power/high impedance designs.
Series resistors	Medium influence. Look also at the on-chip MOS capacitances	Reduces gain
Series inductances	Large influence! Not only as feedback in BJT emitters stages	Changes frequency response
On-chip coils	Medium influence. A peak Q of 5..10 is realistic for Si technologies. Include the lines to the coil!	Modeling is not too difficult, but Q is limited for typical Si technologies
Package model	Strong influence due to series inductances	Not easy to model, e.g. there is no ideal ground in an RF circuit
Substrate model	Medium influence on bias and RF performance	Difficult to model, important for mixed mode designs
PCB and external components	Large influence	Grounding and crosstalk are difficult to model
Bypassing and biasing	Large influence on stability and linearity	Don't optimize only at the operation frequency

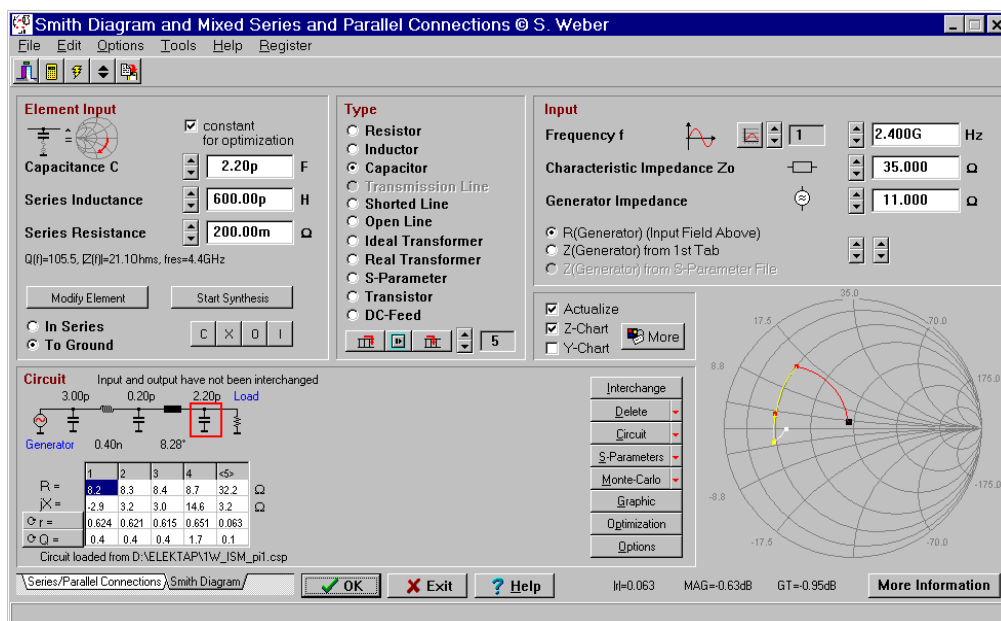


Figure 3 : PA output modeling in CSMITH and the L-type prematching network.

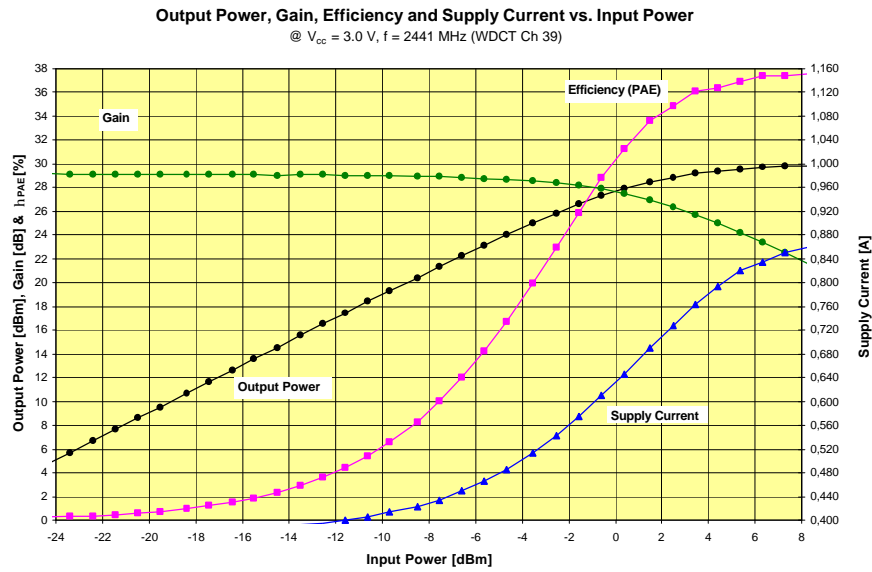


Figure 4 :
Measurement results
for the 29dBm Si PA

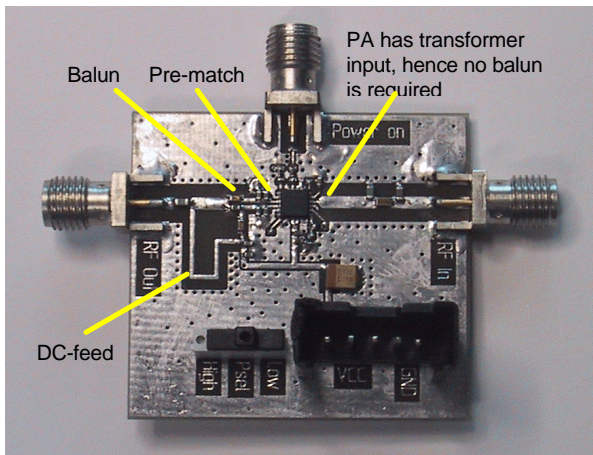


Figure 5 : The 2.4GHz PA board with the 2.4GHz-PA in VQFN20 package

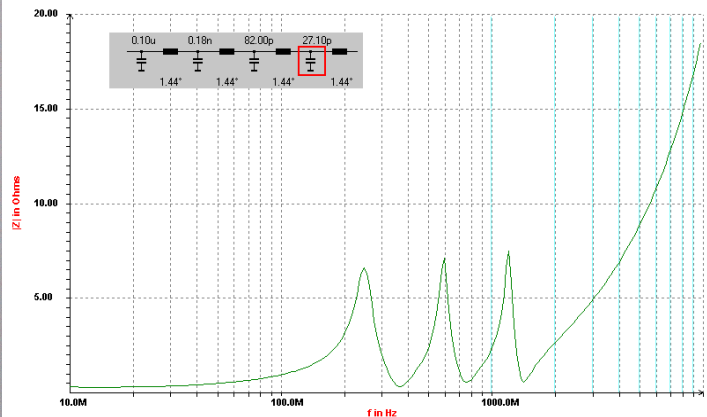


Figure 7 : CSMITH impedance graph of a well-designed supply bypass network with 4 standard

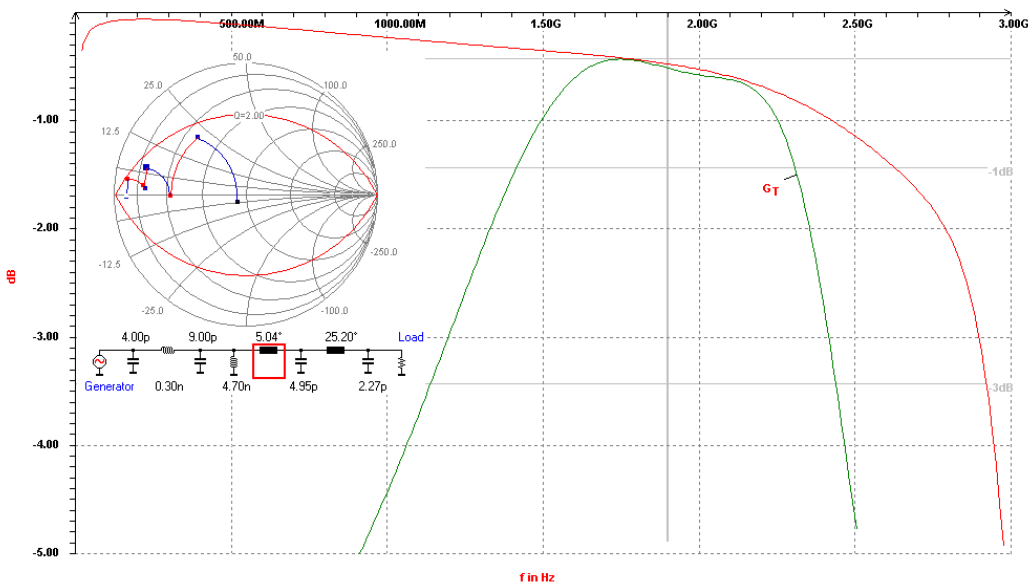


Figure 6 :
CSMITH results of a
1.9GHz 3-step
matching network
optimized for wide
bandwidth. A 1-step
match will only give
one third of the
achieved bandwidth.