Enhanced intrinsic gain (g_m/g_d) of PMOSFETs with a $Si_{0.7}Ge_{0.3}$ channel

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Abstract

PMOSFETs with a $Si_{0.7}Ge_{0.3}$ channel were fabricated. The intrinsic gain of the $Si_{0.7}Ge_{0.3}$ channel PMOSFET was compared to a reference Si PMOSFET, and was found to be enhanced by about 20 to 30 % for all gate lengths down to 0.3 μm. This enhancement is attributed to an increased effective mobility in the $Si_{0.7}Ge_{0.3}$ channel. The inclusion of a $Si_{0.7}Ge_{0.3}$ channel was found to degrade neither the output conductance (g_o) nor the breakdown voltage.

1. Introduction

The interest in strained SiGe PMOSFETs has up till now mainly been focused on digital applications [1-4], where the main objective is to enhance the PMOSFET performance in order to realize a symmetrical CMOS with matched conditions. In recent years, the SiGe channel devices have also attracted attention for potential uses in analogue applications [5] because of their high on-state current (I_{DS}) and transconductance (g_m) as well as low 1/*f* noise. Previous work by Prest *et al.* shows [5] on some increase in the intrinsic voltage gain for $Si/Si_{0.64}Ge_{0.36}/Si$ structures of 10 μm down to 0.5 μm channel lengths. However, this increase is shown to fall off with decreasing channel length. In this paper, we investigate the possibility of using SiGe channels for analogue applications and extend the analysis to include the effect on the parasitic capacitances and the intrinsic cutoff frequency for $Si/Si_{0.70}Ge_{0.30}/Si$ structures down to 0.3 μm channel lengths. The 1/*f* noise performance of the SiGe PMOSFETs will be discussed separately elsewhere [6].

2. Experiment

Figure 1 shows a schematic picture of the fabricated PMOSFETs. After well formation and LOCOS isolation an arsenic threshold voltage implantation was performed to set the peak doping concentration to $1 \cdot 10^{18}$ cm^{-3} beneath the epitaxial layers subsequently grown using reduced pressure CVD. The epitaxial layers, comprising a Si buffer, a strained $Si_{0.7}Ge_{0.3}$ layer and a Si cap, were selectively deposited at 650-700 °C and 20 torr, using SiH_2Cl_2, GeH_4, HCl and H_2. The nominal thicknesses were initially 10, 10 and 3 nm for the Si-buffer, $Si_{0.7}Ge_{0.3}$ channel and Si-cap, respectively. After epitaxy, a 3-nm thick gate oxide was thermally grown at 750°C in $O_2/C_2H_2Cl_2$, followed by deposition of an *in situ* boron doped polycrystalline Si layer as the gate. When gate patterning was performed, the source and drain areas were formed by extension and deep implantations followed by an activation anneal at 950 °C for 10 s in N_2. Details about the ion implantations are given in [7]. Metallization with Al on TiW followed by a forming gas anneal ended the fabrication process.

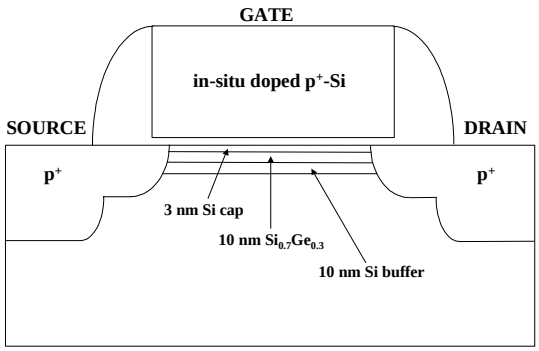

Figure 1. Schematic picture of a fabricated PMOSFET. The gate oxide thickness is 3 nm.

2. Simulations

Simulations using a 2D device simulator [8] were carried out to electrically optimise the PMOSFET structure incorporating a strained SiGe channel layer. It was found that the SiGe channel layer should contain at least 30 at. % Ge and that the thickness of the Si cap layer should be below 3 nm, when using a gate oxide of 3 nm thickness, in order to confine the majority of the carriers (holes) in the SiGe channel layer to attain desired gain performance. These abovementioned constraints

were used as guidelines for the structures investigated in this paper.

3. Results and Discussion

The results presented for the SiGe PMOFETs refer to structures with a nominal Si cap thickness of 3 nm. Figure 2 shows the drain current (I_{DS}) in saturation as a function of gate length measured at the same (V_g-V_t)=-0.5 V. The drain current increases by 40 % with the incorporation of a SiGe channel with 30 at. % Ge. This enhancement is, however, found to decrease with gate length below 0.5 μm. At 0.3 μm I_{DS} is enhanced by 20 %. This can be attributed to velocity saturation and/or an increased importance of the source/drain resistance [9].

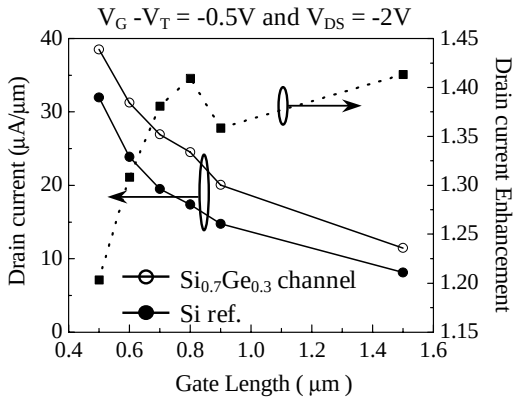

Figure 2. Drain current in saturation versus gate length for the Si and SiGe PMOSFETs. Also shown is the enhancement in I_{DS}.

The maximum low-field transconductance ($g_{m,LF}$) as a function of gate length is shown in Fig. 3. The enhancement in $g_{m,LF}$, comparing the SiGe devices to the Si references, ranges from 1.33 to 1.57 for 0.3 μm≤L_G≤1.3 μm. The increase in transconductance for the SiGe PMOSFETs is mainly a result of the increase in effective mobility as evidenced in Fig. 4. The effective mobility was extracted on large MOSFETs (L_G=10 μm and W=10 μm) using the split-CV method [10]. The enhanced effective mobility also leads to an increase in the maximum transconductance in the saturation regime ($g_{m,sat}$) for the SiGe PMOSFETs, as shown in Fig. 5. The enhancement effect decreases to $1.16 \le g_{m,sat}^{SiGe}/g_{m,sat}^{Si} \le 1.28$ for smaller gate lengths.

Figure 6 depicts the measured drain-source conductance in saturation (g_d). Only minor differences between the SiGe and Si PMOSFETs can be observed.

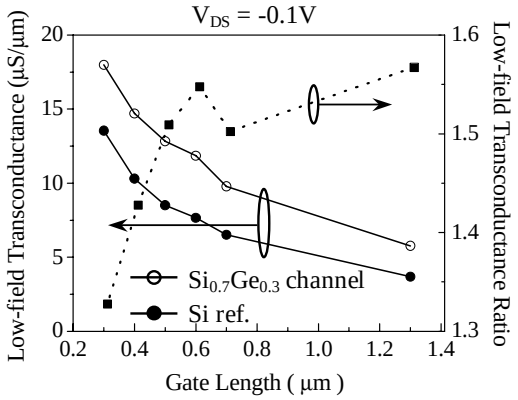

Figure 3. Maximum low-field transconductance and enhancement in $g_{m,LF}$ versus gate length.

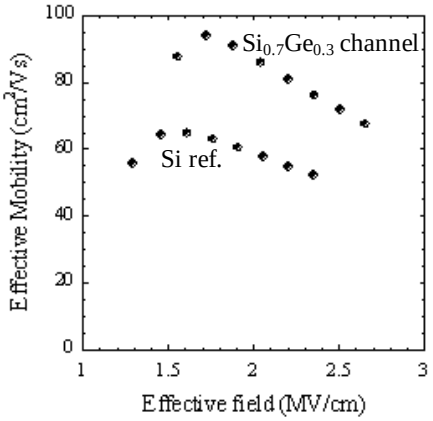

Figure 4. Effective mobility versus effective field for the Si and SiGe PMOSFETs.

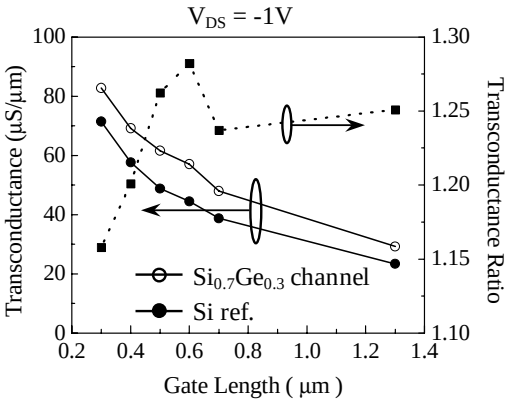

Figure 5. Maximum transconductance in saturation and the enhancement in $g_{m,sat}$ versus gate length.

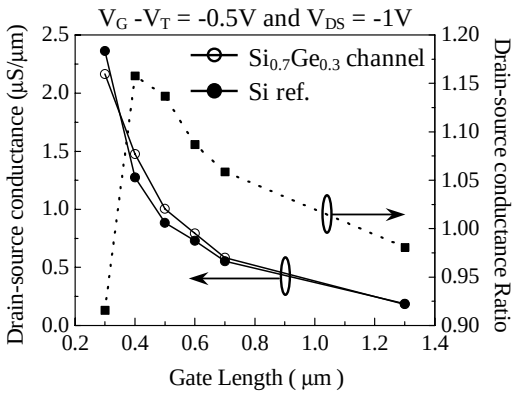

Figure 6. Drain-source conductance in saturation versus gate length. Also shown is the SiGe and Si PMOSFET drain-source conductance ratio.

The short channel effect (SCE) is found slightly better controlled for the SiGe devices as exemplified in Fig. 7 where the threshold voltage (V_t) roll-off is shown for both Si and SiGe PMOSFETs. This implies that g_d and thereby g_o, the output conductance, do not suffer from channel-length-modulation or drain-induced barrier-lowering effect. The breakdown voltage was extracted to –2.8V for both Si and SiGe channel PMOSFETs independent of gate length.

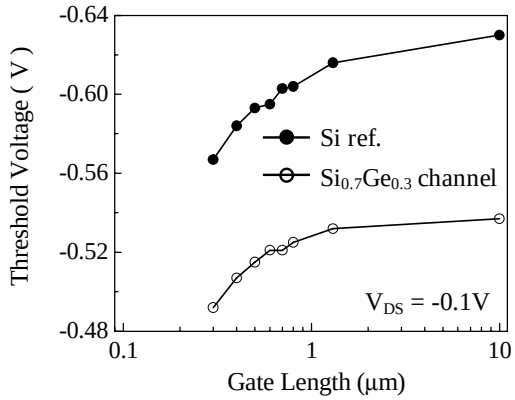

Figure 7. Threshold voltage roll-off for both Si and SiGe PMOSFETs.

The enhanced mobility in saturation coupled with the non-degraded output conductance result in an enhancement of the intrinsic voltage gain given by $g_{m,sat}/g_d$, as shown in Fig. 8. For both Si and SiGe transistors the intrinsic gain decreases when the channel becomes shorter, and the plotted curve falls off 15 % faster for the SiGe devices. Figure 8 also shows the intrinsic gain ratio (r_G).

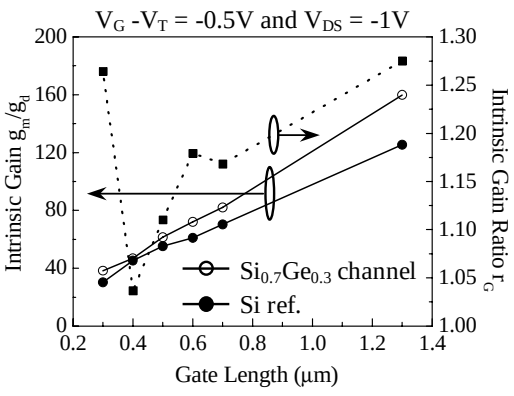

Figure 8. Intrinsic gain ($g_{m,sat}/g_d$) in saturation and the intrinsic gain ratio (r_G) versus gate length.

The intrinsic gain ratio (r_G), defined as

$$r_G = \frac{\left(g_{m,sat}^{SiGe} / g_d^{SiGe}\right)}{\left(g_{m,sat}^{Si} / g_d^{Si}\right)}, \quad (1)$$

gradually decreases from 1.28 to 1.04 as L_G is reduced from 1.3 to 0.4 μm. At L_G=0.3 μm, r_G is found to increase again to 1.26, which could be due to an enhanced velocity overshoot in the SiGe devices [11]. Here, $g_{m,sat}$ is the peak saturation transconductance.

For medium- and high-frequency signals, parasitic capacitances are the dominant factor influencing the performance of MOSFETs. In Fig. 9, the gate-to-channel capacitance (C_{GC}) is shown as a function of gate bias extracted from the split-CV method [10]. From the relationship between C_{GC} and gate voltage as shown in Fig. 9, the parasitic gate-to-source (C_{GS}) and overlap capacitances (C_{OV}) could be extracted [12], see the values in the figure.

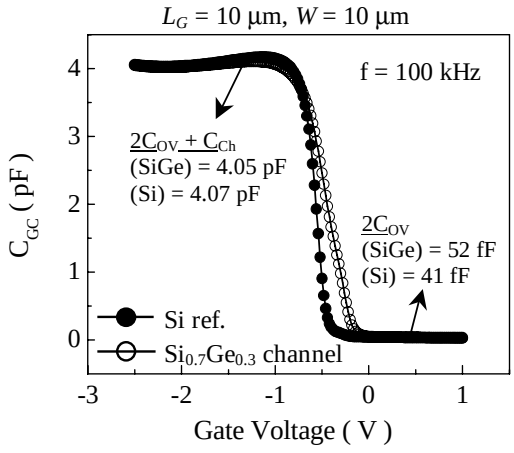

Figure 9. Gate-to-channel capacitance versus gate bias extracted on large PMOSFETs (L_G = 10μm and W = 10μm).

Since the SCE was minor in the saturation region (relevant for analogue applications) for the studied devices, the intrinsic gate-to-drain capacitance was neglected [9]. C_{GS} is found to be slightly smaller for the SiGe devices than for the Si devices, which is attributed to the presence of the Si cap in the former devices that pushes the inversion charge away from the Si/SiO_2 interface. Though C_{OV} is somewhat larger for the SiGe devices, it only amounts to about 1 % of C_{GS}.

The gate and source/drain areas were not silicided, hence no high-frequency measurements could be performed at this stage. Nevertheless, the intrinsic cutoff frequency (f_T) was predicted [9] to be a factor of 2.2 higher for the SiGe devices than the Si references due to the improvements in parasitic capacitances above. The improvements in g_m due to the enhanced effective mobility could further increase f_T by 20-30 %. However, the performance improvement including f_T seems to become less pronounced as the gate length is reduced.

4. Conclusions

PMOSFETs with a $Si/Si_{0.70}Ge_{0.30}/Si$ heterostructure channel have been fabricated and evaluated for their analogue performance. These devices showed improved current drivability and enhanced transconductance compared to the Si reference devices, while the SCE was kept negligibly small. The enhanced transconductance was shown to result from increased effective carrier mobility. As the source-drain conductance was unaffected by channel-length-modulation or drain-induced barrier-lowering effects, an increased intrinsic gain was obtained for the SiGe PMOSFETs. The buried channel nature of the SiGe PMOSFETs was also shown to give rise to a smaller gate-to-channel capacitance which in turn could lead to a two-fold increase in the intrinsic cutoff frequency. Although the enhanced performance seems to gradually fall off as the gate length decreases below 0.3 μm, PMOSFETs with a strained SiGe channel can become a prospective candidate for analogue applications.

Acknowledgments

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5. References

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