Self Heating in InP DHBT Technology for 40Gbit/s ICs

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Abstract

Self heating is investigated in InP/InGaAs DHBT's, a transistor technology well suited for 40 Gb/s IC's. An original approach associates experiments and simulations. InP DHBT's are shown to heat up even if their I-V characteristics do not present a negative differential output conductance as GaAs HBT's do. Their thermal resistance was found in the same range of values both using physical modeling and pulsed measurements coupled with electrical modeling.

1. Introduction

High performance InP/InGaAs DHBT's grown by chemical beam epitaxy (CBE) have been reported with 180 GHz f_T, 185 GHz f_{MAX}, a gain of 50 at a current density of 1x105 A.cm^{-2}, a breakdown voltage>5 V [1]. These features are required for circuits found in 40 Gb/s IC's. On the other side, the more established GaAs HBT's are known to be subjected to self-heating. It is attributed to the GaAs poor thermal conductivity (K_{GaAs}=0.455W.(cm.K)$^{-1}$) and to the large threshold voltage of these heterostructures. In comparison, there is few information available on self heating in InP HBT's [2-3]. Although K_{InP}=0.68W.(cm.K)$^{-1}$ is larger than K_{GaAs}, the former is significantly smaller than K_{Si}. The thermal conductivity of InGaAs is much worse with K_{InGaAs}=0.048 W.(cm.K)$^{-1}$ for X_{In}=53 %. Consequently, self heating occurs to some extent in InP DHBT's operated at high power densities and the consequences for circuit applications need to be investigated. It must be reminded that the threshold of Kirk effect occurs near a current density of 130 kA/cm^2 at V_{CB}=1.2V, and the powers dissipated are in the range of 260 kW/cm^2.

In this work, both static and pulsed I-V characteristics, nonlinear electrical modeling and 2D physical modeling are associated to evaluate self heating in an InP DHBT technology for 40Gb/s IC's.

2. Device structure and experimental set-up

Epitaxial structure: The epitaxial layer structure grown by CBE, consists of (from bottom to top) a N+ InP sub-collector, a N+ InGaAs collector contact layer, a 500 Å N+ InP layer, a 2500 Å undoped InP collector layer, a N InGaAsP layer, a 400 Å undoped InGaAs spacer, a 550 Å P+ InGaAs compositionally graded base, a 1500 Å N InP emitter, a N+ InP layer, and a N+ InGaAs emitter cap. A carbon doped graded base ($Ga_{1-x}In_xAs$) permits to increase the electric field in the base and to obtain a sufficient current gain with a relatively high doping level and thickness [4].

DHBT technology: To reduce the base-collector area and the base resistance, self-aligned HBT's are fabricated using selective wet chemical etchants and dry etching process. First, the TiAu emitter contact is lifted-off from the InGaAs cap layer; this metal is used as a mask for the emitter mesa wet etching. The etchants are H3PO4:H2O2H2O and H3PO4:HCl for the InGaAs and the InP layers. The wet etching leaves a slight undercut around the emitter contact.

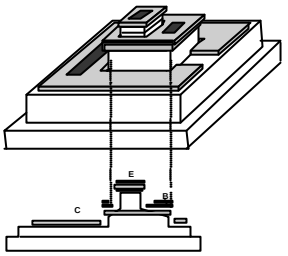

Figure 1. Schematic structure of self-aligned InP/InGaAs DHBT.

Static measurements have been performed using a HP4142B DC source combined with a HP8510C or Wiltron-360 NWA for S-parameters up to 50 GHz. Base and collector pulse measurements have been made through 50 Ω coaxial waveguide in order to avoid oscillation, with a HP8110A 50 Ω pulse/pattern generator and a HP54600 scope. In pulse regime, the transient base and collector voltages are analyzed in order to measure the very first electrical parameter variations during the transient regime of self heating.

3. Electrical modeling

The attractive aspects of the SPICE Gummel-Poon (SGP) model are its simplicity and availability in any

simulation software. Unfortunately, the SGP model is not able to predict with high accuracy special features of InP HBT, e.g. the complex nature of the base current, the Kirk effect regime. The quasi saturation regime, the bias dependence of the space charge capacitances and the bias dependence of the base resistance can only be approximated. Nevertheless it is possible to match the SGP model to the main DHBT physical features by twisting the original meaning of its parameters. Their limited number is an advantage in parameter extraction procedures.

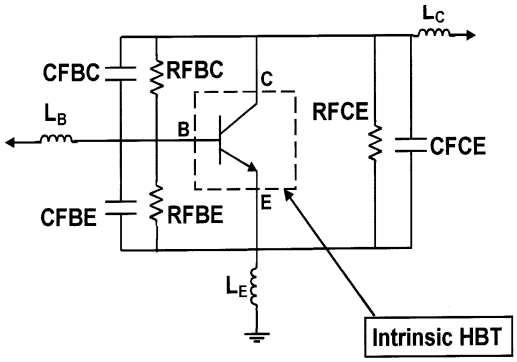

Figure 2. Equivalent circuit of SGP model showing parasitic access elements

The InP/InGaAs/InP DHBT operation is characterized by specific phenomena (nature of base current, Kirk effect, transit time contributions depending on the charging time …). A detailed examination of the SGP model properties allowed us to match it to InP DHBT technology using an original strategy detailed in [5]. Several access elements have been added to the kernel of the Gummel-Poon model (Figure 1) for modeling intrinsic reactive parasitic or extrinsic ones due to access lines, pads, discontinuities, transitions and electromagnetic coupling.

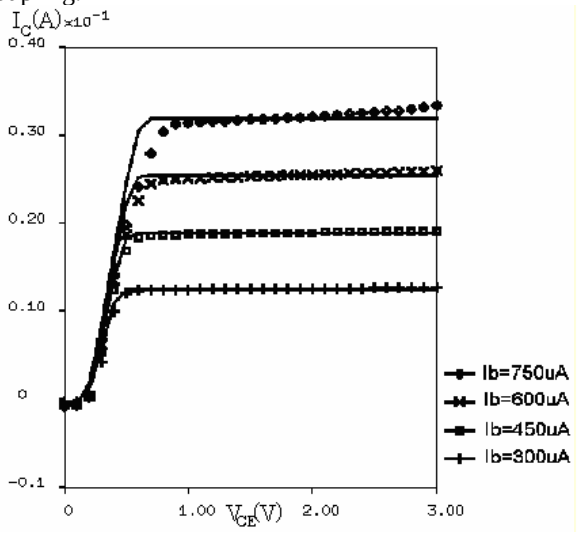

Figure 3. I_C-V_{CE} characteristics with I_B as a parameter for S_E=42.2 µm^2. Symbols are experimental data and full lines are modeling

The small signal equivalent circuit resulting from a linearization of the non linear Gummel Poon model appears to be well suited up to 50 GHz. The Figures 3-4 show the fit obtained in the I-V characteristics and the fit obtained in small signal regime (S parameters) at a given bias point. Modeling of the 4 noise parameters was also performed on the basis of the small signal equivalent circuit and allowed to obtain excellent results [6].

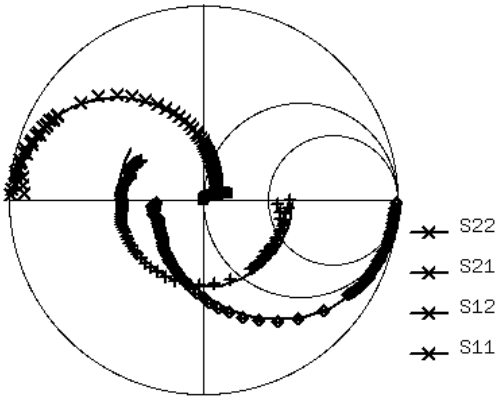

Figure 4. S parameters (0.5-40 GHz) of a DHBT with a carbon doped base, S_E=31.2 µm^2, I_C=37 mA. Symbols are experimental data and full lines are modeling

The GP model within FIT4 [7] has three parameters which allow to follow a temperature variation, namely the forbidden gap energy E_g, X_{TI} which controls the variation of the three saturation currents with temperature, and X_{TB} which controls the variations of the maximum current gain with temperature. There are "variants" of the GP model which give more freedom[8].

We have selected structures with carbon doping and a gradual base as their modeling is easier for a study of DHBT self-heating. We have introduced in the GP model the forbidden energy bandgap corresponding to the material composition at the emitter junction and we have maintained this value throughout the work of thermal modeling. This choice appears well suited due to the exponential dependence of the electron current with the intrinsic potential drop in the emitter junction.

Let us now consider the temperature dependence of the saturation value of the emitter current. If one only keeps the temperature dependent quantities in the expression of the saturation current I_S, one obtains,

$$I_S(T) = I_S(T_0)\,(T/T_0)^{X_{TI}} \cdot e^{\frac{-qE_G}{k}\left(\frac{1}{T}-\frac{1}{T_0}\right)}$$

Where T_0 is the ambient temperature. This approach is not fully satisfactory because electron transport in the base of InP HBT's is highly non stationary [9]. However it allows, in a first approach, to quantify the dependence of the saturation current with temperature. We have taken a value of X_{TI} equal to default value (X_{TI}=3), to 1.2 and to 5.7.

Starting from an investigation of InP DHBT's at variable temperature [10], we have determined the static current gain b for several current densities J_C and we have calculated the values of X_{TB} which express the dependence of b_{MAX} with temperature. A value X_{TB}=-0.05 was selected in the following, giving :

$$b_F(T) = b_F(T_0)\cdot(T/T_0)^{X_{TB}}$$

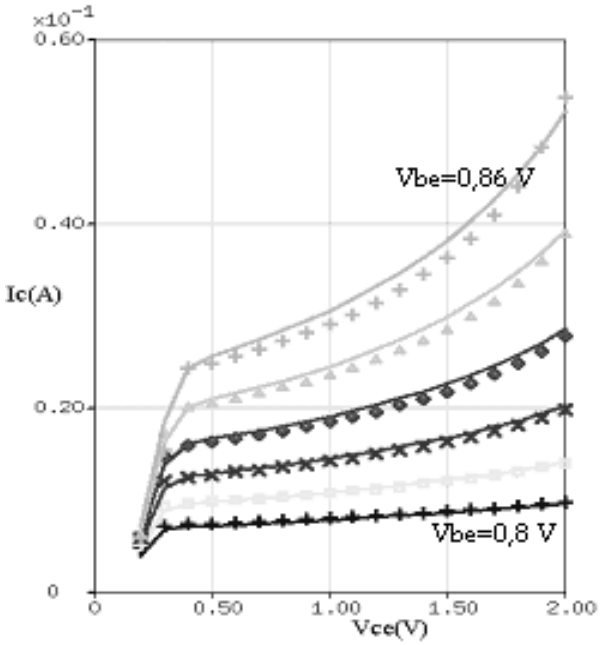

Figure 5. Pulsed I_C-V_{CE} characteristics of S_E=42.2 µm² DHBT with V_{BE} as a parameter

The procedure was repeated for different emitter areas, and the obtained thermal resistances are shown in Figure 6. The Figure 7 shows the correspondence between the bias points of a static I_C-V_{CE} characteristic of a DHBT with 42.2 µm² emitter area and the average temperature of the device.

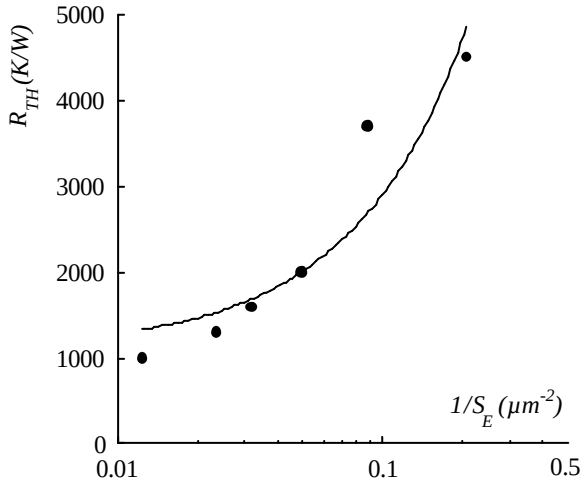

Figure 6. Thermal resistance variation of InP DHBT's with C doped base versus inverse of S_E. The line corresponds to a linear fit for X_{TI} =1.2

We have determined the large signal parameters of the GP model using pulsed measurements with a pulse generator HP8110A. Then the I_C-V_{CE} characteristics were fitted (Figure 4) as well as a Gummel plot in order to determine isothermal non linear parameters. The model was fitted on static I_C-V_{CE} charateristics delivered by a HP4142 at constant V_{BE}, with the thermal resistance R_{TH} as the only variable. This modeling approach of self heating is phenomenological and uses macroscopic electric parameters which do not translate the entire complexity of the phenomenon. In this way we attempt to reproduce the "average" heating in the transistors.

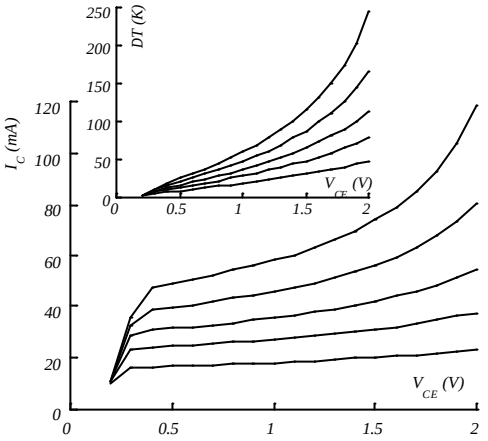

Figure 7. I_C-V_{CE} characteristics of S_E=42.2 µm² DHBT and corresponding device temperature versus V_{CE} for R_{TH}=1050 K/W for X_{TI}=3

For example, at V_{CE}=1.87 V (P=180 mW), the average device temperature rises up to 490K.

4. Physical modeling

We use a finite element bidimensional heat solver to investigate the self heating phenomenon in InP DHBT.

The heat (Fourier) equation is:

$$rc_p \partial T/\partial t = \nabla \cdot K \nabla T + H$$

where c_p is the calorific capacity, ρ is the crystal density, K is the thermal conductivity and H the heat source. In this model, K, ρ and c_p are temperature dependant. H is defined as $\boldsymbol{E}.\boldsymbol{J}$ where $\boldsymbol{E}$ is the electric field and $\boldsymbol{J}$ the current density. This approximation is far from being valid in the collector where transport is highly non stationary but it provides first results.

The variation of the vertical electric field is known thanks to 2D hydrodynamic simulations using ISE software. These simulations include a non local approach. The actual heat source corresponding to the actual energy exchanged between hot electrons and lattice will be soon taken into account in the Fourier equation solver. Concerning the heat source H described above, once the shape of E is determined, some specific values such as the maximum electric field both in the emitter and in the collector junction and the extension of

the space charge zones are fitted to the external bias conditions (V_{BE} and V_{CB}) by an integral calculation after removing parasitic access resistances. Several topologies of InP DHBT's have been investigated.

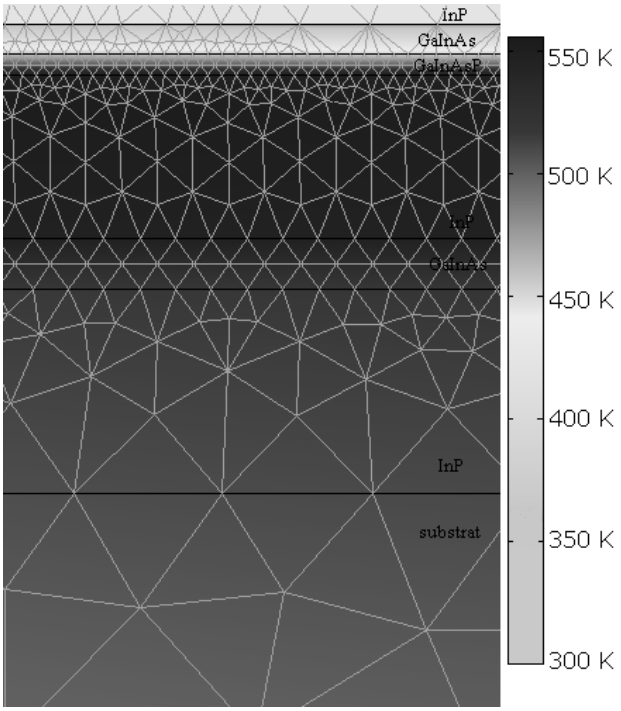

Figure 8. Zoom on DHBT hot spot under the emitter using 15000 nodes for 2D simulation of a sufficiently large structure. At a dissipated power P=180 mW the average temperature below the emitter and in the active zone is about 487K

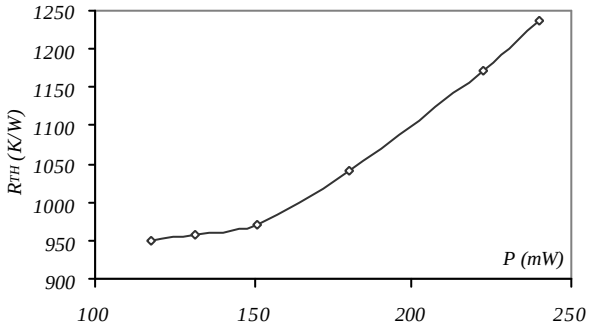

Figure 9. Variation of thermal resistance versus dissipated power for InP DHBT with S_E=42.2 µm²

Figure 8 shows the temperature in the heart of the devices below the emitter contact. One can observe that the collector is the hot area due to the peak of electric field at the entrance of the collector junction. In order to estimate the thermal resistance we have calculated the average temperature in the active area at the vertical of the emitter contact. The thermal resistance corresponding to the bias conditioned chosen in Figure 8 is 1041 K/W that is close to the value obtained by the experimental/electrical modeling approach described in Section 3.

The Figure 9 illustrates for the DHBT with 42.2 µm² emitter area the variation of the thermal resistance versus dissipated power. The previous electric modeling gives for X_{TI} = 1.2, 3 and 5.7 a thermal resistance of 1300, 1050 and 770K/W. Thermal resistance of 1050K/W, corresponding to X_{TI} = 3, is in reasonable agreement with the results of Figure 9.

5. Conclusion

An original investigation of self heating in InP DHBT has been performed mixing experimental and modeling approaches. InP DHBTs have been shown to heat up even if their I-V characteristics do not present a negative differential output conductance as GaAs HBT do. The values of the thermal conductance determined using either physical modeling or pulsed measurements coupled with electrical modeling are well consistent.

6. References

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