A 12Volt, 12GHz Complementary Bipolar Technology for High Frequency Analogue Applications

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Abstract

In this paper we report a new 12volt, high performance, highly competitive silicon complementary bipolar technology. NPN and vPNP devices have been fabricated with cut-off frequencies greater than 12GHz and breakdowns not less than 12volts. Two optimization techniques are discussed that can be used to improve the cut-off frequency of the vPNP device independently of the NPN. The resulting process is considered ideally suited to the manufacture of highly linear 1GHz operational amplifiers.

1. Introduction

To meet the challenge of high performance analogue applications we have developed a complementary bipolar process technology that combines good performance with high operating voltage. We have sought to make the process highly performance- and cost-competitive by combining careful process optimization with the use of wholly silicon substrates. We have adopted the complementary approach as it enables more efficient design of power consumption stages, linear operational amplifiers, active filters, laser drivers and synthesisers. We have adopted silicon substrates to reduce costs. Complementary bipolar processes fabricated using SOI substrates have been reported elsewhere e.g. [1]. Our high voltage complementary bipolar technology is fully isolated and includes a full suite of passive components. In this paper we outline the process and describe process techniques that can be used to optimize vPNP performance for specific applications. We report first results on NPN and vPNP devices with cut-off frequencies of 12GHz and breakdown voltages greater than 12V.

2. Experimental details and results

The 12V analogue complementary process, "HJV", was developed to add to an earlier complementary process, "HJ", designed for RF digital applications. Process HJ has been described in detail elsewhere [2]. The HJV high voltage NPN and vPNP transistors are shown schematically in cross-section in figures 1 and 2 and typical device parameters are shown in Table 1.

Briefly, the HJV process comprises double polysilicon self-aligned technology which includes small emitters, etched polysilicon with TEOS oxide planarisation, narrow trench isolation (for high packing density and low parasitic capacitance), deposited planarised silicon dioxide inter-metal dielectric layers and composite oxide/nitride passivation. The process includes NPN transistors, vertical vPNP transistors, lateral PNP transistors, high and low value polysilicon resistors, low value capacitors, integrated inductors, ESD protection and substrate contacts.

For full triple-layer metallisation the HJV process uses 8 photo masks more than a comparable NPN-only process. The additional photo operations are for low tolerance implant clearance masks. The buried layers for the vPNP are formed by deep implants, optimized for zero defects, but without any degradation in performance. Contact to both NPN and vPNP collectors is made by deep implanted collector “sinks”. The n-type epitaxial layer is determined by the NPN minimum breakdown voltage requirement, and over-doped with an implanted p-well for the vPNP. The minimum photolithographic feature is 0.6µm, for the NPN and vPNP emitters. Isolation is achieved by 0.8µm wide, 7µm deep trenches, lined with oxide and nitride layers and filled with polysilicon. Contact to the bases is made using polysilicon extended contacts, doped appropriately. The emitter-base junctions are formed from shallow base implants and implanted-polysilicon emitters and activated by 2-stage rapid thermal annealing. Low resistance contacts are made using platinum silicide. The process has 3-level metallisation with a contact pitch of 2.4µm at the first level.

Typical Beta-Early voltage products for HJV were 19200 and 2150 and collector-emitter breakdown voltages were >12V for both NPN and vPNP. Forward Gummel plots of NPN and vPNP transistors both exhibited good ideality and near-constant gain over 6

decades of current. Output characteristics for the NPN are shown in figure 3. The relationship between the NPN breakdown voltage BVceo and the thickness of the deposited n-type epitaxial silicon layer is shown in figure 4 for epitaxial layer thicknesses ranging from 0.7um to 1.8um. Breakdown voltages BVceo, BVcbo and BVces increased sequentially with increasing thickness of epitaxy. Cut-off frequency plots for the NPN at a Vce of 2V and 5V are shown in figure 5; the peak cut-off frequency at Vce=5V was 12.8GHz. For the vPNP, output characteristics are shown in figure 6 and a relationship similar to the NPN was observed between BVceo and the thickness of the epitaxial silicon layer (figure 7). Cut-off frequency plots for the vPNP at a Vce of 2V and 5V are shown in figure 8. In this case the peak cut-off frequency at Vce=5V was ~13GHz. The relationship between the vPNP cut-off frequency and BVceo is shown in figure 9.

In certain applications, e.g. operational amplifier design, the resulting chip could have improved performance if the technology available to the designer comprised transistors with matched or near-matched performance and characteristics. For example, in a complementary process the ideal technology would comprise completely performance- and breakdown-matched NPN and vPNP transistors. In practice a true complementary process is difficult to achieve due to the different diffusion characteristics of the relevant dopants and, for the case of silicon substrates, the need for substrate isolation. A near ideal situation can be obtained only after careful optimization of NPN or vPNP transistors. As we have shown here for HJV, after optimization, the cut-off frequencies for the NPN and vPNP devices closely match. Furthermore, the current densities at which the peak cut-off frequencies occur also closely match. This could have been achieved by utilizing an *extra* selective implanted collector, SIC. Here, instead, two non-SIC methods are considered, that can be used to optimize NPN and vPNP devices.

The first method involves optimization by consuming surface epitaxial silicon using a "sacrificial oxidation" technique [3]. The sacrificial oxidation technique is analogous to that of the selective implanted collector but with the advantage of superior control and manufacturability. The technique allows specific devices, NPN or vPNP, to be optimized. In a previous application the performance of NPN devices were enhanced while maintaining the vPNP performance. In this application the technique could be used to enhance the vPNP.

Figure 10 shows an SEM micrograph of a transistor during processing. In this example the device has had buried layer processing, epitaxy, deep trench etching and sacrificial oxidation. All oxide has been removed and the small, depressed region in the silicon resulting from sacrificial oxidation can be seen. The result is a localised reduction of the epitaxial layer thickness, a reduction in the breakdown voltage and an increase in cut-off frequency. Subsequent device fabrication is standard with no further modification necessary. Results from this technique have been reported previously and further results will not be reproduced here.

The second method involves optimization of the vPNP buried collector implant, epitaxial layer deposition and subsequent p-well over-doping. In this case, collector implant range, dose and surface concentration, epitaxy, auto-doping and p-well concentration need to be considered. As an example, the effect on the vPNP BVceo for three different buried collector schedules, over a range of epitaxial layer thicknesses, can be seen in figure 11. In this example the BVceo was reduced by up to 4V. Commensurate with the reduction in BVceo was an increase in cut-off frequency. The effect on cut-off frequency can be seen in figure 12 for two of the buried collector schedules of the previous figure; the increase was ~1.5GHz across the epitaxy range. The effect on cut-off frequency of p-well concentration can be seen in figure 13 for two p-well schedules; the increase was ~1GHz across the epitaxy range.

An important consideration when optimizing the vPNP is to maintain constant beta. Both methods described here maintain the same emitter-base processing throughout.

3. Summary and conclusions

A new 12volt, high performance, highly competitive silicon complementary bipolar technology has been demonstrated. NPN and vPNP devices with cut-off frequencies greater than 12GHz and with breakdown voltages greater than 12V, have been fabricated.

Two optimization techniques have been described to improve the cut-off frequency of the vPNP independently of the NPN. The optimization techniques can be used to tailor the process to specific applications. Here, the resulting process is close to a true complementary and is considered ideally suited to the manufacture of highly linear 1GHz operational amplifiers.

4. Acknowledgements

The authors would like to thank all members of the Swindon Foundry for wafer processing and D Sawyer for technical discussions.

5. References

[1] S Feindt et. al. "XFCB: A high speed complementary bipolar process on bonded SOI", Proc. IEEE BCTM, Minneapolis, USA, 1992, pp264-266.

[2] M C Wilson et. al. "Process HJ: A 30GHz NPN and 20GHz PNP complementary bipolar process for high linearity RF circuits", Proc. IEEE BCTM, Minneapolis, USA, 1998, pp164-167.

[3] M C Wilson et. al. "A new high performance complementary bipolar technology featuring 45GHz NPN and 20GHz PNP devices", Proc. SPIE Microelectronic Manufacturing, Santa Clara, USA, 1999, pp3881-10.

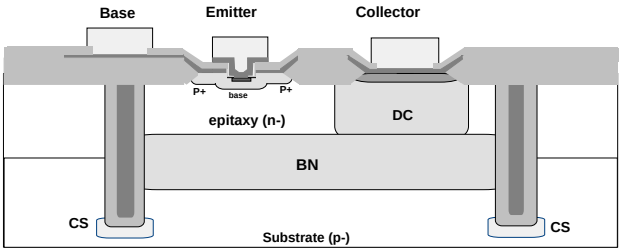

Figure 1. Schematic cross-section of a NPN transistor.

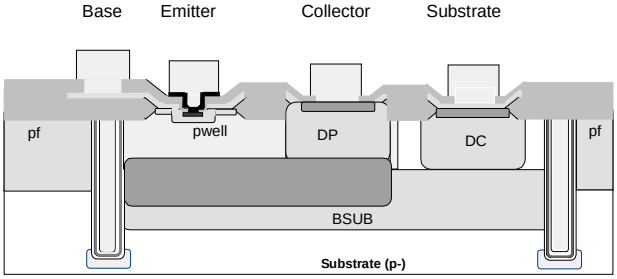

Figure 2. Schematic cross-section of a vPNP transistor.

Table 1. Typical “HJV" device parameters.

Param.	Condition	NPN	vPNP	Units
Emitter size		0.6 x 4	0.6 x 4	µm
Hfe	Vbe=0.7V Vcb=0V	160	50	
Hfe	Vbe=0.8V Vcb=0V	165	50	
Vbe	Ic=10µA Vcb=0V	750	775	mV
Vbe	Ic=200µA Vcb=0V	840	860	mV
BVcbo	Ic=1µA	30	26	V
BVces	Ic=1µA	30	26	V
BVceo	Ic=1µA	>12	>12	V
BVebo	Ie=1µA	3	3.5	V
Vaf		120	43	V
fT	Vce=5V	>12	>12	GHz
Re		9	9	Ω
Rb		245	450	Ω
Rc		105	345	Ω
Cje	Vbe=0V	13	11	fF
Cjc	Vcb=0V	5	8	fF
Cjs	Vcs=0V	15	28	fF

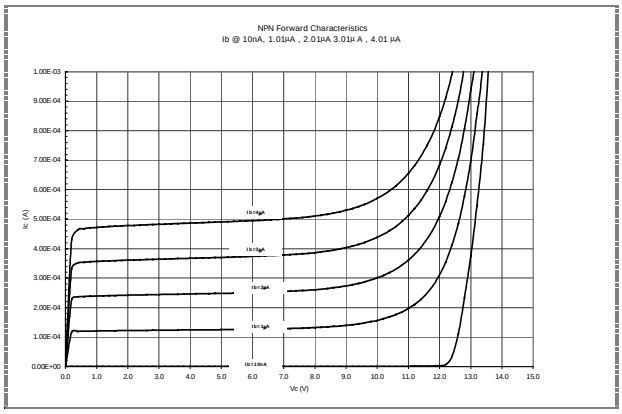

Figure 3. Output characteristics 0.6x4.0µm NPN

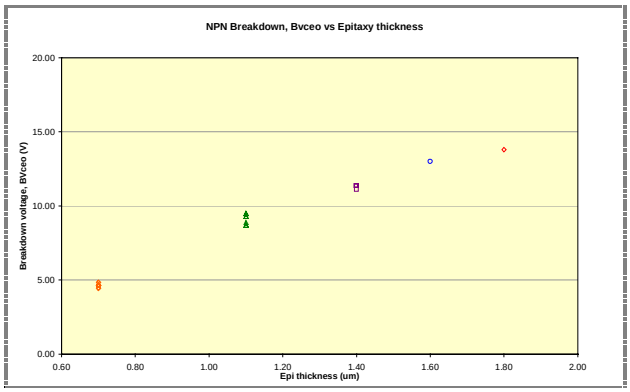

Figure 4. BVceo vs Epitaxial thickness for NPN

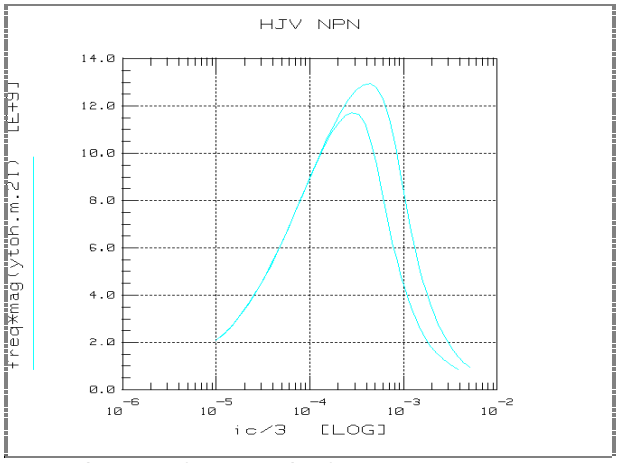

Figure 5. fT vs Ic plot for 0.6x4.0µm NPN

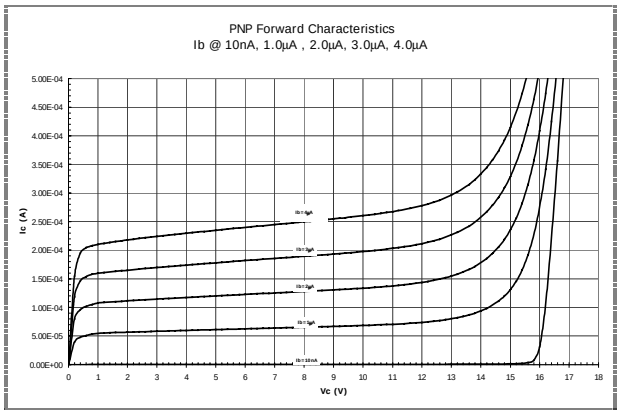

Figure 6. Output characteristics 0.6x4.0µm vPNP

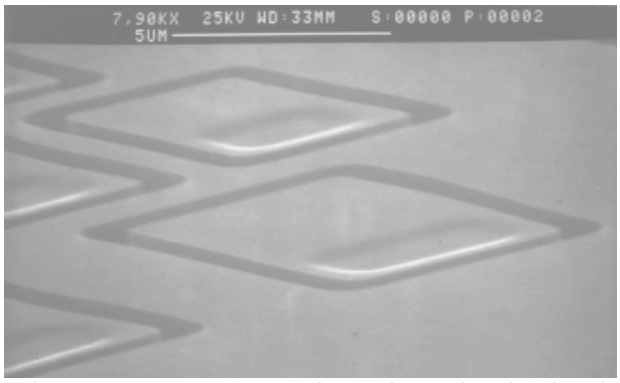

Figure 10. Part-processed transistor showing local thinning of epitaxy after removal of sacrificial oxide

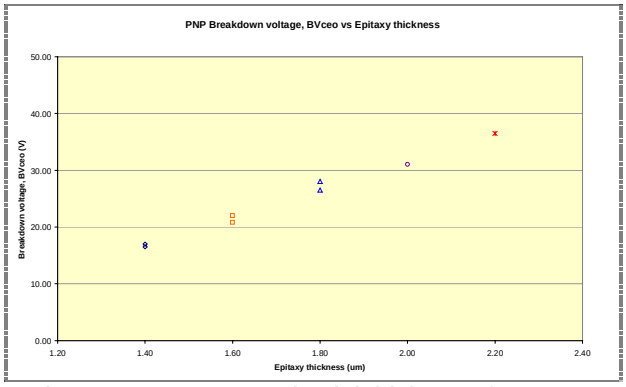

Figure 7. BVceo vs Epitaxial thickness for vPNP

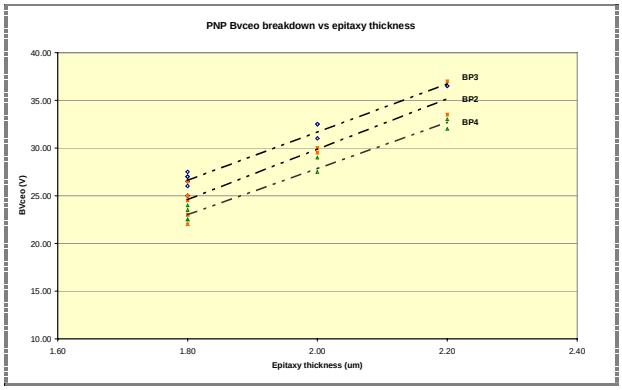

Figure 11. BVceo vs Epitaxy thickness for vPNP with 3 alternative BP collectors

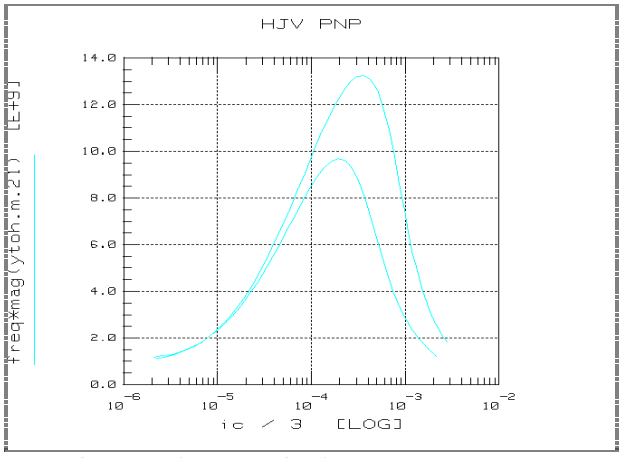

Figure 8. fT vs Ic plot for 0.6x4.0µm vPNP

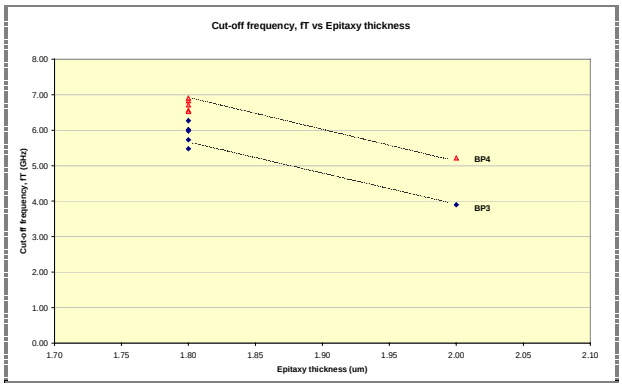

Figure 12. fT vs Epitaxy thickness for vPNP with 2 alternative BP collectors

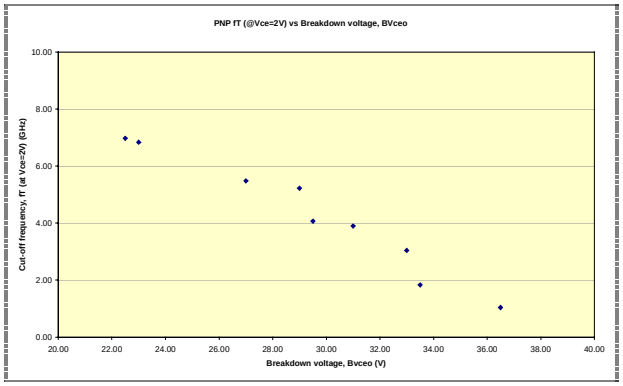

Figure 9. fT (@Vce=2V) vs BVceo for vPNP

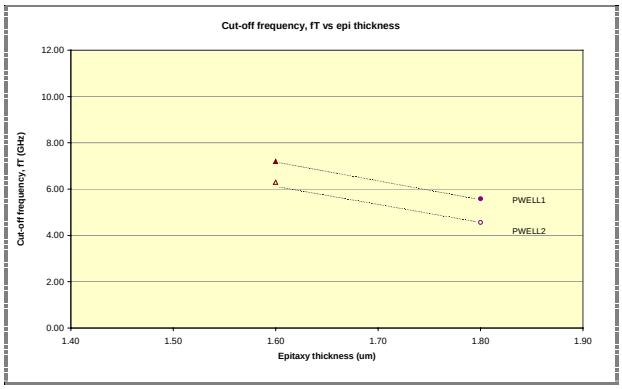

Figure 13. fT (@Vce=2V) vs Epitaxy for vPNP