Engineering of 80V Vertical n-DMOS in a 0.35 mm CMOS Technology

L. Delobel, D. Bolognesi, P. Moens and M. Tack
Alcatel Microelectronics, Westerring 15, B-9700 Oudenaarde, Belgium.
E-mail : *laurent.delobel@mie.alcatel.be*

Abstract

Today challenges in Smart Power applications require highly performant and robust High Voltage (HV) devices, integrated into CMOS technologies offering a high density of Low Voltage (LV) gates. Among HV transistors, DMOS transistors are the most compatible with a CMOS based platform and can be developed by the addition of few modular process steps. Within this class of devices, the vertical n-channel DMOS proves to be the most promising.

In this paper, several process and layout options are presented to describe the optimisation of a 80V vertical n-channel DMOS in a 0.35 mm CMOS based technology.

1. Introduction

DMOS transistors have shown to be very effective in circuits which should provide large output power at expense of a very low dissipation and where a large current density is often required. Their main advantages are the compatibility for integration into any advanced CMOS technology and the best trade-off between performance and area. Integrated DMOS have become the key devices for system level power integration and are broadly used not only in automotive applications, but also in PC and media peripherals, telecommunication, space and industrial electronics [1].

Two main classes can be distinguished depending on the direction of the current flow within the intrinsic device: lateral and vertical DMOS. However, the maximum blocking voltage (BVdss) and the specific on-resistance per unit of area (RdsonA) remain the main common key parameters of all DMOS transistors used for power applications [2].

Although the new standard for the automotive battery is 42V, the voltage requirement is much higher. The maximum operating voltage for full lifetime is 50V, with a dynamic over-voltage estimated in 8V. Extra 12V are usually desired for a charge pump to drive external switches. This leads to a required voltage up to 70V. Furthermore, a voltage window has to be foreseen as margin for ESD protection, bringing to a minimum voltage requirement of about 80V.

The implementation of additional HV transistors, either MOS or bipolar, within a CMOS technology is always a tough challenge. No alteration of the electrical performance of the CMOS logic (nor of embedded memories) is allowed, in order to guarantee full compatibility to existing libraries. Therefore, a modular approach has been chosen and most of the additional process steps are included in the early phase of the processing flow.

2. Device features and characterisation

The basic cross-section of a vertical nDMOS transistor is depicted in Figure 1. The new technology should evidently provide all necessary layers for such a device: thick epitaxy, n-doped buried layer and sinker, p-doped well or dual body implant, thick top metal layer.

A lightly doped n-epi is used: its thickness and doping profile are tuned for optimal trade-off between vertical and lateral devices. This n-epi realises the conductive channel for the current being collected by the N^+ buried layer underneath (BLN). The deep N^+ sinker acts as top drain connection and prevents also possible current leakages to the p-doped substrate, due to the activation of the parasitic substrate PNP, of which the emitter is represented by the p-doped body implant of the DMOS.

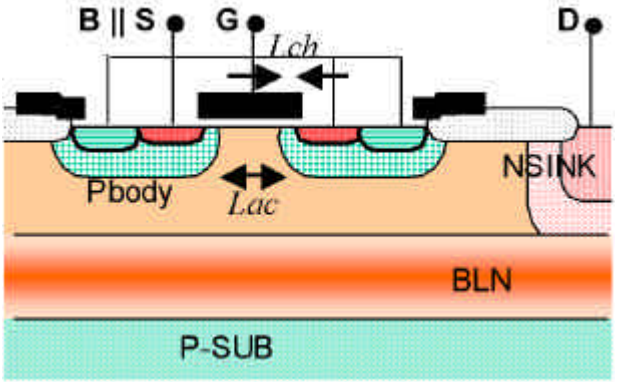

Figure 1. Cross-section of basic vertical nDMOS.

The tuning of the layers is done in function of optimised vertical devices (nDMOS, NPN, HV free-wheeling diode and ESD bipolar-alike protections). The preference for vertical current flow arises from the better heat sinking and the reduced carrier trapping at the surface, which represent a severe source of oxide degradation in lateral (D)MOS transistors [3].

In case of big switches the choice for a vertical n-channel DMOS is evident: it is floating up to the maximum isolation breakdown; it offers a high density, whatever is the layout (stripes, cells), because the source-to-source distance can be made considerably smaller than source-to-drain in a lateral non-Resurf

DMOS; it is intrinsically self-protecting to ESD stress, when its width is at least few tens of µm.

The (D)MOS devices in a 0.35 µm CMOS based technology have the standard gate oxide of 7 nm, for which the gate voltage is limited to 3.3V.

2.1. Process optimisation of BVdss/RdsonA

In a lateral DMOS device, BVdss is mainly defined by the distance from source to drain (i.e. length of field oxide between source active and drain active), and by the extension and doping of the drift region.

In a vertical device, the source is integrated in a big active area, in which the different cells are next to each other. The breakdown voltage is controlled by the vertical distance source-to-drain, i.e. the residual epi-thickness (T_{epi}) till the BLN, and by the edge structure of the device. Secondary parameters are the layout options (shape of the cells, Jfet width) and the junction profile of the p-doped body.

The doping concentration of the epitaxy has a very strong impact on the BVdss variation (Figure 2). The decrease of BVdss is not entirely proportional to the increase of the epitaxy doping. In the elementary theory, BVdss variation is hyperbolic when the depletion of the epitaxy from the bulk does not reach the BLN underneath, but it is linear when the depletion region enters the BLN, as observed on a different experiment with concentrations lower than C_0. The knee point between the two trends is close to C_0.

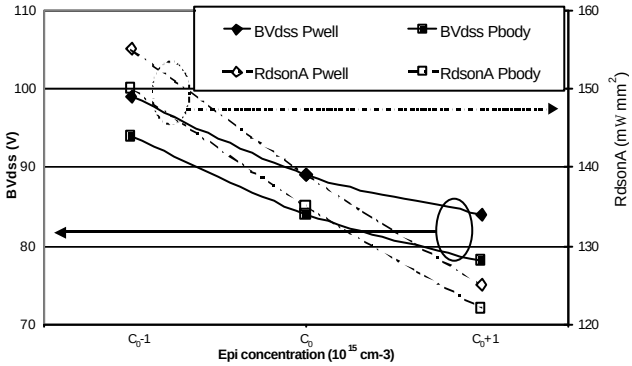

Figure 2. Variation of BVdss and RdsonA with epitaxy concentration (C0 is reference doping).

The channel of a DMOS can be made by using the standard (retrograde) CMOS Pwell, as by means of a self-aligned Pbody implant. A constant difference of 8 V between the two different channels, Pwell and Pbody, is evident from Figure 2. The Pwell mask is aligned with the active area, whereas Pbody is a LATID implant self-aligned to poly. To avoid punchtrough, Pwell channel must be not minimal to cope with mask alignment tolerances. The difference in BVdss is probably due to the variation in the body doping, impacting the voltage held between bulk contact and junction with the Epitaxy, as well as the junction curvature itself.

A similar analysis is done for the specific RdsonA, which is most relevant for the packing density of smart power IC's. The figures quoted in this article, in general refers to the Rdson per source pitch, that is the elementary vertical DMOS under each source including a normalized drain resistance contribution.

The impact of the epitaxy concentration on RdsonA is also shown in Figure 2. Its trend is close to the formula $A+\frac{B \cdot T_{epi}}{Nd}$, where B is a fixed parameter. Again, the effect of different channels is mostly related to the remaining free Jfet regions (coefficient B) and also to the channel resistance variation (term A). This formula however does not fully account for the variation of the Jfet resistance as a function of the epitaxy concentration.

T_{epi} is as well important for the breakdown (Figure 3). The increase of BVdss as function of the epitaxy thickness is close to the quadratic law expected for a 1-D junction. Such data allow an efficient modelling of the electrical performance of the device as a function of the process parameters.

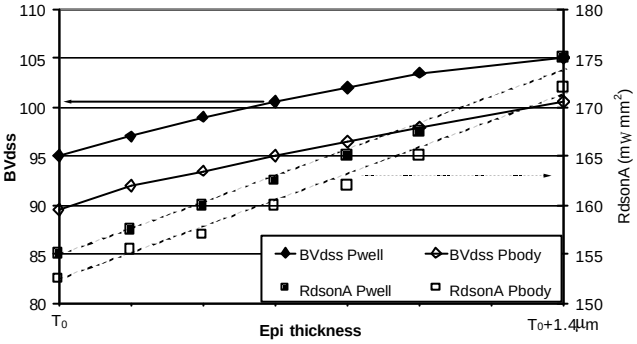

Figure 3. Variation of BVdss with Tepi.

In a vertical device, the use of buried layer (BLN) and N^+ sinker is mandatory to efficiently collect the drain current up to the surface of the silicon. Above a certain threshold dose of BLN, a drastic linear decrease of BVdss is observable (Figure 4). Furthermore, BVdss starts to show a big spread over the samples population. This is related to BLN up-diffusion. In the plateau behaviour, one can expect that the depletion layer from the p-body does not enter the BLN profile, thus giving a very reproducible breakdown voltage. When the BLN dose increases such that its up-diffusion interferes with the depletion layer, then BVdss decreases.

A longer diffusion drives BLN species deeper into the substrate, reducing the upward diffusion during the following thermal steps, thus resulting in a larger T_{epi}.

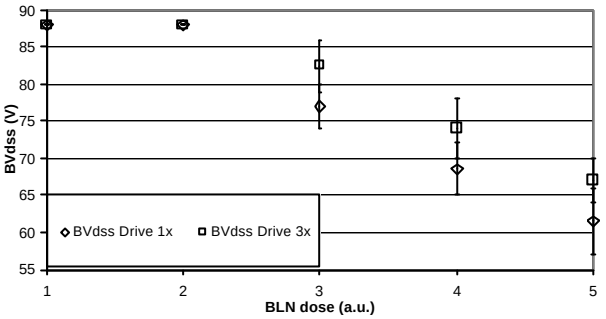

Figure 4. Variation of BVdss with BLN dose.

In an integrated vertical device, the optimization of BLN defines also the maximum size of the area containing folded sources, which all provide Ids current to the same drain termination, since the collection of the vertical current depends on this layer. The optimum sizing of the source can be extracted from the curves in Figure 5, in which RdsonA includes also the contribution of the drain branch. The source size (X axis) is given as spacing between the edge of two consecutive drain terminations. For a short spacing, the area pertinent to the drain is dominant, thus RdsonA is higher. When this parameter is much larger, the sources most far from the drain will have a higher access resistance due to the buried layer source-to-drain series resistance. After an optimum value, the increase of the device area is not compensated anymore by a further reduction of its resistance.

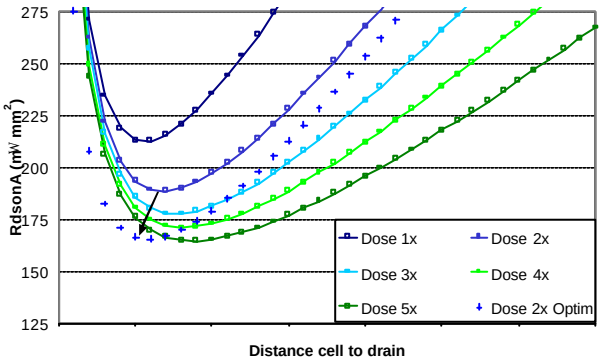

Figure 5. RdsonA as function of source size.

In the same plot, the dependence on BLN dose is visible, i.e. curves for multiple values of a reference implanted dose are shown. When BLN concentration increases, the optimum source size increase and the minimal RdsonA reduces, because it benefits of the effective current injection coming from this additional source area. The arrow shows the improvement obtained by a careful layout of the source edge towards the drain.

A way to improve the BVdss/RdsonA tradeoff in vertical devices is to modulate the surface doping, in order to decrease the Jfet resistance effect [4]. However, it should not impact too much the BVdss. The main results of these experiments are shown in Figure 6.

When the surface concentration raises from 0 (reference level) to 1x (a.u.), the BVdss changes by less than 3V for any epitaxy concentration, whereas the RdsonA reduces by more than 10%. When the surface concentration is increasing further, then BVdss is decreasing by few volts (more if the epitaxy concentration is larger), whereas the RdsonA is not improving significantly. For the highest epitaxy concentration, we see that RdsonA per pitch can be decreased from 155 to 135 $m\Omega \cdot mm^2$.

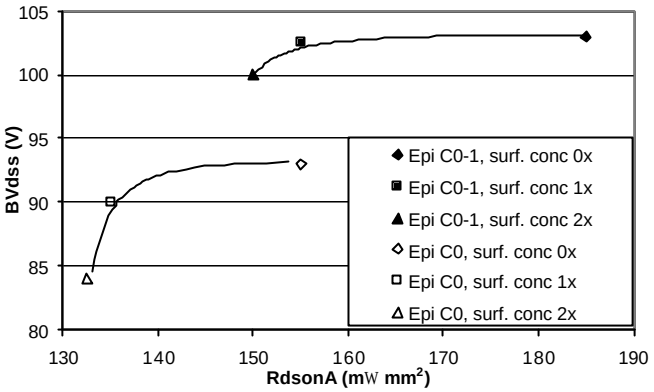

Figure 6 : Variation of BVdss and RdsonA with epitaxy and surface concentration.

2.2. Layout optimisation of BVdss/RdsonA

Out of the layout parameters of the vertical nDMOS, both the extension of the so-called JFET region (*Lac*) and channel length (*Lch*) (see Figure 1) influence the BVdss of the device. In Figure 7, the dependency on *Lac* and on the choice of the cell shape is shown.

Two common geometries, stripe and hexagonal (Hexa) cells, are compared. For Hexa, BVdss decreases when *Lac* increases and it is always lower than the one of stripe-shaped devices. In fact, the uncomplete merging of the depletion regions in the Jfet area, between adjacent sources of Hexa cells, makes BVdss occur there, due to the depletion layer curvature effect. In the case of stripe geometry, *Lac* is the same between parallel sources, thus opposite depletions always merge.

Lac has a direct impact also on RdsonA via the Jfet resistance (see Figure 7). A very large *Lac* increases RdsonA, however the measured Ron increases when *Lac* gets smaller, because the current flow is pinched between the two sources. On the other hand, RdsonA decreases less than the increment of the area of the device when *Lac* increases. Indeed the free Jfet region (at the surface) is not efficiently employed for the drift of the electrons (e^-), hence the area used by the device is bigger than what really needed for the current conduction [4].

The increase of RdsonA for very small *Lac* is likely due to a partial closure of the Jfet region. The resistance grows exponentially due to the filling of $\bar{e}$ in the Jfet region at a concentration much higher than the epitaxy itself, thus leading to velocity saturation, while the area of the device is decreasing linearly with *Lac*. There is therefore an optimum value of *Lac*, for which the use of the silicon area for device performance is optimised.

In case of devices with Hexa cells, the estimate of the optimum RdsonA can lead further to a 10% decrease.

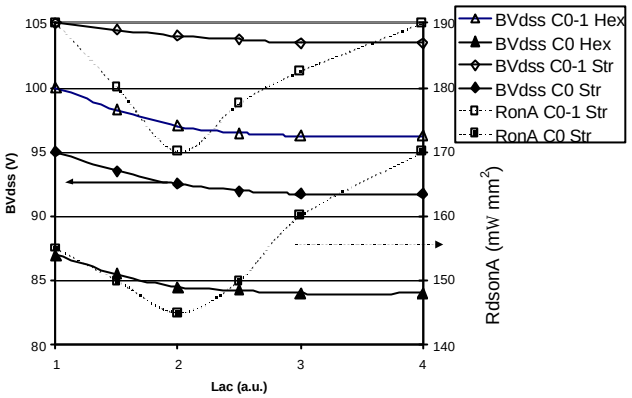

Figure 7. Variation of BVdss with Lac and comparison between Stripe and Hexa cell shape.

Finally a short *Lch* reduces BVdss because of the early punch-through to the source: otherwise, the impact of *Lch* is negligible. Nowadays, alignment tolerances are quite small hence the channel is well controlled and the self-aligned implant option is mostly used in RF devices.

3. Reliability aspects

In addition to the standard DC electrical characterisation, extensive reliability tests were performed to determine the safe operating area (SOA) of this device: 80V components should have full lifetime (25 years) up to Vds=62V. The hot-carrier tests [5] are made at Vds=70V and at Vgs corresponding to the largest I_{bulk}, which results are shown on figure 8.

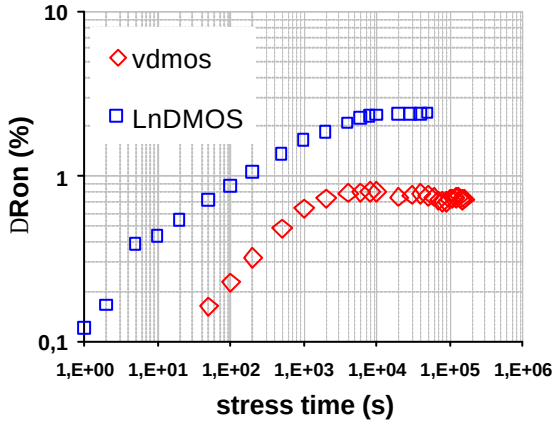

Figure 8. Hot Carrier degradation of Rdson of the devices: 80V VDMOS and lateral nDMOS.

The VDMOS has a lower hot carrier (HC) degradation compared to the lateral devices, due to the absence of the field oxide overlap along the electron current path.

Additionally, TLP measurements (100 ns current pulses) are also performed. The plot of Fig 9 shows how much the best selected 80V VDMOS is robust against ESD: a small driver with W=80 µm is already self-protecting against 4kV HBM.

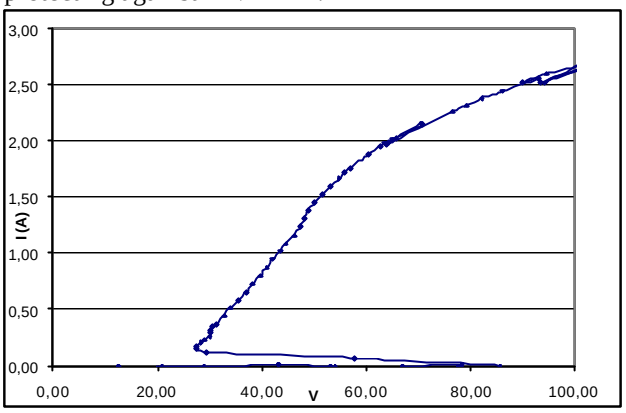

Figure 9. TLP curve of a 40 µm wide VDMOS.

4. Conclusions

The use of a vertical n-channel DMOS in a 80 V technology is a good approach for achieving low RdsonA device for big output drivers. A detailed analysis of the sensitivity of BVdss and RdsonA towards process and layout option is described in this article.

Out of these experiments, an optimised device has been selected. It has a RdsonA as low as 135 mΩ mm^2 and a BVdss around 90 V. Furthermore, this device is self-protecting against 4kV HBM ESD pulses, and its degradation is smaller than for an equivalent lateral DMOS. It should be noticed that for small analogue devices, LDMOS is still interesting due to the small area the device is using compared to the vertical device.

5. Acknowledgments

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6. References

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