High reproducible ideal SiC Schottky rectifiers by controlling surface preparation and thermal treatments

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Abstract

In this work, the effects of surface preparation on the forward I-V characteristic of Ni/6H-SiC Schottky diodes were studied. The ideality factor n and the barrier height F_B were found to be strongly dependent on the surface treatment prior to Schottky contact deposition. On the other hand, the diodes annealed above 600°C exhibited an almost ideal I-V curve, independently of the surface preparation. Further improvement in the barrier height distribution can be obtained by increasing annealing temperature up to 950°C.

The formation of nickel silicide was responsible for this behaviour and, under appropriate annealing conditions, may be the key to achieve a higher reproducible nearly ideal Schottky diode.

1. Introduction

Silicon carbide (SiC), because of its unique physical parameters (wide band gap, high thermal conductivity, high saturated electron drift velocity) has been used for the fabrication of high-power and high-temperature electronic devices [1]. In fact, for power devices applications, the wide band gap of SiC (3.0 eV for 6H-SiC and 3.2 eV for 4H-SiC) allows to reach high breakdown voltages, whilst the high thermal conductivity (4.9W/cmK) and saturation electron drift velocity ($2x10^7$cm/s) are fundamental for power dissipation and high frequency device operation.

The greatest progresses in SiC power devices have mainly taken place in the field of Schottky rectifiers, which are the least complex SiC power devices and, hence, excellent candidates for future commercialisation [2]. One of the common outstanding problems related to SiC device fabrication is the control of the surface preparation before the metal-gate deposition. For example, the electrical performance of a Schottky diode strongly depends on the quality of the metal-semiconductor interface, the latter being essentially determined by the surface preparation prior to metallisation. As a matter of fact, in many works, the surface preparation for SiC Schottky rectifiers has been proved to be a non-trivial issue and only poor reliability could be achieved [3-6]. Therefore, it is extremely important to find optimised procedures which enable to obtain electrically reliable metal/SiC contacts .

In this paper, several surface preparation methods were used before the metal deposition and the Schottky barrier height was determined by means of current-voltage (I-V) measurements. The aim of this work is to correlate the interfacial properties with the electrical behaviour, in order to optimise fabrication process and device performances.

2. Experimental details

The diodes were fabricated on epitaxial wafers, from CREE Research, Inc. The n-type epitaxial layer was 4 μm thick, and its carrier concentration ~ $3x10^{15}cm^{-3}$. The heavily doped substrate had a doping level of $7x10^{18}cm^{-3}$. After growing a thermal oxide layer by dry oxidation at 1150°C, a 1 μm thick oxide was deposited by chemical vapour deposition.

The device area was defined by standard photolitography combined with wet or dry etch. Four different etching processes were used in order to monitor the electrical performance of the devices as a function of the surface pre-metallisation treatment and find the optimal conditions for device fabrication: (a) wet etch in $HF:H_2O$=1:5, (b) wet etch in NH_4F:HF=7:1, (c) Reactive Ion Etching (RIE) by CF_4 gas source, (d) combined wet + dry etch (NH_4F:HF + RIE by CF_4).

A large area backside ohmic contact was formed by annealing in N_2 at 950°C a 100 nm thick Ni film. The Schottky contact, a 200 nm thick Ni film, was deposited on the wafer front side; a lithographic process defined a metal field plate over the oxide.

The electrical forward I-V characterisation of the diodes was performed on a probe station equipped with a Keithley 236, both before (as deposited) and after a rapid thermal annealing of the devices in the temperature range 600-950°C.

X-ray photoelectron spectroscopy (XPS) was used to monitor the presence of processing induced surface contamination on the samples while Atomic Force Microscopy (AFM) allowed to determined the surface roughness. Transmission electron microscopy (TEM) on cross section was also performed in order to monitor the metal/SiC interface. The structural characterisation of the Schottky metal after thermal annealing of Ni/6H-SiC unpatterned samples was done by means of X-Ray diffraction (XRD) analysis, in order to identify the phase transformation.

3. Results

The forward I-V characteristic of the Schottky diodes are shown in fig. 1 for the different surface pre-metallization treatments, both for the as deposited devices (fig. 1a) and for those annealed at 600°C in N_2 for 60 s (fig. 1b).
The first investigated method was a surface preparation based on the oxide etch done by means of a dip in diluted HF (HF:H_2O=1:5). In this case, nearly ideal Schottky diodes with an ideality factor n=1.07 and a barrier height Φ_B=1.25 eV were achieved . The devices show a linear characteristic over height orders of magnitude.
Although in this case good ideality of the devices was achieved, the etch process in HF:H_2O often resulted in a poor adhesion of the photoresist on the sample surface, thus leading, in turn, to a poor reliability of the geometry definition and to the difficulty to control the oxide ramp angle. In order to overcome this problem, buffered HF was used for oxide etch (NH_4F:HF solution). However, as can be seen from fig. 1a, NH_4F:HF etch only led to a non-ideal behaviour, i.e. n=1.77. The barrier height Φ_B value was lowered to about 1 eV.
For several applications, such as in MESFETs and SITs fabrication, reactive ion etching (RIE) is suitable for surface preparation before metal-gate deposition. However, when using plasma etching, a non-optimal choice of rf power and gas pressure could be detrimental for the device performances. Therefore, as alternative to the wet etch, RIE in CF_4 was used to prepare the sample surface before metal deposition. The rf power (300 W) and gas pressure (700 mTorr) were chosen to remove our thick densified oxide layer.
As can be observed from fig. 1a, also in this case, the forward I-V characteristics of the diodes show a non ideal behaviour with a very strong curvature, which indicates a wide distribution of barrier height. The higher value of the forward current measured in the low voltage region (<0.5 V) results in an average barrier height of 0.87 eV. Moreover, the calculated series resistance R_{on} of these device (205 mΩcm^2) was about one order of magnitude higher than the typical values found when after wet etch preparation.
As forth method, in the attempt of improving the forward I-V performances of the rectifiers, a two step preparation was developed, by combining a 8 min wet etch in buffered HF with a soft reactive ion etch (2 min). The measured values of the ideality factor (n=1.38) and of the Schottky barrier height (Φ_B=1.10 eV) demonstrate an improvement in the electric behaviour of the devices.

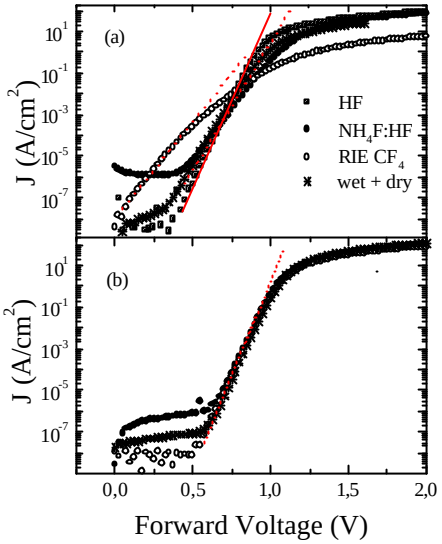

Figure 1: Forward I-V characteristics of Schottky diodes for different surface preparation methods as deposited diodes (a) and after annealing at 600°C (b)

In spite of the strong dependence of the device characteristic on the surface preparation, a significant modification of the metal/SiC interface, and then of the Schottky barrier height, can be induced by post-deposition thermal treatments. The latter can be clearly observed in fig. 1b, which depicts the forward I-V characteristics of the devices after a rapid thermal treatment in N_2 at 600°C.
Independent of the surface preparation, the ideality factor n decreases, tending to the ideal behaviour predicted by the thermoionic emission theory. On the other hand, the barrier height increases to values of 1.3-1.4 eV. In particular, fig. 1b reports the curves relative to the dry etched diodes (n=1.08, Φ_B =1.37 eV), the NH_4F:HF (n=1.16, Φ_B=1.31 eV) and the combined wet + dry etch (n=1.06, Φ_B=1.39 eV).

4. Discussion

In order to explain the experimentally observed strong dependence of the Schottky barrier height on the surface preparation method, both TEM of the Ni/SiC interface and chemical and morphological analysis of the surface (XPS and AFM) were performed.
In spite of the differences shown in the I-V characteristics, both in the case of HF and NH_4F:HF etch, AFM analysis showed very flat etched surfaces with the same value of roughness (RMS = 0.3 nm). Also XPS analysis was not able to show significant differences between these samples. However, the discrepancy from

the ideal behaviour (n=1.77) and the observed lowering of the average Schottky barrier height (Φ_B=1 eV), monitored after NH_4F:HF etch, could be explained by the presence of patchy contamination, i.e. a thin residual oxide layer not completely removed by this etch. The latter was confirmed by the cross section TEM image of the Ni/SiC interface prepared with this treatment, in which a discontinuous thin oxide layer could be detected. The presence of this interfacial layer explains the lowering of the barrier. In fact, according to Tung [7], if metal and semiconductor are separated by an interfacial oxide layer, the voltage drop across the barrier partly occurs in this layer and the effective Schottky barrier height is reduced.
On the other hand, when sample surface was prepared by RIE, XPS analysis showed an intense peak at a binding energy of 687.2 eV, which can be ascribed to the presence of fluorine [4]. A wide signal which appearing in the range 283.2-290 eV cannot be unambiguously attributed to single species, but it may be related to SiC covered by a carbonaceous surface layer. The amount of fluorine present on the surface, estimated from this analysis, was 25%. All these observations are consistent with the formation of fluorcarbon contaminations on the sample surface.
Moreover, AFM analysis showed that the sample surface has a high value of the surface roughness with RMS > 10 nm. Since almost no oxygen (i.e. residual oxide) could be monitor by XPS, fluorcarbon contamination, as well as the high interface roughness caused by RIE, must be responsible for the non-ideal behaviour of the diodes and for the high device on-resistance. In particular, the processing may induce interface states (originating from dry etching induced damage at the SiC surface), which determine the strong lowering of the barrier (0.87 eV). However, according to Bozack [8], high electron affinity impurities species at the interface (e.g. fluorine, in our case) may enhance a charge transfer from the semiconductor to the interface, thus increasing the semiconductor work function and reducing the average value of Φ_B [8]. In this way, the combined effect of damage and contaminants explain the strong reduction of the barrier height in the RIE etched samples.
Finally, the surface prepared with the combined procedure (wet + dry etch) does not show the presence of fluorcarbon contaminations, having a similar chemical composition and surface roughness like the NH_4F:HF wet etched surfaces. Therefore, a soft CF_4 plasma etch step following the wet etch results to be more suitable than removing the oxide only by simple NH_4F:HF etch.
Although after annealing at 600°C almost ideal diodes are formed, the curves reported in fig. 1b were chosen to be representative of the general trend. However, a significant spread in the distribution of ideality factor and barrier height values was observed in the characterization of a set of several diodes.
A further optimisation in the forward I-V characteristics of the devices could be observed after annealing at increasing temperatures up to 950°C, depending on the initial interface.
This effect can be clearly seen by the statistical distribution of n and Φ_B, extracted from the I-V characteristics of a set of 40 devices, shown in fig. 2 for the case of the devices formed with the combined wet + dry etch. The as deposited diodes have an average barrier height of 1.09 eV and ideality factor of 1.43. As can be seen, after thermal annealing at increasing temperatures a decrease of the ideality factor, accompanied by the increase of the average barrier height, occurs.
It is interesting to notice that the distribution of both barrier height and ideality factor become narrower at higher annealing temperatures up to 800°C. At this temperatures the average values of n and Φ_B were 1.10 and 1.35 eV, respectively. The decrease of the distribution width is an indication of the improvement in the Schottky barrier homogeneity.

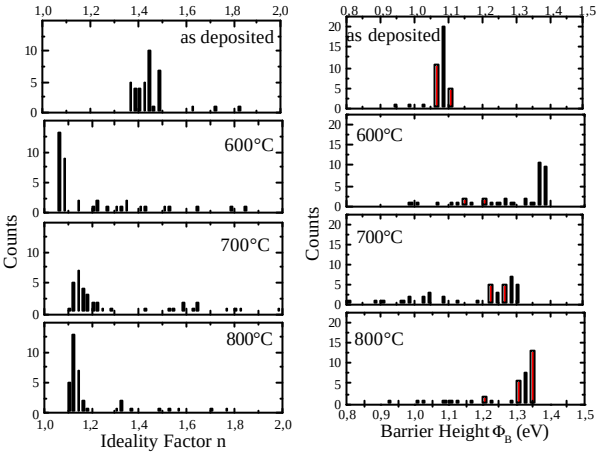

Figure 2: Distribution of the ideality factor n and of the Schottky barrier height Φ_B after different annealings up to 800°C

A complete explanation of the evolution of the improvement of the forward I-V characteristics of the diodes after annealing above 600°C was possible by investigating the formation of silicides induced by thermal reaction of Ni with SiC.
The XRD spectra of the Ni/SiC samples annealed in N_2 in the range 600-950°C are depicted in fig. 3. Thermal annealing at 600°C already results in the formation of polycrystalline nickel silicide (Ni_2Si), as can be deduced from the main peaks observed in the spectra, which are associated to diffraction from the planes (240), (203) and (133) of the phase Ni_2Si. The presence of the $Ni_{31}Si_{12}$ phase was also detected at 600°C. At high temperatures annealing up to 900°C only the Ni_2Si phase is present.
Therefore, the improvement of the barrier homogeneity can be explained by the formation of nickel silicide (Ni_2Si), which starts to form after annealing at 600°C by reaction of nickel with silicon carbide. At this temperature

and for short annealing time, however, the Ni_2Si phase still coexists with the $Ni_{31}Si_{12}$, which is the first phase forming in the reaction of the Ni-Si-C system because of its more negative hentalpy [9].

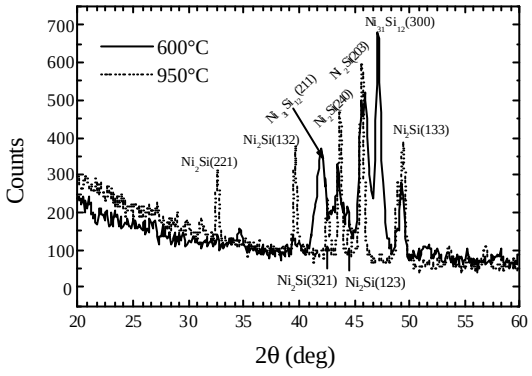

Figure 3: XRD spectra of Ni/SiC samples after annealing in N_2 at 600 and 950°C, showing the formation of nickel silicide phases.

As consequence of the presence of both $Ni_{31}Si_{12}$ and Ni_2Si at 600°C, a wide distribution of the Schottky barrier heights is observed. By increasing temperature all silicide transforms in the most stable Ni_2Si phase and this leads to a more uniform barrier, as can be observed from the narrowing of the distribution of Φ_B.

The electrical behaviour, however, may be also ascribed to the formation of a metal/SiC new interface after silicidation. In fact, when silicide forms, a silicon carbide layer is consumed by the solid state reaction, thus giving rise to a new interface, at a higher depth inside the material. The consumption of a SiC layer leads to the removal of surface damage, while residual oxide patches or plasma etch induced fluorcarbon contaminations are embedded in the silicide. Then, almost ideal I-V characterisitcs can be observed already after annealing at 600°C, i.e. the onset temperature for silicide formation. However, a further increase of the annealing temperature may be required to optimise the uniformity of the Schottky barrier and ideality factor, depending on the chemical composition and roughness of the initial Ni/SiC interface. As a matter of fact, the same trend shown in fig. 2 for the case of wet + dry etched devices, was also revealed independently of the surface preparation method, although slight differences in the optimisation temperature were observed. For example, the ideality was reached even in the case of plasma etched samples, which among all the preparation methods exhibited the worst I-V characteristics after Schottky metal deposition; in this case a higher thermal annealing temperature (950°C) was necessary to optimise the Schottky barrier ($n<1.1$, $\Phi_B=1.42$ eV).

5. Conclusions

In this paper, the dependence of the forward I-V characteristics of Ni/6H-SiC Schottky rectifiers on some surface preparation methods was presented. The results allowed to correlate the performance of the devices with the interface physical properties.

When carrying out the oxide wet etch in $HF:H_2O$, it was possible to obtain a nearly ideal behaviour of the diodes. The measured Schottky barrier height of Ni was 1.25 eV. Other surface pre-metallisation treatments only led to non ideal behaviour, and to a lower barrier. The latter was explained by the presence of a residual thin interfacial oxide layer or plasma induced fluorcarbon contamination. The contaminants left by plasma etch and the high surface roughness also determine the strong increase of the device on-resistance.

A sensible improvement of the forward I-V characteristic could be achieved by annealing the devices at 600°C in N_2. With this treatment, which lead to the formation of Ni_2Si, nearly ideal behaviour was achieved, with a barrier height approaching the value of 1.4 eV. Higher annealing temperatures led to a further improvement in the barrier homogeneity, as results from the narrower distribution of the measured values of n and Φ_B.

On the basis of all these results, the formation of nickel silicide (Ni_2Si), under appropriate annealing conditions, may represent the key to overcome the strong dependence of the device electric behaviour on the surface preparation and to achieve reproducibly nearly ideal diodes on SiC.

Moreover the higher SBH of Ni_2Si, makes it a good alternative to Ni for obtaining lower leakage current SiC Schottky rectifiers

6. References

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