Future Trends in Intelligent Interface Technologies for 42 V Battery Automotive Applications.

P. Moens, D. Bolognesi, L. Delobel, D. Villanueva, K. Reynders, A. Lowe, G. Van Herzeele and M. Tack
Alcatel Microelectronics, Westerring 15, B-9700 Oudenaarde, Belgium.
E-mail : peter.moens@mie.alcatel.be

B. Bakeroot
ELIS-TFCG St-Pietersnieuwstraat 41, B-9000 Gent, Belgium.

Abstract

This paper describes the emerging needs for future 42V battery automotive applications. To comply with these needs, a new modular 0.35 mm based smart power technology is introduced. The I3T80 technology contains various types of DMOS transistors in the range between 15 to 80V. A set of bipolars, a high voltage floating diode, a large array of passive components, floating logic up to 80V and 4kV HBM compatible ESD protection structures are available. In addition, embedded flash memory is offered. The extensive device library together with the robustness of the devices, makes it perfectly suitable for future 42V automotive applications.

1. Introduction

In the past few years, the number of electrical components installed in a car has been increased significantly. Today, the cost of the electrical systems in a midsize car is already more than the engine and transmission combined. To reduce the weight of the wiring, future automotive electronic systems will have to operate at a higher battery voltage (today, the wiring in a car is approximately 35 kg). After a series of workshops at MIT, it was proposed to change the battery voltage in the near future from 14V to 42V, taking into account economical and safety aspects [1,2]. However, although the typical battery voltage is 42V, the technology should be able to withstand much higher voltages. The maximum operating voltage for full lifetime (25y) is 50V. A maximum dynamic overvoltage of 8V (<1hour) is added, increasing the voltage requirement up to 58V. When a 12V charge pump for external drivers is required, these voltages shift to 62 and 70V respectively. Also an ESD protection window has to be foreseen, pinpointing the minimum voltage requirement at 80V. These voltage requirements are shown in Figure 1.

Besides the new battery voltage requirement, the average gate density is believed to increase from 5 k gates today to more than 30k gates in the near future, while also complex µcontrollers and a substantial amount of ROM/RAM is needed. Embedded memories are required in the range from 32-256Kbytes with endurance capability of up to 10^5 write-erase cycles and retention times in excess of 10years. As a result, these smart-power System-on-Chip (SoC) applications require a further downscaling of the technology feature size.

A third important requirement for automotive applications is robustness. Operating temperatures can range from -40°C up to 150°C under hood. Also for ESD, a minimum of 4 kV HBM is required. Latchup immunity, parasitic substrate effects and protection against Schaffner pulses has to be checked carefully. Besides the standard Hot Carrier degradation tests (lifetime is required up to 25 years !), additional tests assessing the ability of the drivers to switch large currents (Clamped and Unclamped Inductive Switching, Energy Capability measurement, …), are to be performed.

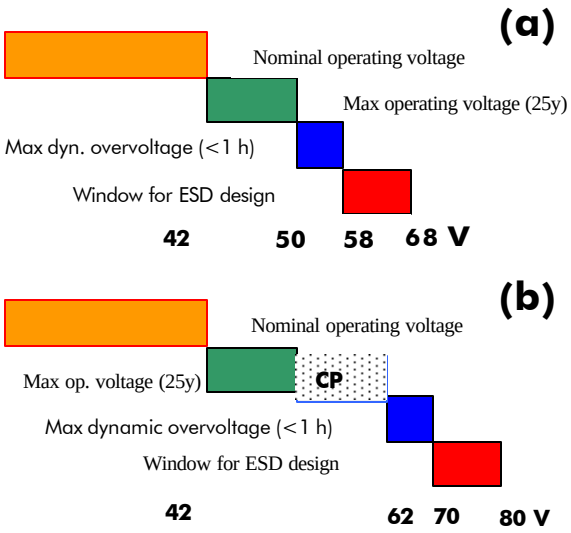

Figure 1. Voltage requirements for the 42V automotive system design, without (a) and including (b) a charge pump for external drivers.

This paper describes a 80V modular smart power technology based on a 0.35 µm CMOS core, called I3T80. To our knowledge, this technology is the first to combine the features of 80V capability with a 0.35 µm CMOS logic. Competitors either use a 0.35 µm compatible process flow, but are limited to lower voltages (e.g. [3,4]), or are in the same voltage range but use a larger critical dimension ([5,6]) and use multi-chip solutions. Figure 2 shows the roadmap and application areas from the cheap 2.4 µm HBIMOS technology towards the much more complex 0.35 µm QLM I3T80 technology.

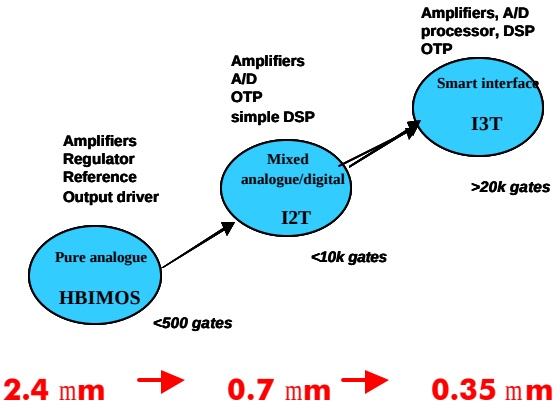

Figure 2. Application areas for different intelligent interface technologies

2. Technology description.

The I3T80 technology is developed in a modular way. For the basic 80V devices, a minimum of only five masks is added to the standard process flow (N/P buried layers, N/P sinker, Pdrift). A lightly doped n-epi is used: its thickness and doping profile are tuned for optimal tradeoff between vertical and lateral devices. Moreover, the n-epi ensures a good contact with the n-type buried layer, which is mandatory for the vertical devices (VDMOS, NPN bipolar devices, high voltage floating diode, ESD protection structures). The N and P sinkers are used to contact the N and P buried layers respectively, and are indispensable for the vertical devices and the electrical isolation. As the technology is mainly targeted towards the automotive market, the layer optimisation is done for the vertical devices, hence making the technology much more robust. A vertical current flow is desired in order to improve heat sinking and to avoid oxide degradation by carrier trapping at the surface.

The Pdrift layer is used for the junction termination and pDMOS structures. Its dose and implantation energy are optimised such that the layer is fully depleted at 80V. In this way, a high performing resurf lateral pDMOS is made. All devices have the standard 0.35 µm 7 nm gate oxide, limiting the maximum gate voltage to 3.3V. The channels of the basic nDMOS and pDMOS devices are made with the standard C035 Pwell and Nwell respectively.

The CMOS devices are not altered by the additional I3T80 processing. Hence, all standard C035 libraries can still be used. Besides the standard logic, floating logic up to 80V is also available.

In addition to the standard I3T80 process flow, a Pbody implant module can be added. By using a LATID implant [7], the channel of the nDMOS devices is made self-aligned to the poly. Also an embedded flash memory is optional, at the expense of 3 extra masks (HIMOS™ [8]). One time programmable circuit blocks are also available at no extra cost based on zapping Si bulk diodes. A Power metal can be added.

Figure 3 shows a SEM cross-section of an ESD protection structure, with the isolation ring. All layers are clearly indicated and visible.

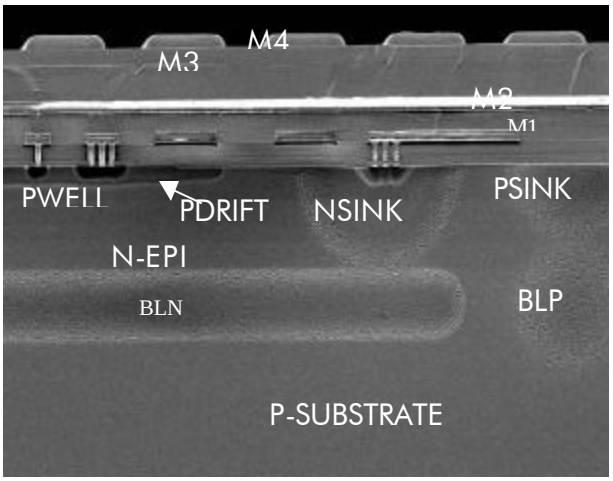

Figure 3. SEM cross-section of (part of) an ESD protection structure in I3T80 + isolation

3. Results and Discussion

In automotive applications a lot of big drivers are needed. Examples are e.g. motor and power supply drivers, relays, power regulator, lamp drivers etc. In such cases, the drivers can occupy between 30 up to 70 (!) % of the total chip area. For sensor interfacing, the driver area is less, but can still range from 10 to 30 %. As drivers are made of DMOS devices, the I3T80 technology is mainly targeted towards optimum and robust DMOS drivers. Besides n and p-type DMOS, the technology also features bipolar devices (NPN and PNP), a High Voltage floating diode, a large array of passive components (resistors, inductors and capacitors), and HV floating logic. As the technology will also be used for consumer electronics (e.g. peripherals), also DMOS devices optimised for lower voltages (60V) are present. Table 1 gives an overview of the main device parameters of all the above-mentioned components.

Table 1. Electrical Characteristics of the most important devices in I3T80

Device	Channel	Vt (V)	βlin µA/V²	Ron mΩ*mm²	Vbd (V)
VND80	Pwell	0.57	70.2	165	89
	Pbody	0.71	102	155	84
FND80	Pwell	0.58	82.9	219	83
	Pbody	0.70	98	183	84
FND60	Pwell	0.58	42.1	135	62
	Pbody	0.70	110	100	65
FND25	Pwell	0.60	114	56	28
FND15	Pwell	0.60	125	36	17
PD80	Nwell	-0.54	38.8	308	-94
PD60	Nwell	-0.54	31.7	250	-61

Device	Beta	Bvceo (V)	Bvces (V)	Vearly Ib=15µA	Rcol (Ω)
V-NPN	58	31	71	-520	900
S_PNP	6.8	-65	-75	400	531

Diodes	
HV floating diode	Vbd > 80 V, Isub < 1 %
Bulk Zener Diode	Vz=4.5V, Rseries < 50Ω
LV Clamping Diode	Vrev=9 V

Passives	
Diffused resistors	Rsheet from 20 to 10k Ω/[]
Poly resistors	Rsheet from 300 to 1000 Ω/[]
Metal 1,2,3,4,5 resistor	Rsheet from 0.03 to 0.08Ω/[]
Power metal resistor	Rsheet=0.015 Ω/[]
BLN resistor	Rsheet=12 Ω/[]
Capacitors	C from 90 to 800 pF/µm²
MiMC	C=1.5 fF/µm² , Vbd < 30V

The specific on-resistance (Ron) for all devices is determined at Vgs=3.3V and Vds=0.5V. No parasitic bipolar turn-on is observed, up to the maximum Vds and Vgs (Vds=15, 25, 60 or 80V, depending on the device).

Two types of 80V nDMOS transistors are available : a vertical DMOS, using the Nsinker and BLN as the drain, and a lateral nDMOS. The Ron for the VDMOS, as specified in Table1 takes into account the overhead for the drain. As the buried layer resistance is very low, up to 8 gate stripes can be put in between two drains. As such, the drain overhead is only 12%, making integration of vertical devices very interesting. Figure 4 shows variation of the specific Ron of the VDMOS as a function of the number of gate stripes for two different BLN resistivities. The lateral device uses a field oxide in the drift region. The field oxide length is tuned such that the breakdown voltage reaches 80 V.

The 15, 25 and 60V nDMOS devices are lateral devices. The breakdown voltage is scaled using layout modifications (field oxide length and poly overlap on field oxide are tuned). The 60V and 80V devices are isolated by a BLN and are floating up to 90V. Hence, they can be used for high-side drivers. The 15 and 25V nDMOS devices do not have a buried layer, and have a Nwell in the drift region. These devices are mainly used in the OTP circuits.

The pDMOS devices are lateral devices, and use the resurf effect to increase their performance. An optimisation of the pdrift implantation led to optimum resurf devices. Their electrical performance is also given in Table 1.

Extensive hot carrier reliability tests are performed on the n and pDMOS devices in order to determine their Safe Operating Area (SOA) : 80V components should have full lifetime (i.e. 25y) up to Vds=62V for applications using the charge pump, see Figure 1. All devices are "true rated devices" i.e. they have full lifetime up to 62V for the 80V components and up to 40 V for the 60V devices. Typical degradation curves for the worst parameter (Ron) are shown in Figure 5 for the 80V VDMOS, LnDMOS and LpDMOS. The devices are stressed at Vds=70V and Vgs at I_{bsmax} (nDMOS) or I_{gsmax} (pDMOS).

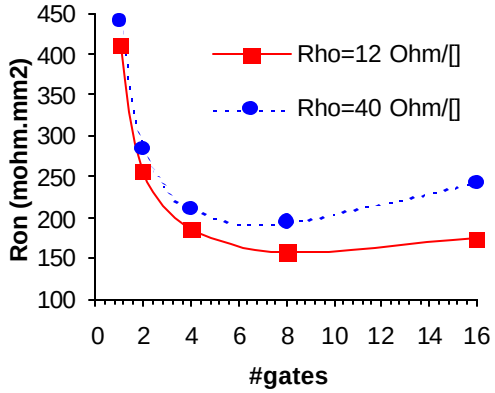

Figure 4 : Total specific on-resistance of a VDMOS as a function of the number of gate stripes for two different BLN resistivities.

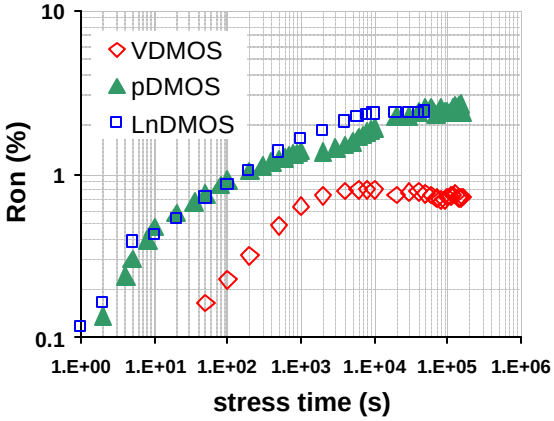

Figure 5 : Hot Carrier degradation of Ron of the 80V VDMOS, LnDMOS and pDMOS. Devices are stressed at Vds=70V and for the worst case Vgs.

As can be noticed from Figure 5, the degradation of the devices is very slow. The degradation saturates for the lateral devices, and even seems to decrease again for the vertical device. The vertical DMOS has a lower degradation compared to the lateral devices, as expected.

The performance of the I3T80 nDMOS devices is compared with literature data in Figure 6. Although the technology is mainly developed for robustness (vertical devices, good hot carrier performance, …) the Ron versus Vbd is competitive.

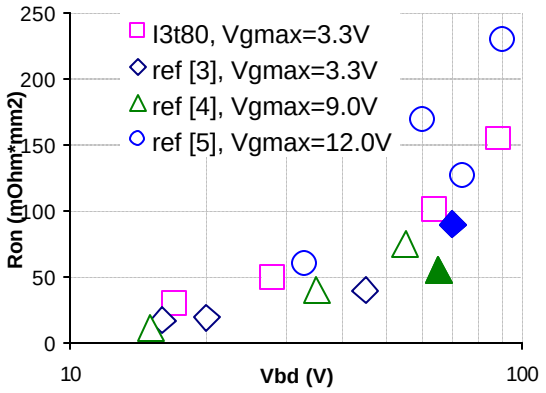

Figure 6 : Benchmarking of I3T80 against competition. The devices indicated in bold have no buried layer (can only be used in low-side switches). Refs [4,5] use a dual gate approach (thicker DMOS gate oxide).

TLP measurements (100ns current pulses) are also performed on 80V devices in order to study the robustness of the components and to assess their self-protecting capabilities. In particular the 80V VDMOS is very robust against ESD: a small driver with an effective W=80 µm is already self protecting against 4kV HBM. The lateral devices are destroyed as soon as they go into snapback.

For the High Voltage lateral DMOS devices bipolar-like ESD protection structures, with triggering voltages ranging from 50 to 80V, are developed. Trigger and holding voltage (for supply protection) can be tuned separately towards the desired voltage. All bipolar protection structures have current capabilities in excess of 20 mA/µm. No leakage current increase is observed for currents up to almost 6 A ! All structures are developed to pass 4 kV HBM, and scalability rules up to 8 kV HBM are provided.

For Low Voltage applications (OTP, EEPROM, 15 and 25V DMOS), special Grounded Gate NMOS structures and SCR devices are used.

Embedded flash in I3T80 is based on the HIMOS™ cell [8]. This is an n-channel split gate device incorporating a control gate in series with and a program gate on top of the floating gate channel. Dimensions are tuned to provide sufficient coupling of the program gate voltage to the floating gate, leading to a cell size of 3.8µm^2. Processing of the memory cell requires only 3 extra masks in contrast to embedded memory solutions derived from stand-alone memory processes where typically 7-9 extra masks are required. The programming mechanism is source side injection, which gives effective programming in approx. 10µsec at moderate voltages. Erasure is via Fowler-Nordheim tunnelling between the floating gate and drain, taking approximately 0.5secs.

Full operation of the embedded memory requires voltage levels from −6 to +9V, which can be handled by means of extended drain NMOS and PMOS devices. These are available in the standard I3T80 process flow.

4. Conclusions

I3T80 is presented as the first next generation intelligent interface technology, compatible with the 42V battery automotive market needs. This technology provides 80V smart-power devices integrated into a dense 0.35 µm technology. The large device library together with the robustness of the devices, makes it perfectly suitable for future 42V automotive applications. The optimisation of MV devices leads als o to cost effective use for less demanding applications, like peripheral and battery management chips.

5. Acknowledgments

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6. References

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