The Advanced RESURF Structure to Improve On-Resistance in BCDMOS

C.J. Kim, Y.C. Choi, S.K. Lee, T.H. Kwon, H.S. Kang and C.S. Song
Fairchild Semiconductor, Process Development Group
82-3, Dodang-Dong, Wonmi-Ku, Puchon, Kyunggi-Do, Korea
E-mail : kcj782@fairchildsemi.co.kr

Abstract

In this paper, We report the novel RESURF structure of LDMOS TR with the p-bottom layer to improve On-Resistance. The developed LDMOS achieved the low 0n-resistance, which is improved by 25% compared to conventional structure LDMOS TR. In addition to this result, This LDMOS had the good reliability because the high field point moves surface to bulk and showed the excellent safe operating area compared to conventional structure. Technique and issues related to this transistor are concerned and discussed

1. Introduction

Until comparatively lately, in most of power analog IC applications, LDMOS transistor has replaced the bipolar transistor because of its advantages, such as good reliability, low power dissipation and high switching speed [1].

Many studies on LDMOS transistor have been conducted and especially, concern of on-resistance has been increased. For a typical high voltage LDMOS transistor, it is difficult to get a low on-resistance as a parameter of the most important characteristics of LDMOS transistor. It is well known that on-resistance depends on the resistance of channel and drain. Typically, in high voltage LDMOS transistor, drain resistance is more dominant than channel resistance. In order to reduce the on-resistance of LDMOS transistor, it is necessary to reduce the drain resistance. The drain region of 2. The drain region of conventional LDMOS is normally formed by n-well and therefore we need to increase the concentration of n-well to reduce the drain resistance. However, n-well resistance is limited by the breakdown voltage between source and drain. This paper describes the method for increasing the n-well concentration without the decrease of breakdown voltage between source and drain by using RESURF layer, so called p-bottom. discussed

2. Process and Device simulation

Fig.1(a) shows schematic cross section in the proposed LDMOS and Fig.1(b) shows the one in the conventional LDMOS. The proposed LDMOS is built on a n-epi on p-substrate layer considering compatibility with BiCMOS process. The thickness and resistivity of the n-epi in the proposed LDMOS structure are typically suitable for a 0.8μm BCDMOS process. The n-well forms the region of drift and drain. In the proposed LDMOS p-bottom layer is formed on the n-buried layer and used for RESURF action. The p-bottom layer also serves as a bottom layer of the isolation for other devices. So, the proposed LDMOS has been achieved with no additional thermal budget or mask layer compare to conventional one. The junction depth of n-buried layer has to be deep enough so that it can prevent the parasitic bipolar PNP action formed by p-bottom, n- buried layer and p-substrate. The profiles of p-bottom and b-buried layer have to be controlled carefully because they affect breakdown voltage and parasitic bipolar PNP gain directly.

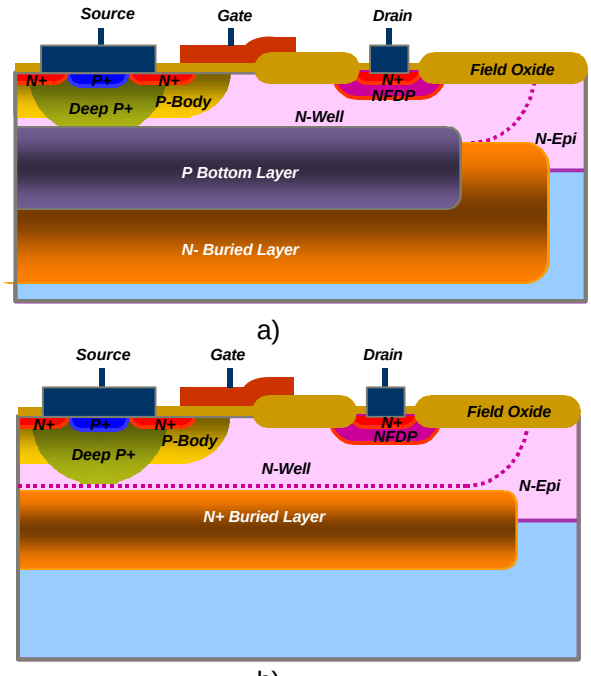
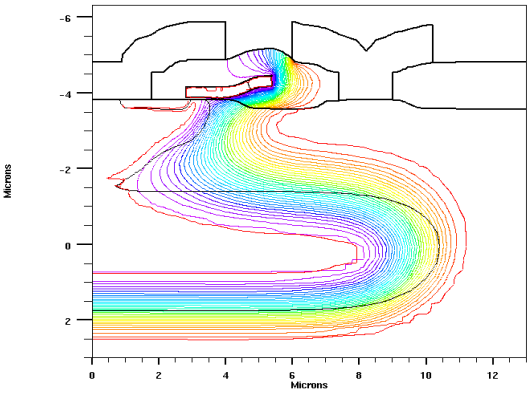


Fig. 1 Schematic Cross-section of the (a) New Structure (b) conventional structure of LDMOS Transistors

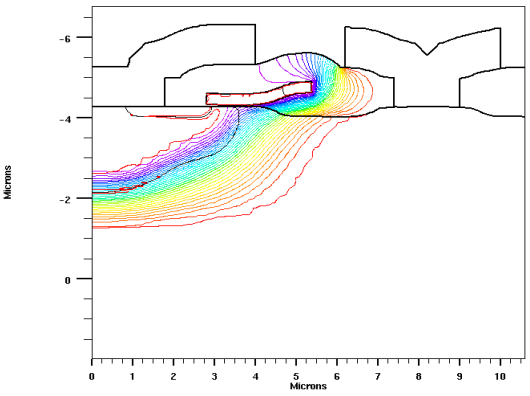
3. Simulation Result and Discussion

3.1. Device performance

Fig1.(a) shows the schematic cross section of the proposed RESURF LDMOS. In the structure, the RESURF n-well and p-bottom layers can be more easily depleted to near drain contact region than in the case of the only n-well layer of the conventional LDMOS shown in Fig.1(b) when the reverse bias was applied to the drain [2]. As a result potential drop is uniformly distributed between source and drain. Fig.2(a) shows the potential contour line of proposed LDMOS and Fig.2(b) shows one of conventional LDMOS [3].



(a)



(b)

Fig. 2 Potential Contour Line of (a)New Resurf LDMOS (b) Conventional LDMOS at Breakdown

In conventional high voltage LDMOS, getting breakdown voltage above 40V need to decrease the n-well concentration significantly. When the n-well concentration is high, the depletion region cannot be extended enough to drain and the peak field point is formed in surface under LOCOS. As a result, getting higher breakdown voltage above 40V requires the decreasing in n-well dose, which results in increasing the device on-resistance.

However, for a proposed RESURF LDMOS, the RESURF action by p-bottom layer and n-well layer delays forming peak field on surface under LOCOS. Thus the proposed LDMOS has higher BVdss value than the conventional one when the n-well concentration of those devices is similar to each other. The n-well concentration in the proposed LDMOS can be remarkably increased even though the proposed device is almost the same as the BVdss of the conventional device. Therefore the proposed LDMOS guarantees lower on-resistance. With higher doping concentration of n-well and RESURF action of p-bottom, the proposed LDMOS can be improved by 25%.

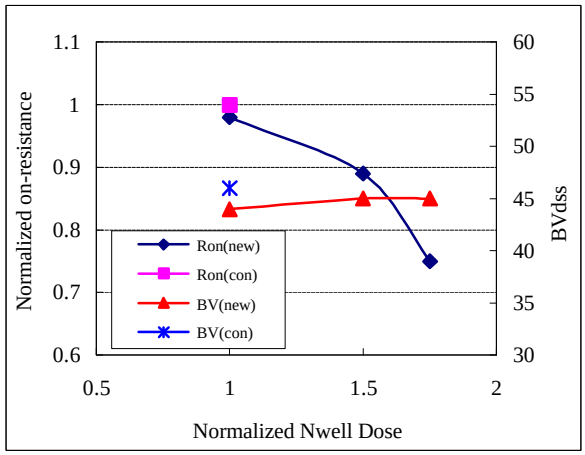


Fig. 3 Simulated BVdss and on-resistance as a Function of Normalized n-well Dose.

In the newly proposed structure, the concentrations of p-bottom and n-buried layer are very important. The breakdown of proposed LDMOS occurs at junction between p-bottom and n-buried layer. When the breakdown of high voltage device occurs near surface, the device may have a problem that it doesn't recover after breakdown. However, with bulk breakdown, the proposed device can solve the unfavorable shows good reliability. Thus, the bulk breakdown was intentionally induced even though we can obtain higher breakdown voltage when it occurs on surface. In proposed device, the concentrations of b-bottom and n-buried layer have to be controlled adequately. If it is not balanced, the high field point moves to surface and the breakdown occurs near surface. As a result, we obtain the good RESURF effect and bulk breakdown when the charge balance of p-bottom and n-buried layer is well controlled

Table1 Simulated Breakdown Voltage as a Function of Normalized NBL and PBTM Dose.

NBL dose	PBTM dose	BV(V)	Point
1.0	1.0	50	Surface
1.0	1.2	46	Bulk
1.0	1.4	44	Bulk

The difference of RESURF effect with distance of p-bottom to drain is indicated by variation of breakdown shown in Fig.4. As the p-bottom layer is overlapped enough under the drain, the breakdown voltage is the highest because the depletion region can be extended to n-well region under drain by p-bottom and the forming peak field on near surface is delayed.

However, when the overlap is above –3μm, the breakdown voltage is saturated. Fig.6 shows the potential contour lines when the distances of p-bottom to drain are 3μm and -5μm respectively..

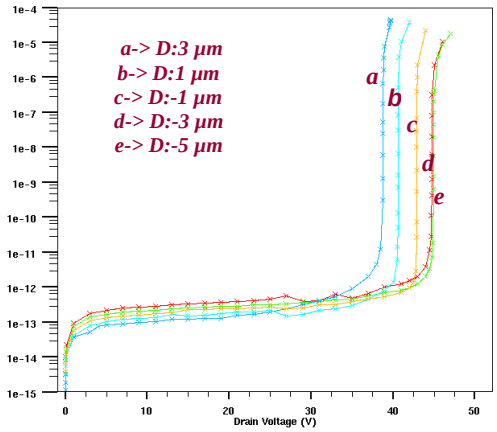
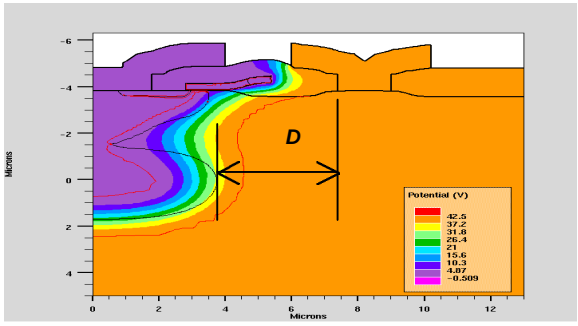
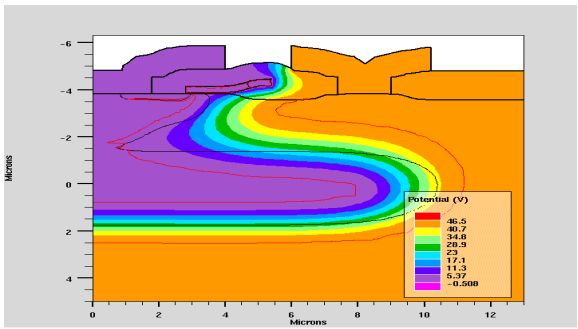


Fig.4 Simulated Breakdown Voltage of New LDMOS Transistor.



(a) P-bottom <-> Drain : 1μm



(b) P-bottom <-> Drain : -5μm

Fig.5 Potential Contour Line of New LDMOS With distance of P-bottom and Drain

3.2. Parasitic PNP Operation

The proposed LDMOS has higher possibility of parasitic PNP operation than conventional LDMOS because the concentration of n-buried layer which is the base of parasitic PNP is lower than conventional one. This parasitic PNP operation restricts the use of proposed LDMOS in some applications. So, the suppression is very important. The parasitic action of proposed LDMOS can be suppressed by controlling the concentration and junction depth of n-buried layer.

3.3. Safe Operating Area

The safe operating area of the proposed LDMOS is very good due to high doping concentration of n-well. The highly doped n-well makes the new LDMOS have good current driving ability and delay the Kirk effect while high bias is applied to drain. Fig.6 shows the output characteristics of new LDMOS and conventional one.

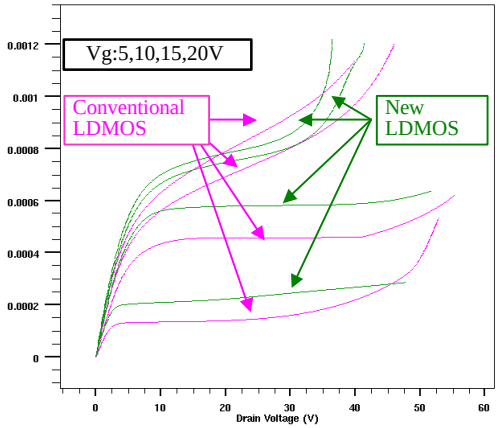


Fig.6 Simulated output characteristics of LDMOS

4. Conclusion

The newly proposed LDMOS can have highly doped n-well as a drain by RESURF effect of p-bottom layer. Therefore, it has low on-resistance, which is improved by 25% in 45V, 0.8μm smart power technology without additional process steps is proposed. This device also has better SOA than conventional one and it is relatively insensitive to process variations because the breakdown of it occurs in bulk junction

5. References

[1] B.JAYANT BALIGA, “Modern Power Devices” 1987, pp.263.

[2] A.W.Ludikhuize,“Performance and Innovative Trends in RESURF Technology”, Proc. of ESSDERC’01, pp.35.

[3] SILVACO ATLAS, “Device simulation software,” *User’s manual*, 1998.