On the High Temperature Operation of High Voltage Power Devices

Vasile V.N. Obreja
National R&D Institute for Microtechnology (IMT), P.O. Box 38-160, Bucharest, Romania
Tel: +401-490-8212, Fax: +401-490-8238,
E-mail:vasileo@imt.ro,vnobreja@hotmail.com

Keith I. Nuttall
Department of Electrical Engineering and Electronics, The University of Liverpool, L693BX, Liverpool, UK, Tel: 0151 –794-4508
E-mail: ee16@liverpool.ac.uk

Abstract

The surface component of reverse current is a serious limitation for the operation of high voltage/current devices at high junction temperature. This component may induce reverse current-voltage instability of a PN junction followed by device failure during high temperature operation. Experimental results are presented for silicon rectifier diodes revealing the influence of the junction surface leakage current on the reverse I-V characteristics. Known results for silicon carbide PIN diodes are considered for comparison. Available PN junction passivation methods at this time are not effective enough in controlling the junction surface leakage current.

Improved surface passivation techniques are required to achieve reliable device operation, especially above 200 ^oC.

1. Introduction

Silicon high voltage bipolar or MOS devices cannot operate reliably at junction temperature higher than 175 – 200 ^oC. Although high temperature performance is expected from SiC, commercial devices with a permissible junction operation temperature above 200 ^oC are still not available. The first Schottky barrier diodes with a rated current from 1A to 10A and blocking voltage rated from 300 V to 600 V which appeared on the market in 2001 have a maximum junction operation temperature limited to 175 ^oC. SiC based PIN diodes have been demonstrated with a reverse voltage up to 6.2 kV, [1-2], but are still not available as commercial devices. As reported in [2] surface phenomena from the junction peripheral surface may govern the diode behavior at reverse bias voltage and low forward voltage.

Even though silicon device technology has a very mature status, the reverse I-V characteristics of silicon power PN junctions may still be controlled by surface effects, [3-4]. PN junctions are vital building cells of modern bipolar or MOS semiconductor devices. Power devices whose PN junction passivation is based on Si-SiO_2 interface manifest reverse current-voltage instability which may be followed by failure at elevated temperature sometimes even before 200 ^oC, [5]. Analysis of defective devices after operation at high junction temperature, T_j, has revealed electrical short-circuits accompanied by crystalline lattice damage at the junction peripheral surface.

The purpose of this work is to show that electrical phenomena at the junction peripheral surface are still a significant factor that is preventing the full potential of silicon devices operated at junction temperatures above 200 ^oC from being realized.

2. Experimental results. Discussion

Typical results that reveal the influence of junction surface effects on the reverse I-V characteristics are shown in Fig.1. This data relates to a mesa type silicon P^+NN^+ structure of about 16mm^2 area and passivated with organic dielectric (silicone rubber). This passivation method has the advantage that for the same structure, the passivation dielectric layer can be easily removed and the passivation process repeated.

Planar oxide and glass passivated junctions of about the same area and breakdown reverse voltage as those considered in Fig.1 have also been investigated. For some of them the passivating oxide was removed and a re-passivation by using organic dielectric was performed. It has been found that the state of the silicon junction surface in direct contact with the dielectric layer is of great significance for I-V reverse characteristic stability at T_j higher than 200 ^oC whilst the nature of the dielectric passivation material (organic or inorganic) is of less importance. The results in Fig.1 also show a significant reduction in the value of reverse current, I_R, takes place after heat treatment at 300 ^oC and that since the same behavior is repeated with the second passivation and anneal cycle, then this must be attributed to a reduction in surface related current. Fig.1 also shows that a low level of I_R near room temperature does not necessarily provide a low I_R at high T_j. Further experiments taking into account a correlation of the I_R level with the junction area and its perimeter have indicated that the I-V characteristics in Fig.1 after heat treatment at 300 ^oC are still influenced by the surface component.

Investigated glass or oxide passivated junctions of available commercial devices with a silicon die of about

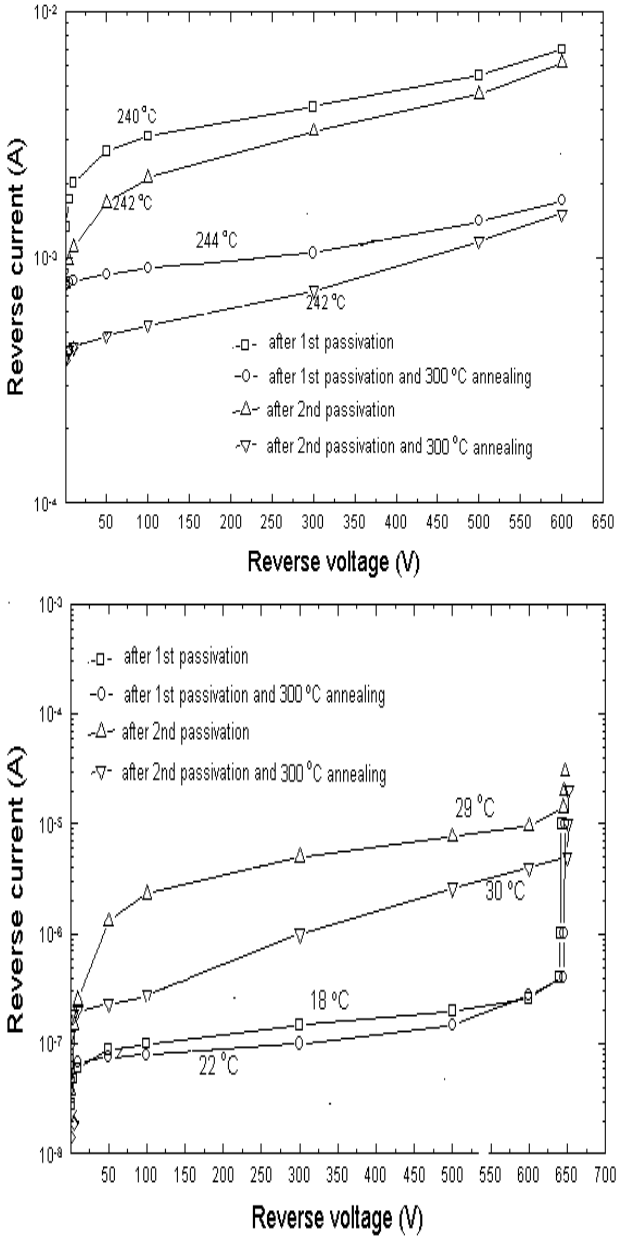

Figure 1. Current–voltage characteristics for a silicon controlled-avalanche diode structure with organic dielectric passivation near room temperature and above 200°C junction temperature

the same dimensions, breakdown voltage and charge carriers lifetime as that used in Fig. 1, exhibited I_R values above 200 °C not less than the lowest level shown in this figure. Consequently, the I_R level of junctions passivated with inorganic dielectric is not necessarily less than those passivated with organic dielectric and may be also controlled by surface phenomena.

Other examples that demonstrate the influence of the surface component on the level of I_R are shown in Fig.2. This time a mesa P^+NN^+ rectifier silicon structure of 16 mm^2 area but with an expected bulk breakdown voltage higher than 1500 V has been used and the graphs have been drawn with logarithmic voltage scales. The different I-V reverse characteristics shown correspond to three different re-passivations of the same silicon structure. The characteristics plotted after the 1st passivation relate to the situation when some contamination from the surrounding manufacturing ambience was permitted after the cleaning of the junction surface. Reverse characteristics for the 2nd and the 3rd re-passivations relate to a passivation process that was completed without allowing any influence from the surrounding manufacturing ambience. Nonetheless, some acid traces remained after the junction surface cleaning during the passivation process, more for the 2nd and less for the the 3rd re-passivation**.**

Fig. 2 shows that the surface component of I_R has a significant influence not only on its level at room temperature and above, but also on the obtained breakdown voltage value. This time, significant voltage dependence of I_R (soft surface breakdown characteristic) is evident at room temperature well below the expected value of the bulk breakdown. At higher junction temperature the curvature of the characteristic towards 1000 V is significantly attenuated. As in the case of Fig.1 a reduced voltage dependence of I_R at room temperature observed in Fig.2 (which may be favorable in reaching the bulk breakdown value determined at low current), does not provide low I_R values at high T_j. In practice it is known that for higher reverse working voltages, above 1000 V, it is more difficult to reach the bulk breakdown voltage. Silicon controlled-avalanche diodes of breakdown voltage above 2000 – 3000 V are not easily realized.

While the level of reverse current at high junction temperature for the 1st passivation in Fig.2 is comparable with the corresponding one for similar commercial silicon diodes available on the market, for the other two passivation situations the level of leakage current is significant lower. It has also been found that the blocking I-V characteristic of the drain junction of some investigated high voltage commercial power MOS devices of about the same area as the diode structure used in Fig.2, do not exhibit lower I_R values at high T_j than it is shown in this figure. A saturation tendency of I_R at lower V_R and high T_j observed in Fig.2 for the 1st and 3rd passivations cannot be considered evidence for the bulk diffusion component dominance because even lower I_R values are obtained for the 2nd passivation case where visible voltage dependence is manifested. Consequently, in spite of significantly reduced I_R values at high T_j obtained in Fig.2 its level continues to be under the influence of the surface component. Nonetheless, excessive high surface leakage current is prevented for the 2nd and 3rd passivation case.

High temperature reverse bias (HTRB) tests at 250 °C and 300 V for 250 hours have indicated good stability of the devices passivated in the same conditions as for the 2nd or the 3rd re-passivation cycle but no device from the first passivation cycle survived. These devices exhibited a relatively high initial I_R level at 250 °C and

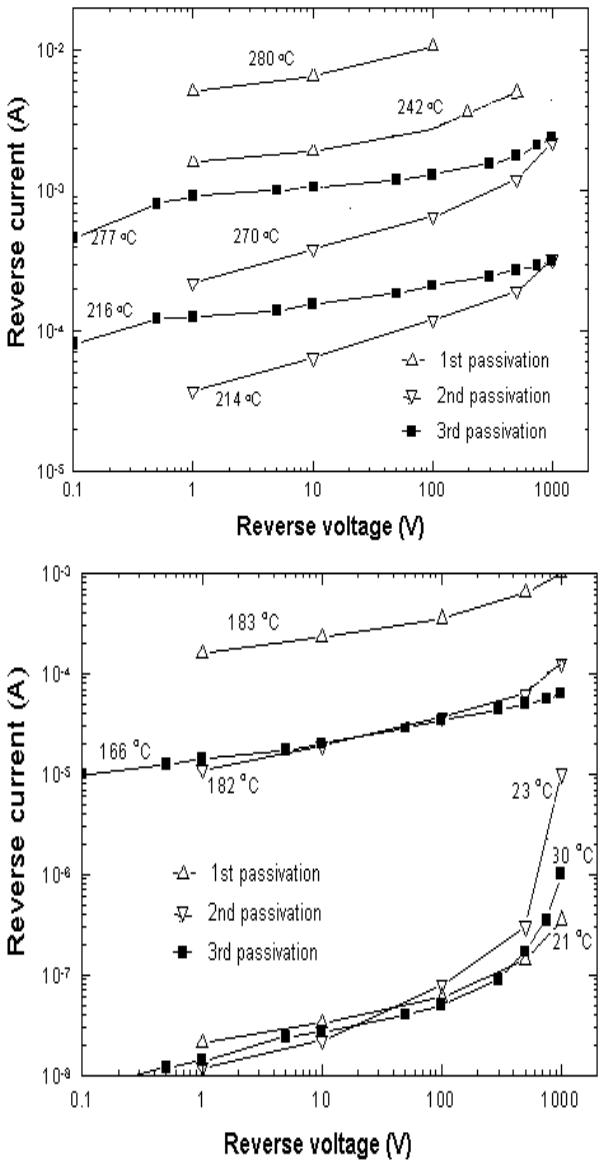

Figure 2. Electrical characteristics of a silicon high voltage rectifier diode passivated with organic dielectric; **1st passivation:** permitted exposure of the junction peripheral surface to the surrounding manufacturing ambience; **2nd and 3rd passivations:** without exposure to the ambient but with acid traces, more for the second and less for the third.

300 V of 6 – 8 mA. After the test, electrical short-circuits were found, caused by local current conducting at the junction peripheral surface. Devices from the 2nd and 3rd passivation cycle that were subjected to HTRB tests had a reverse current level of 0.5 – 0.7 mA at 250 °C and 300 V prior to the test. After the tests no significant change in the level of I_R was found. It is likely that local overheating takes place at the junction peripheral surface due to excessive local power dissipation, particularly if it is considered that the surface current is unlikely to be uniformly distributed around the junction perimeter.

As a consequence, reliable operation of silicon high voltage diodes at junction temperature above 200 °C is only possible when the surface component of the reverse current is kept at a low level by a suitable junction passivation process. Suitably chosen organic dielectrics for junction passivation may be more efficient at high temperatures than the presently used inorganic dielectrics.

The experimental results presented in this work were taken on high carrier lifetime PN junctions i.e. the density of bulk generation –recombination centers is low. However, for silicon fast recovery PN junctions the bulk component of I_R may become the primary component at T_j higher than 125 – 150 °C, [4]. Nevertheless even in this case, the surface component can still be a cause for reverse I-V characteristic degradation at elevated temperature.

To our knowledge PIN diodes based on SiC and with an area larger than 10 mm^2 are still not available even as demonstration devices. However, a significantly lower level of I_R for SiC based devices is expected because the carrier intrinsic concentration for this material is orders of magnitude lower than for silicon. Nevertheless it has already been observed in the literature that the experimental values for I_R are orders of magnitude higher than predicted. Near room temperature, I-V reverse electrical characteristics of similar shape and visible voltage dependence of I_R as shown in Fig.2 have been reported. At high T_j the same saturation tendency is observed. High excessive I_R is possible for a SiC PIN diode in comparison with another diode from the same wafer and with the same physical parameters. Published experimental reverse voltage characteristics for 4H-SiC or 6H-SiC diodes are often limited to less than 250 °C and voltages significantly lower than those given for the room temperature, [1,2]. Furthermore, the practice of expressing PN junction reverse leakage as a current density (A/cm^2) can be misleading in the presence of a significant contribution from surface current.

Evidently, high temperature surface passivation is an issue that will need to be addressed to successfully realize the full potential not only of silicon, but of SiC as well.

3. PN junction physical model

The experimental results presented in Figs.1-2 can be understood by taking into account surface electrical phenomena of the types shown in Fig.3. Either a surface inversion, depletion or accumulation layer may cause surface leakage current at reverse bias voltage. The surface current component is dependent on the carrier intrinsic concentration. Consequently, for silicon based junctions a significant higher level of I_R is expected than for semiconductors with higher band gap energy.

Besides the bulk component of I_R uniformly distributed over the junction area, the surface component may be non-uniformly distributed over the junction perimeter so that reverse current crowding may be favored in some

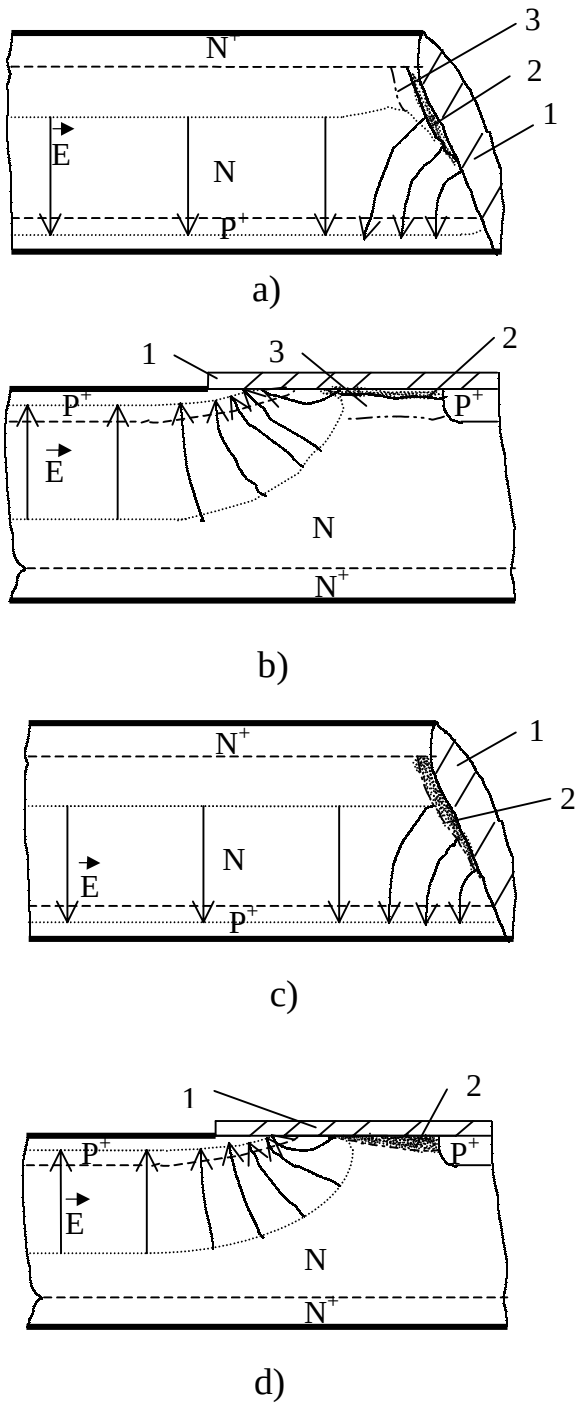

Figure 3. Surface space charge layers in silicon PN junctions under reverse bias voltage;
inversion and depletion layer in mesa (a) and planar (b) PN junction;
accumulation layer in mesa (c) and planar (d) PN junction;
1- passivation dielectric layer; 2- inversion or accumulation layer; 3- depletion layer;

local regions. Ideally, the junction passivation process would prevent a surface space charge layer forming to assure device ability for operation at T_j higher than 200 ^oC. In practice a surface depletion or inversion layer may be responsible for excessive high I_R at high T_j – such as in the case in Fig.1 before annealing or in Fig.2 (1^{st} passivation) whilst a charge accumulation layer can reduce the surface leakage current. This may account for the behaviour observed in Fig.1 & 2. With a decrease in the doping concentration of the starting silicon material necessary to obtain high working voltages, the formation of a surface space charge layer at the semiconductor surface is more difficult to control. Control difficulties may be also encountered for SiC due to a significant lower intrinsic concentration. More influence on the level of I_R at high T_j or on the obtained breakdown voltage value is expected. A weak accumulation layer obtained by suitable junction passivation could be acceptable for high junction temperature operation providing low level of I_R from low to high reverse voltage. The annealing process and silicon surface treatment with acid traces whilst avoiding contamination from the surrounding ambient are thought to be instrumental in creating these conditions.

4. Conclusion

The results presented indicate that high temperature operation of silicon power devices may be still affected by a significant surface leakage current component. Presently available junction passivation based on the Si-SiO_2 interface does not appear to provide an adequate control of leakage current needed to fully realize the potential of silicon at temperatures above 200 ^oC. This is an issue that will be particularly relevant to the successful introduction of SiC devices.

5. References

[1] K. Fujihira, S. Tamura, T. Kimoto, and H..Matsunami , "Low-Loss, High-Voltage 6H-SiC Epitaxial p-i-n Diode", *IEEE Transactions on Electron Devices,vol.49, No.1, 2002,* pp.150 –154

[2] T. Kimoto, N. Miyamoto, and H. Matsunami, "Performance Limiting Surface Defects in SiC Epitaxial p-n Junction Diodes", *IEEE Transactions on Electron Devices, vol.46, No.3,1999, pp.471 - 477*

[3] V. Obreja, "On the Leakage Current of Present-Day Manufactured Semiconductor Junctions", *Solid–State Electronics*, vol.44, No.1, .2000, p. 49-57

[4] V. Obreja , " An experimental investigation on the nature of reverse current of power silicon PN junctions" *IEEE Transactions on Electron Devices, vol.49, No.1, 2002, pp.155 – 163*

[5] J.R. Trost, R.S. Ridley, M. Kamal Khan and T.Grebs, "The effect of charge in junction termination extention passivation dielectrics", *Proc.11th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1999, pp.189-192