A Low On-Resistance 700V Charge Balanced LDMOS with Intersected WELL Structure.

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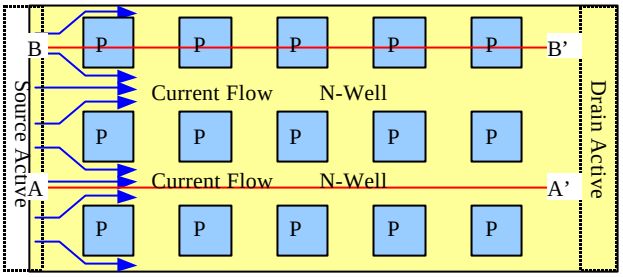
Abstract

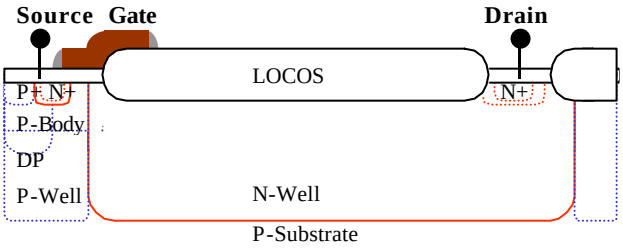
A new 700V rate charge balanced LDMOS structure is proposed. The key feature of this structure is the ***intersected N-Well and P-Well*** *that divides drift region into multi parallel conduction path. Ron,sp can be reduced by considerably high doped N-Well region and surface electric field can be dispersed by each Well junction. Ron,sp of the proposed LDMOS is* ***reduced by 55%*** *compared with conventional LDMOS. This value nearly gets to the limit of LDMOS made by bulk silicon. The surface electric field that can cause fatal failure of LDMOS in reliability characteristics is* ***decreased by 30%*** *compared with conventional LDMOS. The position occurring breakdown was moved from surface to bulk below drain contact in the proposed LDMOS.*

1. Introduction

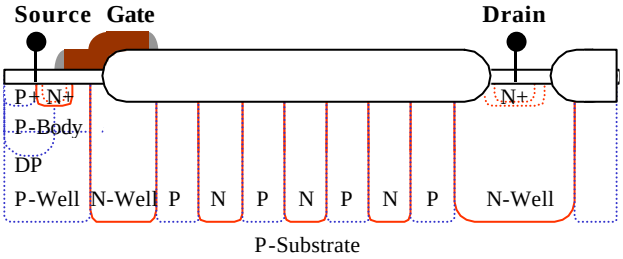
Recent advances in one chip process that integrate power IC's and power switch require the power devices with low power consumption, high breakdown voltage and high current driving capability [1]. LDMOS (Lateral Double-diffused MOS) employing double RESURF (REduced SURface Field) technology using low thickness of EPI or N-Well has allowed the construction of high voltage devices with low on-state resistance [2]. Although there were many studies to improve reliability characteristics of lateral devices [3-5], it still remains fatal failure in conventional LDMOS because the maximum electric field concentrates on the silicon surface. There is another study to reduce surface electric field maintaining Ron,sp (specific on-resistance for active area), but decrease of breakdown voltage was unavoidable [6]. In order to overcome poor reliability characteristics of LDMOS, some POWER IC's implement an external clamping diode in parallel with high voltage LDMOS, but this makes cost high. In order to obtain more stable reliability characteristics in LDMOS, the LDMOS should be designed that maximum electric field concentrates **on bulk below drain contact instead of silicon surface.**



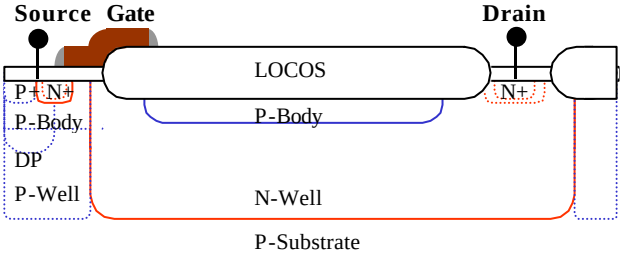
(a) Top view of proposed LDMOS



(b) Proposed LDMOS along with A-A'



(c) Proposed LDMOS along with B-B'



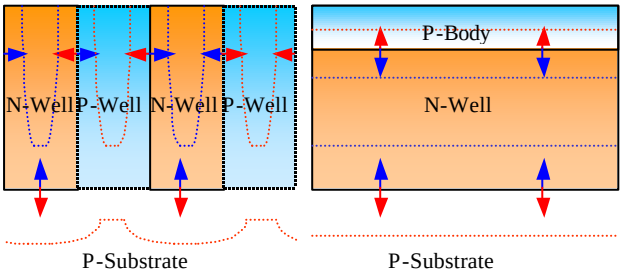
(d) Conventional double RESURF LDMOS

Figure 1. LDMOS structures

In this paper, the new 700V rate charge balanced LDMOS is introduced. This LDMOS was realized with lower Ron,sp and surface electric field by employing intersected N-Well and P-Well. The intersected N-Well and P-Well can easily deplete the drift region before breakdown occurs which results in breakdown voltage improvement. In addition, good reliability characteristics are expected by moving the breakdown occurring position from surface to bulk silicon below drain contact as surface electric field is decreased.

2. Proposed LDMOS Structure

Fig.1 (d) shows conventional double RESURF LDMOS using N-Well and P-Top to realize high breakdown voltage. In order to get high breakdown voltage extended drain region must be fully depleted before breakdown occurs. Therefore the doping level of extended drain region should be low. But this makes Ron,sp high and electric field concentrate on silicon surface. Fig. 1 (a) is the top view and Fig. 1 (b) and (c) are cross sectional view of proposed LDMOS employing intersected N-Well and P-Well. Fig. 1 (b) region can reduce Ron,sp because of considerably high doping level. And Fig. 1 (c) shows the key point of this paper how to get lower Ron,sp and decreased surface electric field with maintaining high breakdown voltage. Intersected N-Well and P-well region helps extended drain region to be easily depleted before breakdown occurs even though doping level of drift region is very high. Each junction can disperse surface electric field.



(a) Proposed (b) Conventional

Figure 2. Depletion mechanism of LDMOS (Dotted lines indicate depletion boundary)

Fig. 2 shows how drift region of LDMOS is depleted when high voltage is applied. In conventional LDMOS, depletion regions are extended from junction of N-Well to P-Body and substrate. However, in proposed LDMOS, depletion regions are extended from vertical junction of each N-Well to P-Well as well as N-Well to P-substrate junction. This enables drift region to have high doping level.

3. Simulation and Experimental Results

3.1. Ron,sp Characteristics

In order to obtain low Ron,sp, the width and doping level of intersected N-Well and P-Well must be properly optimised. We extracted the Ron,sp of proposed LDMOS from measured Ron,sp and sheet resistance of conventional LDMOS because it is impossible to simulate our three-dimensional structure using two-dimensional device simulator. The elements determining Ron of LDMOS are channel, drift, contact, metal, and etc resistances [7]. Among these elements the drift resistance is the only different element between conventional and proposed LDMOS.

To begin with, the drift resistance of conventional LDMOS is calculated from measured sheet resistance, and then other resistances are extracted by excluding drift resistance from measured Ron,sp as shown in Table 1. The drift resistance of proposed LDMOS is also calculated by using N-Well sheet resistance from experiment and one dimension simulation. Finally, Ron,sp of proposed LDMOS is calculated by adding drift resistance of proposed LDMOS to previously calculated other resistance in conventional structure.

Table 2 shows calculated Ron,sp of proposed LDMOS as a function of N-Well and P-Well dose. It can be seen from Table 1 and 2 that Ron,sp of proposed LDMOS is reduced by 55% compared with conventional LDMOS.

Table 1. Ron,sp, drift resistance, other resistance and measured BVdss of conventional LDMOS

Drift Length	Measured Ron,sp [ohm•mm^2]	Analytic calculated drift Res [ohm•mm^2]	Analytic calculated other Res [ohm•mm^2]	Measured BVdss[V]
60um	21.56	17.26	4.30	718
65um	23.43	18.83	4.60	729
70um	25.14	20.40	4.74	750
75um	26.80	21.97	4.83	770

Table 2. Analytic Calculated Ron,sp and drift resistance of proposed LDMOS

Well Dose [E12]	Numerical calculated sheet Res [ohm/sq]	Analytic calculated drift Res [ohm•mm^2]	Analytic calculated Ron,sp [ohm•mm^2]
4.0	1520	20.67	25.50
6.0	1040	14.15	18.98
8.0	804	10.94	15.77
10.0	660	8.98	13.81
12.0	563	7.66	12.49
14.0	***492***	***6.69***	***11.52***
16.0	439	5.97	10.80

3.2. Breakdown Characteristics

In order to get high breakdown voltage, the extended drain region, intersected N-Well and P-Well, must be fully depleted before breakdown occurs. In order to get maximum depletion width before breakdown, we simulated simple diode structure composed of N-Well and P-Well. Fig. 3 shows maximum depletion width as a function of N-Well and P-Well dose. Maximum depletion width decreases as N-Well and P-Well dose increase. This is the important factor to optimise N-Well and P-Well width. And then, from above simulation data, two dimensional breakdown simulation was performed by changing intersected N-Well and P-Well width from 4.5um to 7.0um and dose from 1.0E13 to 1.6E13cm^{-2}.

The results are shown in Fig. 4. It is seen that breakdown voltage of proposed LDMOS was found to be over 700V and the position occurring breakdown was moved from silicon surface to bulk below drain contact **in condition of intersected N-Well and P-Well width of 5.0um and dose of 1.4E13.** Fig.5 shows potential contours and the position occurring breakdown of conventional and proposed LDMOS when breakdown occurred.

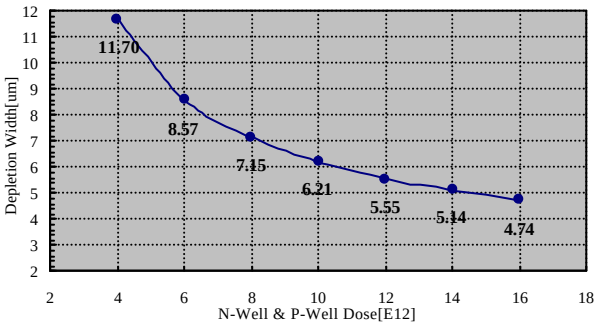


Figure 3. Depletion width as a function of Well dose

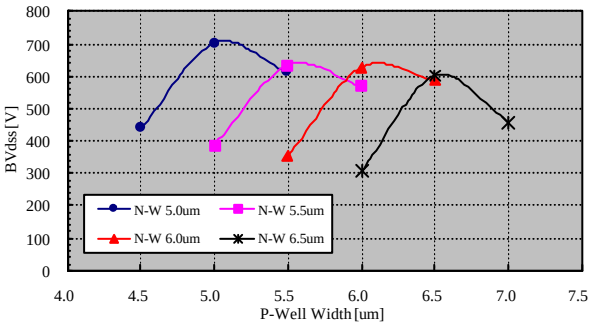
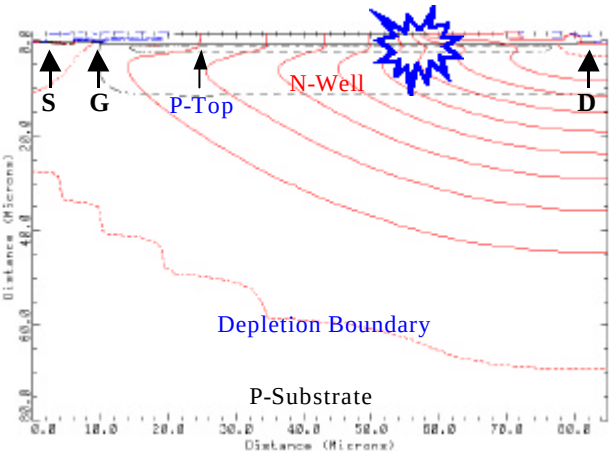


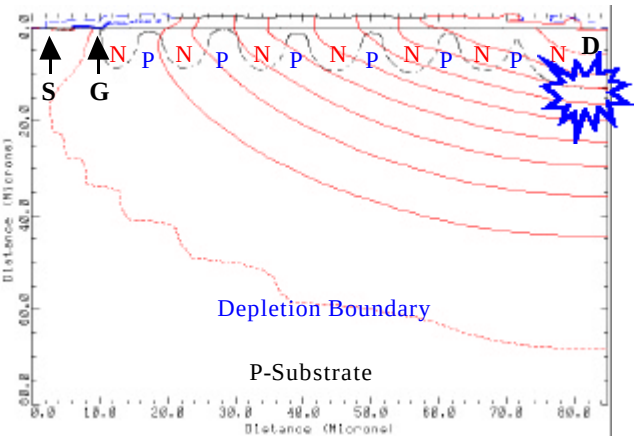
Figure 4. Breakdown voltage as a function of Well width at Well dose of 1.4E13

3.3. Comparison of conventional and proposed

Fig. 6 shows Ron,sp comparison of conventional double RESURF LDMOS [6], thin SOI LDMOS [8], and proposed charge balanced LDMOS. The Ron,sp was reduced by 55% than that of conventional LDMOS. Although Ron,sp of thin SOI LDMOS is little bit smaller than that of proposed LDMOS, the fabrication cost of proposed LDMOS is remarkably lower than that of thin SOI LDMOS



(a) Conventional LDMOS



(d) Proposed charge balanced LDMOS

Figure 5. Potential contours of LDMOS when breakdown occurred (Explosive mark indicates the position occurring breakdown, solid line indicate potential contours)

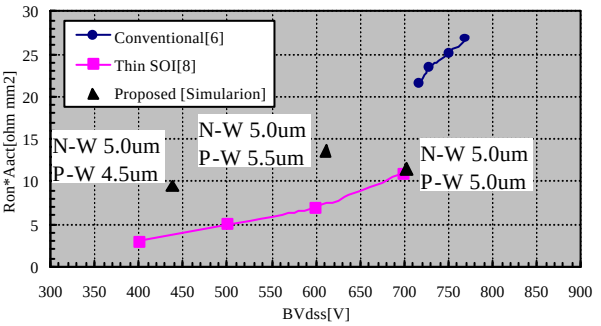
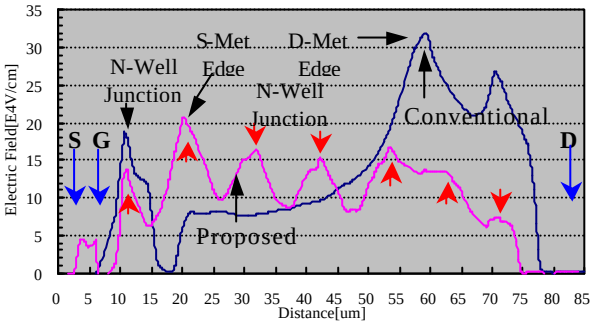
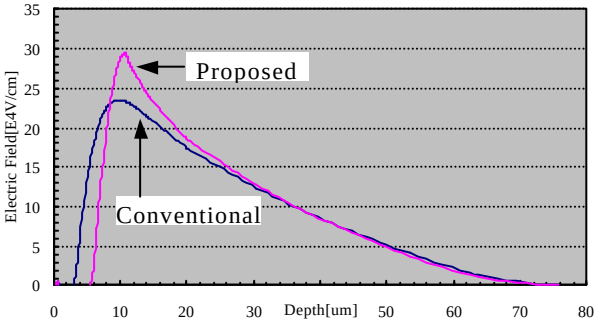


Figure 6. Ron,sp versus BVdss of LDMOS employing conventional double RESURF, proposed charge balanced and thin SOI

Fig. 7 shows comparison of (a) surface and (b) bulk below drain contact electric field when breakdown occurred. As you see in fig. 7 (a), the maximum surface electric field of proposed LDMOS was decreased by 30% than that of conventional LDMOS. Electric field was concentrated on silicon surface in conventional LDMOS. But in proposed LDMOS, electric field was slightly concentrated on each of N-Well and P-Well junction and electric field did not reach critical electric field. It indicates that reliability characteristics of proposed LDMOS is more stable than conventional LDMOS. Table 3 shows comparison of conventional LDMOS and proposed LDMOS.



(a) Surface electric field



(b) Bulk electric field along a vertical line passing through LDMOS drain contact

Figure 7. Comparison of electric field of LDMOS when breakdown occurred

Table 3. Comparison of conventional and proposed

LDMOS	Conventional	Proposed
Drift Length	75um	75um
Ron,sp	26.80 ohm•mm^2	***11.52* ohm•mm^2**
Simulation BVdss	698V	703V
Experiment BVdss	770V	-
Max surface E-Field	3.20E5	2.08E5
Breakdwon position	Surface below drain metal edge	Bulk under drain contact

4. Conclusions

We proposed the new LDMOS structure having very low on-resistance and good reliability characteristics. The Ron,sp of proposed LDMOS employing intersected N-Well and P-Well was reduced by 55% compared with that of conventional double RESURF LDMOS. The maximum surface electric field of proposed LDMOS was also decreased by 30% compared with that of conventional LDMOS at same breakdown voltage. This leads more stable reliability characteristics in proposed LDMOS. In addition, the fabrication cost will be reduced by skip of p-top mask. The proposed LDMOS would be implemented on 1.2um Bi-CMOS process, and applied to switch mode power supply 1chip IC's.

5. References

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