Reduction of Short-Channel Effects and Improvement in Microwave Characteristics for V-groove Gate Pseudomorphic Doped-Channel HFET with Dual V-groove Gate Structure

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Abstract

The single V-groove gate and dual V-groove gate device have been fabricated successful at the same ship at the same time. The dual V-groove gate employs its cascode structure to reduce the output conductance furthermore decrease the short channel effect which the reduced gate length down to sub-micron or used V-groove gate structure. The measured transconductance and output conductance at V_{GS}=0 V are 275mS/mm (245mS/mm) and 9.64mS/mm (1.46mS/mm) for V-groove gate (dual V-groove gate) device, resulting in A_V=28.52 (167.8). The second gate G2 increase from 0V to 1.0V, the output conductance decrease from 0.63mS/mm to –0.45mS/mm at G1=0V. Beginning at G2=+0.4V, the I-V characteristic curve have negative differential resistance. The maximum transconductance to output conductance ratio 192/0.011=17454.54 is available. The measured current gain cut-off frequencies (f_t) of single V-groove gate HFET is 22.5GHz and maximum stable gain frequency is 33.5GHz. The microwave characteristics of dual V-groove gate HFET will be presented.

1. Introduction

With the increasing request for high-speed and high-quality components in wireless mobile communication applications, sub-micron field-effect transistors (FETs) have been widely used as low-noise amplifiers (LNAs) and high-frequency power amplifiers [1-2]. Reducing the gate length of FET is the most effective way to improve the high frequency performance. It is because that the gate capacitance decreases and the overshoot effect becomes more noticeable. Quarter-micro meter gate length FET's have suffered from the short channel effect and the leakage current under the channel that causes the threshold voltage to shift toward the pinch-off voltage.

To date, most of the commercially used GaAs-based FETs comprise a gate of about 0.5 μm in length. However, it is very difficult to obtain such a sub-micro metal gate with acceptable performance and processing yield by using conventional optical lithography (in particular, with G- and I-line aligner).

The conventional V-groove gate pseudomorphic doped-channel heterjunction FET by III-V compound materials such as InGaP/InGaAs is an alternative candidate that exhibits an effective gate length down to quarter-micron dimension. On the other hand, this sub-micron gate device obtained from a micro-level gate window generally exhibits better direct-current (DC) and radio-frequency (RF) performances as compared to those of traditional devices fabricated with the same gate window. In this paper, we have demonstrated a dual V-groove gate structure. It comprises a cascode structure, where a configuration including a common source and a common gate is provided while the drain of first HFET is connected to the source of the second HFET. It has a high gain and a bandwidth such that the output conductance is reduced in the range from DC to microwave frequency to overcome the short channel effect [4] and thus improve the microwave characteristics.

2. Device Structure and Fabrication

The structure was epitaxially grown by molecular beam epitaxy (MBE) on a Cr-doped (100) GaAs substrate. Along the growth direction, the epitaxial layers consist of a 0.6-ì m thick undoped GaAs buffer layer, a 150 Å thick n doped InGaAs channel layer with 5×10^{18}cm^{-3}, a 200 Å thick undoped InGaP layer, and a 0.7~1 ì m thick undoped GaAs sacrificial layer. Figure 1 shows the parameters of the device cross-section of a V-groove gate InGaP/InGaAs doped channel HFET.

The device fabrication started with mesa formation. Since wet etching for GaAs is anisotropic, we chose the

direction of the gate width parallel to [110]. The GaAs-base layer was etched by $H_2SO_4/H_2O_2/H_2O$, the InGaP layer was etched by HCl/H_3PO_4, and the InGaAs layer was etched by $H_3PO_4/H_2O_2/H_2O$. Au/Ge ohmic contact metal was evaporated on the InGaP layer and then annealed at 450℃ for ten seconds for three times in a rapid thermal process. The 1-ì m gate window was defined by the conventional optical lithography on the undoped GaAs sacrificial layer. Before the deposition of gate shottky metal, the undoped GaAs sacrificial layer was etched by $H_2SO_4/H_2O_2/H_2O$ to form a V-groove gate. Since both the single-gate pattern and the dual-gate pattern were formed on the same mask, therefore, we obtain the single-gate device and dual-gate device at the same time. Figure 2 is a SEM picture showing the cross section of the fabricated dual V-groove gate InGaP/InGaAs doped channel HFET.

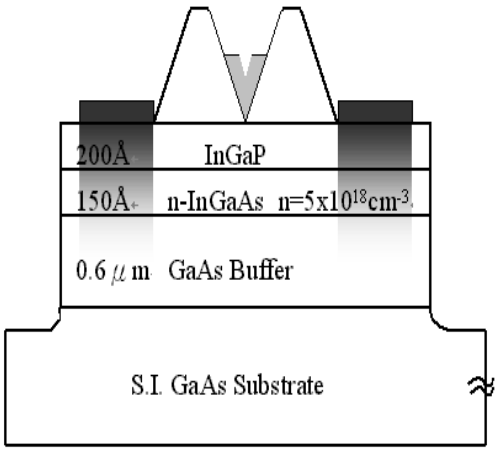

Fig. 1 Device cross-section of V-groove gate InGaP/InGaAs doped channel HFET.

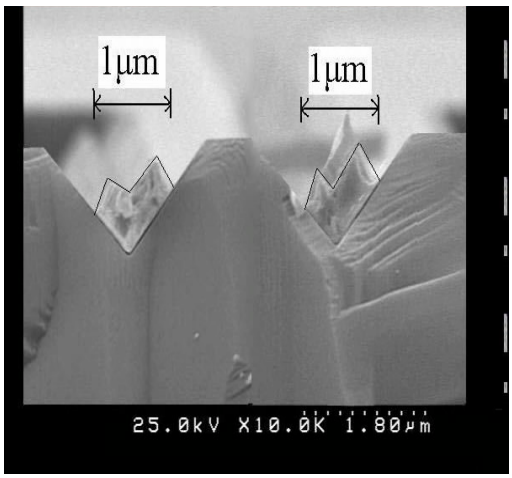

Fig. 2 The SEM picture for dual V-groove gate InGaP/InGaAs doped channel HFET.

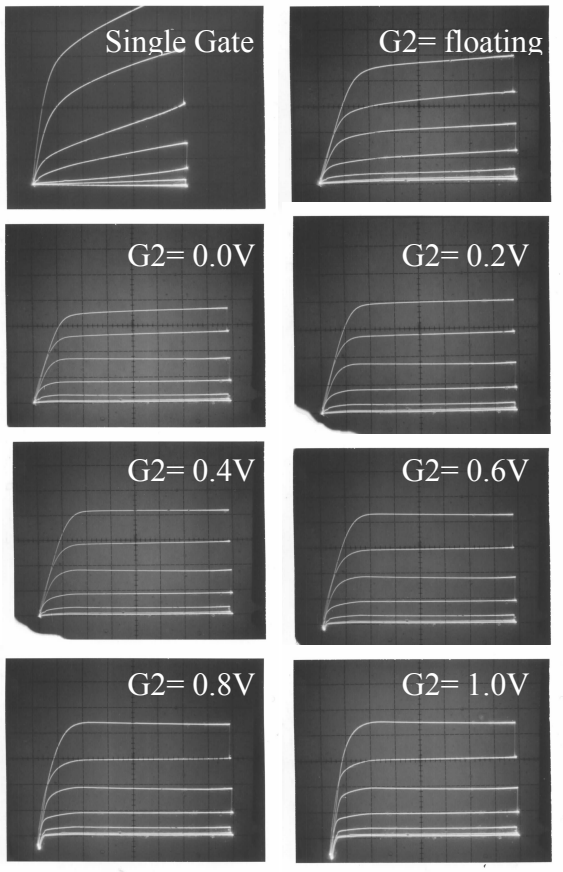

Figure 3 The common-source I-V characteristics of the V-groove gate InGaP/InGaAs doped channel HFET. The scales for V_{DS} is 1.0V/div, for I_D 2mA/div, for the first gate bias G1 -0.2V/step and for the maximum V_{GS} 0V.

The single-gate dimension is 1×100 μm^2 with the drain-to-source spacing of 4 μm, while the dual-gate dimension is the same but with a drain-to source spacing of 7 μm. The second gate of the dual V-groove gate device is located closer to the drain that can reduce the field under the first gate and increase the isolation between the first gate and the drain.

3. Device performance and Discussion

The device was measured for DC and microwave characteristic. The measured I-V characteristics were shown in Figure 3. The scale for the drain-to-source voltage is V_{DS}=+1.0V/div, for the drain current I_D=2mA/div, for the first gate bias G1=0.2V/step. The second gate bias varies from 0V to 1.0V with 0.2V/step. Figure 3 also shows the DC characteristics for the single gate device and the floating second gate G2. The considerably weak kink effect observed in the single V-groove gate device almost disappears for the dual V-groove gate device. The dual V-groove gate structure

exhibits reduced efficiently short channel effect by using the floating second gate G2. Furthermore, we chose the optimum second gate bias G2 to obtain the I-V characteristic as desired.

The transconductance was measured at the bias of drain-to-source voltage V_{DS}=+4.0V and first gate voltage G1=-1.0V~+1.0V. The voltage of the G2 controls the saturated drain current (I_{DS}) and transconductance (g_m). The device with the second gate G2 floating and the single gate device characteristics are as shown in Figure 4. The single V-groove gate device has a poorer cut-off voltage then the dual V-groove gate device. The excellent pinch-off voltage of the dual V-groove gate device is also depicted as in Figure 4. The dual V-groove gate device having the second gate can apply voltage variably and their g_m falls off sharply as the second gate bias that the channel under the first gate is no longer saturated. But the g_m under the first gate value above 1.0V is decreased by about 14% compared with the single V-groove gate device. We can obtain the result that we can control the saturated drain current, the transconductance and the output conductance of the dual V-groove gate FET by the control of the G2 voltage in spite of scarifying a small amount of gain. The measured transconductance and the output conductance at V_{GS}=0 V are 275mS/mm (245mS/mm) and 9.64mS/mm (1.46mS/mm) for single V-groove gate (dual V-groove gate) device, resulting in A_V=28.52 (167.8). The second gate voltage G2 increases from 0V to 1.0V, therefore the output conductance decrease from 0.63mS/mm to –0.45mS/mm at G1=0V. We also observe that, from G2=+0.4V, the I-V characteristic curve exhibits negative differential resistance. The maximum transconductance to output conductance ratio is 192/0.011=17454.54.

The small signal equivalent circuit of the dual V-groove gate employed is in a cascode configuration of two HFETs. A coupling capacitor is inter-posed between a common source and a common gate configuration. In the equivalent circuit, the input impedance value for the single V-groove gate device is close to that of the dual V-groove gate device, but the output impedance for the single V-groove gate device differs a lot from the dual V-groove gate device. The output resistance R_{OUT} and the transconductance g_m of a dual V-groove gate device is expressed as,

$$g_m \sim g_{m1}$$
$$R_{OUT} \sim R_{DS1} R_{DS2} g_{m2}$$

where g_{m1} is the transconductance of the common source configuration in the dual V-groove gate device, g_{m2} is the transconductance of the common gate configuration, R_{DS1} is the output resistance of the common source configuration and R_{DS2} is the output resistance of the common gate configuration. Due to the large output resistance of the dual V-groove gate device, the output conductance is very small. Therefore, the unilateral gain of the dual V-groove gate device is higher than that of a comparable single V-groove gate device. These two kinds of devices behaved quite differently in microwave characteristics. The measured current gain cut-off frequencies (f_t) is 22.5GHz and the maximum stable gain frequency (f_{MAX}) is 33.5GHz for the single V-groove gate HFET. Furthermore, the microwave characteristics of the dual V-groove gate HFET will be presented.

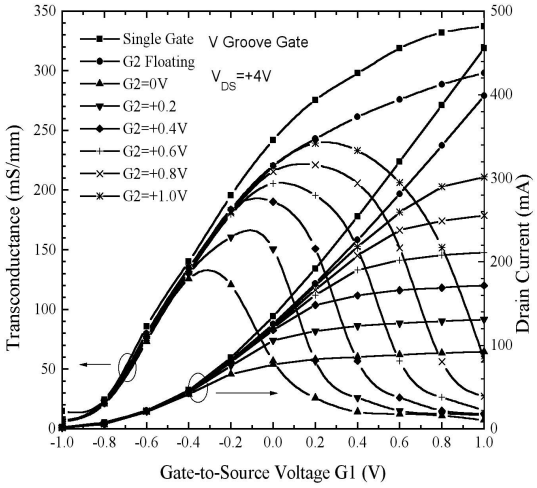

Figure 4 The transconductance (gm) and drain saturation current (I_{DS}) as function of V_{GS} voltage. The V_{DS} voltage is fixed at +4.0V. The second gate G2 is applied from 0.0V to 1.0V .

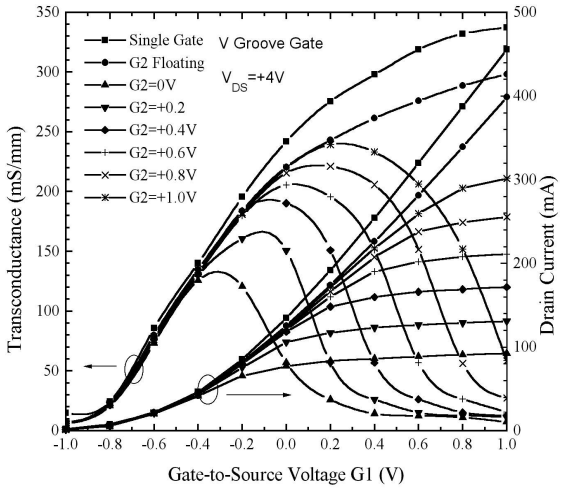

Figure 5 The output conductance (g_D) as function of the second gate G2 voltage. The V_{DS} voltage is fixed at +4.0V and first gate G1 is fixed at 0.0V. The second gate G2 is applied from 0.0V to 1.0V

4. Conclusion

In summary, the dual V-groove gate doped channel HFET have been fabricated that have successful reduced the output conductance and short channel effect of single V-groove gate by the second gate variably bias G2. The maximum transconductance to output conductance ratio 192/0.011=17454.54 is available. It has the best advantage that mask does not need more and choose the optimum second gate bias G2 to obtain the I-V characteristic that we want.

5. Acknowledgement

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6. References

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