Voltage-controlled substrate structure for integrated inductors in standard digital CMOS technologies

Judith Maget[*,o], Rainer Kraus[*], Marc Tiebout[o]
[*]*University of Bundeswehr, Institute of Electronics, D-85577 Neubiberg*
[o]*Infineon Technologies AG, Corporate Research, D-81730 Munich*
judith.maget@unibw-muenchen.de

Abstract

A new substrate structure for integrated inductors in standard CMOS technology is presented. It is comprised of alternating n^--well and p^--substrate regions. Through applying a voltage to the structure the semiconductor region below the inductor is depleted from mobile charge carriers up to a certain depth. Substrate losses due to parasitic capacitances and eddy currents are reduced. Without applied voltage the peak quality factor and the corresponding frequency is increased by 34% compared to an inductor without substrate structure. Through applying a voltage a total increase of quality factor by more than 41% and of resonance frequency by up to 56% is achieved.

1. Introduction

LC-Tank VCOs (voltage controlled oscillators) are building blocks in transceivers for wireless communications. The inductance L and the parallel capacitance C determine the oscillation frequency f of the VCO by

$$f = \frac{1}{2\pi\sqrt{LC}}. \quad (1)$$

Varactors are used to cover a certain frequency band and the active part of the VCO overcomes losses in the tank.
To reduce phase noise of the VCO the passive elements of the tank need to have large quality factors, as the quality factor of the LC-tank Q_{LC} quadratically influences the phase noise S_{SSB} of the VCO [1]

$$S_{SSB} = F\frac{kT}{2P_{SIG}}\frac{\Delta f^2}{Q_{LC}^2 f_0^2} \quad (2)$$

where P_{SIG} is the signal power, F the noise factor of the active devices and f_0 and Δf the oscillation and offset frequency, respectively.
At the frequencies for mobile communications the quality factors of integrated inductors are usually much lower than the quality factors of conventional diode or MOS varactors. In these applications the inductors determine the worst-case phase noise and whether VCO specifications can be met.
The performance of integrated inductors is strongly influenced by losses through undesired currents in the substrate or by the series resistance of the inductors windings. Especially in digital CMOS technologies the thickness of the metal layers is much lower than in bipolar and BiCMOS technologies, leading to higher series resistances. Further the substrates are highly doped leading to large substrate losses.
The urge to use digital CMOS technologies is on the one hand the desire to integrate both digital and analog functions on the same chip and on the other hand the low cost of digital CMOS technologies.
To describe substrate losses Fig. 1 shows the cross section of a simple (one metal layer) integrated inductor. The grey bar indicates the metal layer. The inductor is described by the inductance L and the series resistance of the metal windings R_s. There are parasitic capacitances from input to output C_f and from the inductor to the substrate C_{ox}. R_{sub} describes an effective substrate resistance.

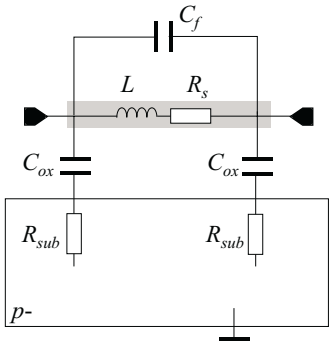

Figure 1. Cross section of a simple one-layer inductor (grey bar) and its lumped-elements model.

The output signal of the VCO appears at the inductor nodes. The swing of this signal is large (almost V_{dd} due to phase noise reasons) and the inductor is subject to large-signal AC currents resulting in undesired substrate currents. First, the capacitive coupling between the inductor and the substrate through C_{ox} leads to capacitively induced substrate currents. Second, the constantly changing magnetic field around the inductor results in inductively induced eddy currents.
A variety of substrate structures and ground shields has been published. Many aim mainly at reducing eddy cur-

rents [2, 3, 4, 5], whereas capacitive coupling between inductor and substrate remains constant or is even increased. A reduction of parasitic capacitances is achieved in [5, 6, 7, 8], but always in non-standard CMOS technology. The only solution compatible with standard CMOS technology is obtained by a biased n^--well described in [9]. But this solution has a homogeneous region below the inductor. Only a vertical depletion region below the n^--well can be used to decrease the parasitic capacitance, and there is no patterning that could reduce eddy currents.
This work presents a substrate structure for integrated inductors in standard digital CMOS technologies to reduce the parasitic capacitance C_{ox} and undesired current flow in the substrate. Simultaneously eddy currents are reduced and further patterning is accommodated.
The structure is fully compatible with standard digital CMOS process flow and low resistivity substrates (here: 8Ωcm).
Four test structures with the identical inductor, three with and one without substrate structure, were fabricated in a standard 0.12μm digital CMOS process.

2. Substrate structure

The cross-section of the substrate structure and (for simplicity) a one-metal-layer inductor is shown in Fig. 2, a top view in Fig. 3.

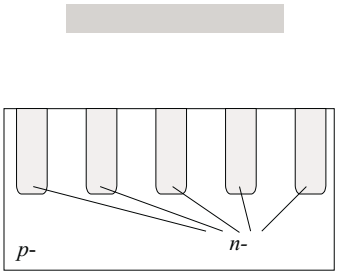

Figure 2. Substrate structure: thin, parallel n- wells in p- substrate and a simple one-layer inductor (grey bar).

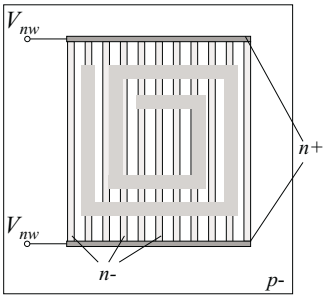

Figure 3. Substrate structure: thin, parallel n- wells in p- substrate and a simple one-layer inductor.

The substrate structure is in the simplest case implemented as parallel stripes of equidistant n^--well and p^--substrate regions. At both ends the n^--wells are connected by highly doped n^+-regions and a voltage can be applied. Metal fill structures, which are common to modern sub-micron process, are suppressed for the benefit of a higher quality factor [10].
Increasing the voltage applied to the n^--wells increases the depletion region laterally between them, and vertically beneath them. At some n^--well voltage the depletion regions of two adjacent n^--wells will touch and deplete the p^--substrate totally to at least the depth of the n^--wells (Fig. 4). The n^--wells themselves will be partially depleted, too.

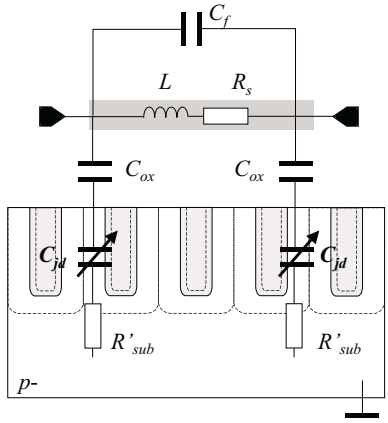

Figure 4. Simple inductor (grey bar) and substrate structure with totally depleted p^--substrate regions between the n^--wells. Dashed lines indicate the borders of the depletion regions.

The depleted semiconductor layer leads to a reduced effective small-signal capacitance between inductor and substrate. Assuming that the non-depleted width of the n^--wells is neglectable, this capacitance can be approximated by

$$C_{eff} = (C_{ox}^{-1} + C_{jd}^{-1})^{-1}. \quad (3)$$

with C_{jd} the depletion region capacitance.
As parasitic capacitances reduce the quality factor and the self-resonance frequency of the inductor, the performance of an inductor can be enhanced by applying a voltage to the substrate structure.
Patterning the substrate structure as described in [2, 5] can further reduce the influence of eddy currents.
The n^--wells should be as thin as possible, as they usually can be depleted only partially due to their higher doping compared to the p^--substrate.

3. Measurement results

Three identical three metal-layer inductors (metals 2,3,4) with substrate structures having different distances of the n^--wells (0.7μm, 1.0μm and 1.3μm) have been fabricated in a standard 0.12μm CMOS process. For comparison reasons also an inductor without substrate

structure is measured. The n^--well width has been chosen to be the minimum allowed in the process.
The inductors have five windings with staggered winding width to reduce series resistances. Fig. 5 shows a die photograph of one of the inductors. Clearly visible is the suppression of metal fill structures in the area of the inductor. Inductor size is 200μm x 200μm.

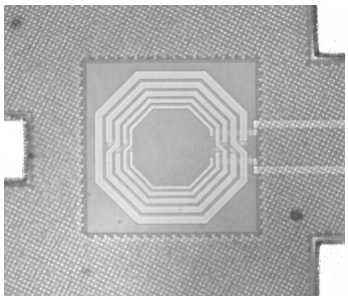

Figure 5. Die photograph of one of the inductors.

The effective inductance is extracted from S-parameter measurements (HP 8510)

$$L = \frac{\mathrm{Im}(Y_{11}^{-1})}{2\pi f}. \quad (4)$$

with f the frequency. The measured low frequency inductance is 4nH at a DC series resistance of 6.2Ω.
The quality factor is obtained according to the 3dB-bandwidth definition [11]. An ideal capacitance (no series resistance) is numerically added in parallel to the measured Y_{11} data of the inductor. The 3dB-bandwidth at the resonance frequency of the resulting network is then converted to an effective quality factor Q_{BW} using relationships for simple parallel RLC circuits.
This definition is the most useful for designing any circuit with a LC-tank and it is also valid at self-resonance frequencies of the inductors.
Figs. 6 - 8 visualize the results, table 1 lists the values for measured quality factors.

Table 1. Maximum quality factors and corresponding resonance frequencies at different n^--well voltages.

	$Q_{BW,max}@f_{resonance}$		
V_{nw}	0.7μm	1.0μm	1.3μm
0 V	11.5@4.3GHz	10.9@4.0GHz	10.5@3.9GHz
1.5 V	12@5.0GHz	12.1@5GHz	10.9@4.4GHz
3 V	12@5.0GHz	12.1@5GHz	11.6@4.9GHz
4.5 V	12@5.0GHz	12.1@5GHz	11.9@5GHz

reference: 8.6@3.2GHz

Fig. 6 depicts the quality factors of the inductor with a 0.7μm distance of the n^--wells for 4 different n^--well voltages V_{nw} and the reference inductor.

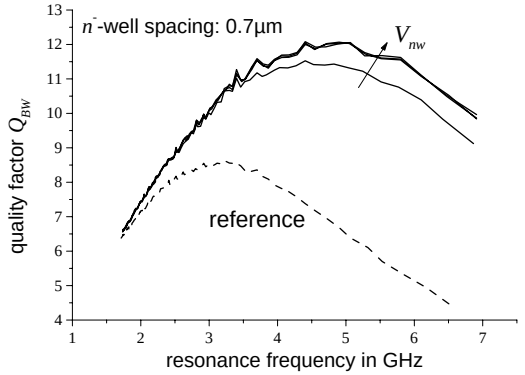

Figure 6. Quality factors of the inductor with n^--well distance 0.7μm and at n^--well voltages [0V;4.5V;1.5V].

Due to the built-in voltage (ca. 1V) of the n^--well/p^--substrate junction, depletion regions are already present at zero n^--well voltage. They reduce C_{eff} (see Eq. 3) and also eddy currents. Thus, already at zero V_{nw} the substrate structure increases the maximum quality factor as well as the corresponding resonance frequency by 34% compared to the reference inductor.
Increasing V_{nw} from 0V to 1.5V increases the maximum quality factor by further 5%. The corresponding resonance frequency is 16% higher.
At the n^--well voltages 3V and 4.5V no influence is observed any more: the p^--substrate regions are totally depleted at 1.5V already.
The quality factor results for the inductor with n^--well distance of 1.0μm are shown in Fig. 7. At zero n^--well voltage a 27% higher quality factor and a 25% shift in resonance frequency is obtained. With a V_{nw} increase from 0V to 1.5V the maximum quality factor of the inductor increases by further 12% and the resonance frequency shifts by 25%.
Similarly to the substrate structure with 0.7μm distance of the n^--wells, the p^--substrate regions seem to be totally depleted at 1.5V already and a further increase of applied voltage has no effect.

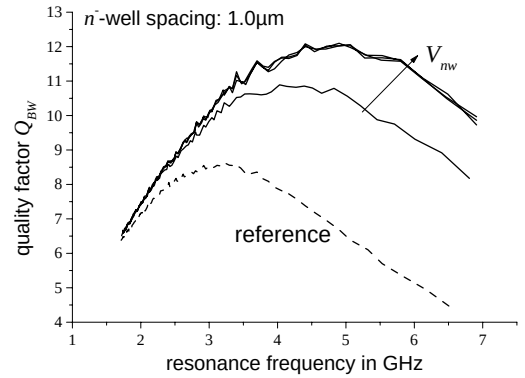

Figure 7. Quality factors of the inductor with n^--well distance 1.0μm and at n^--well voltages [0V;4.5V;1.5V].

Fig. 8 depicts the quality factor of the inductor with 1.3μm n^--well distance. At zero V_{nw} a 16% higher maximum quality factor and a 22% higher resonance frequency as for the reference inductor are observed. The maximum quality factors are increased by further 14% through applying a voltage. The resonance frequency shifts to higher frequencies by another 28%.
Contrary to the two inductors with less n^--well spacing different maxima are observed at all voltages V_{nw}, indicating that only above 4.5V a total depletion of the p^--substrate regions between the n^--wells can be obtained.

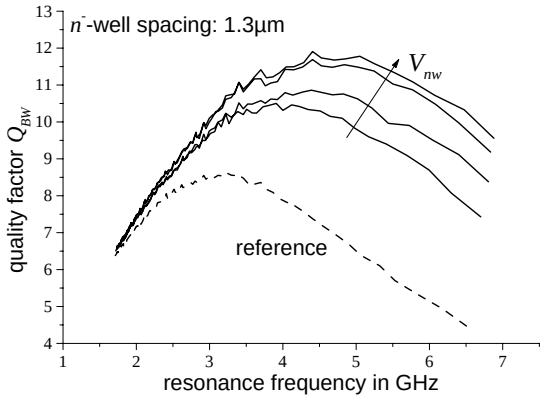

Figure 8. Quality factors of the inductor with n^--well distance 1.3μm and at n^--well voltages [0V;4.5V;1.5V].

Apparently the maximum quality factors at zero V_{nw} are lower with larger n^--well distance (compare Figs. 6, 7, 8). With closely spaced n^--wells the depletion regions due to the built-in voltage of n^--well/p^--substrate junction lead to a larger amount of depleted area and smaller capacitance. At larger n^--well spacing this situation with already - to some extent - decreased capacitance is only reached at some non-zero V_{nw}.
Additionally more freely flowing eddy currents in wider p^--substrate regions might be of importance.
But all inductors reach the same values at total depletion between the p^--substrate.
As mentioned before, patterning the n^--wells according to [2, 5] can strongly reduce eddy currents leading to a further increase of the quality factor.

4. Conclusion

A new substrate structure for inductors consisting of alternating n^--well and p^--substrate regions with voltage controlled, variable lateral and vertical depletion regions is presented. The structure covers the whole area underneath an inductor and is compatible with standard digital CMOS process flow. The inductors with substrate structure are compared to an inductor without the proposed structure. Applying a voltage to the structure alters depletion regions and the number of free carriers underneath the inductor. Thus the parasitic capacitances and eddy currents can be reduced. Already at zero n^--well voltage quality factor and resonance frequency advantages of 34% are achieved. Applying a voltage to the substrate structure increases the maximum quality factor by 41%. Simultaneously the resonance frequency at peak quality factor shifts towards higher frequencies by up to 56%. Especially at high frequencies the advantages of the new structure are obvious.

[1] D.B. Leeson, "A simple model of feedback oscillator noise spectrum", *Proc. IEEE*, Feb. 1966, pp. 329-330.

[2] C.P. Yue, and S.S. Wong, "On-Chip spiral inductors with patterned ground shields for Si-based RF IC's", *IEEE Journal of Solid State Circuits*, Vol. 33, No. 5, May 1998, pp. 743-752.

[3] T. Yoshitomi, et al., "On-Chip spiral inductors with diffused shields using channel-stop implant", *International Electron Device Meeting*, Washington DC, USA, Dec. 1998, pp. 540-543.

[4] J.N. Burghartz, "Progress in RF inductors on silicon - understanding substrate losses", *International Electron Device Meeting*, Washington DC, USA, Dec. 1998, pp. 523-526.

[5] S.M. Yim, T. Chen, and K.K. O, "The effect of a ground shield on the characteristics and performance of spiral inductors", *IEEE Journal of Solid State Circuits*, Vol. 37, No. 2, Feb. 2002, pp. 237-243.

[6] M. Park, et al. "High Q microwave inductors in CMOS double-metal technology and its substrate bias effects for 2GHz RF ICs application", *International Electron Device Meeting*, Washington DC, USA, Dec. 1997, pp. 59-62.

[7] H. Erzgraber, et al. "A novel buried oxide isolation for monolithic RF inductors in silicon", *International Electron Device Meeting*, Washington DC, USA, Dec. 1998, pp. 535-539.

[8] H. Jiang, et al. "Electromagnetically shielded high-Q CMOS-compatible copper inductors", *International Solid State Circuits Conference*, Feb. 2000, pp. 330-331.

[9] K. Kim, and K. O, "Characteristics of an integrated spiral inductor with an underlying n^--Well", *IEEE Transactions on Electron Devices*, Vol. 44, No. 9, Sept. 1997, pp. 1565-1567.

[10] W. DeCock, and M. Steyaert, "A CMOS 10GHz voltage controlled LC-oscillator with integrated high-Q inductor", *European Solid State Circuits Conference*, Villach, Austria, Sept. 2001, pp. 496-499.

[11] K. O, "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies", *IEEE Journal of Solid State Circuits*, Vol. 33, No. 8, Aug. 1998, pp. 1249-1252.