Vertical high voltage devices on thick SOI with back-end trench formation

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Abstract

We present a new process flow for the integration of vertical high voltage devices on thick SOI. The creation of slip dislocations has been avoided by etching and filling the trenches at the end of the process. Thereby are the trenches not exposed to high temperature steps which trigger the creation of these defects. The electrical characteristics of the fabricated devices are not affected by these process modifications. High voltage transistors with breakdown voltages of 480 V have been fabricated with this new process.

1. Introduction

SOI substrates offer the possibility to integrate more functions on the same chip for smart power applications. Different areas of the chip can be isolated by deep trench isolation. The monolithic integration of vertical power devices together with control circuits increases the functionality and minimizes the size of the chips.

The integration of vertical DMOS transistors [1] and bipolar power devices [2] on thick SOI substrates has been demonstrated. In our former process many defects [3] have been created during high temperature steps. In that process we have not been restricted in terms of diffusion temperature and time in order to create a low resistive current path between the drift region and the drain contact. In this study we avoided the formation of the slip dislocations by etching and refilling the trenches at the end of the process. By doing this we have been restrained in the choice of the diffusion temperature and time.

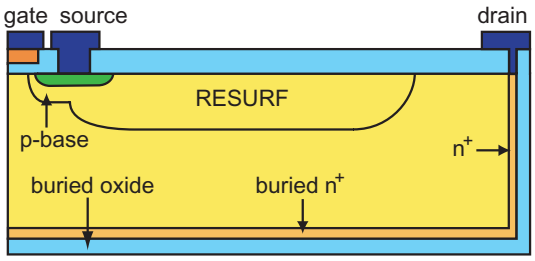

Figure 1. Schematic drawing of our devices.

2. Device structure

A schematic drawing of the vertical DMOSFET is shown in fig. 1. Due to the buried oxide all contacts are on the top of the structure. A buried n^+-layer was created in the 50 μm thick silicon layer prior to wafer bonding and phosphor has been diffused into the trench side walls in order to create a low resistive current path between the drift region and the drain contact.

The structure has to withstand high voltages in the vertical and lateral direction. The vertical breakdown is determined by the SOI layer thickness, its doping level, and by the p-base curvature. RESURF terminations are used to reduce the consumed area by reducing the surface field. The doping concentration is determined by the charge balance criteria [4]. Three different RESURF terminations have been used: one with uniform doping, a second with a step doping profile in the lateral direction, and a third with a laterally graded doping profile [5]. The latter two are shorter as the first one, thus reduce the specific on-resistance for a given device size. Fig. 2 shows a homogeneous potential distribution due to the RESURF termination for an applied voltage of 515 V.

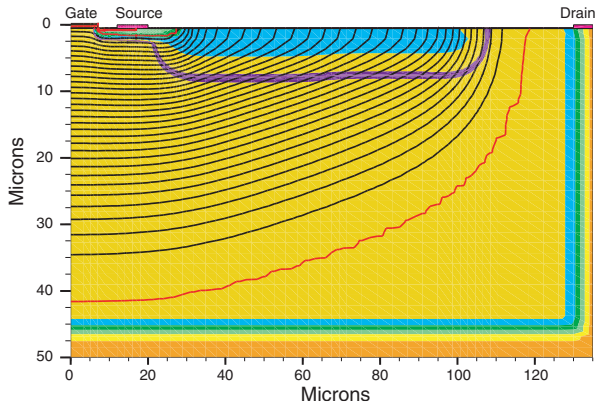

Figure 2. Homogeneous potential distribution due to RESURF termination at an applied voltage of 515 V.

Devices with different gate length and width, with different cells sizes, and different number of cells have been manufactured and studied. Furthermore, low voltage nMOS and pMOS devices, as well as lateral DMOS transistors have been included in the chip layout.

3. Process description

First a thick field oxide is grown on top of a 50 μm thick device layer and is patterned prior the RESURF implantations. The implantation energy is 50 keV and a boron dose of $2.8{\cdot}10^{12}$ cm^{-2} is chosen for the uniform doping profile and the graded doping profile and $2.4{\cdot}10^{12}$ cm^{-2} for the second step of the step doping profile. A thin cap oxide is grown at 1000°C in order to avoid out-diffusion of the boron during the 15 h long RESURF drive-in at 1200°C. After this step the formation of the slip dislocations can be observed if the trenches are etched at the beginning of the process [1].

The cap oxide is removed and a 50 nm thick gate oxide is grown followed by polysilicon deposition. We do not implant dopants into the polysilicon at this point, because they can diffuse through the gate oxide into the silicon during the high temperature p-base drive-in. After patterning the polysilicon gate with a ICP dry etch system boron is implanted at an energy of 90 keV and a dose of $6{\cdot}10^{13}$ cm^{-2}. The p-base is formed during a diffusion step at 1100°C for 120 min, which results in a lateral diffusion of 1.3 μm.

The source and drain areas are formed by an arsenic implantation (dose $5{\cdot}10^{15}$ cm^{-2} and energy 50 keV). During this step dopants are introduced into the polysilicon as well. The p^+-contacts are implanted with a dose of $5{\cdot}10^{15}$ cm^{-2} and an energy of 50 keV. A CVD oxide (TEOS) is deposited and patterned with the trench mask. The trenches are etched all the way down to the buried oxide with a STS DRIE system at a plasma frequency of 380 kHz in order to avoid notching [6]. The trench etch has been optimized for a trench thickness of 4 μm. Phosphor is diffused from solid sources into the sidewalls for

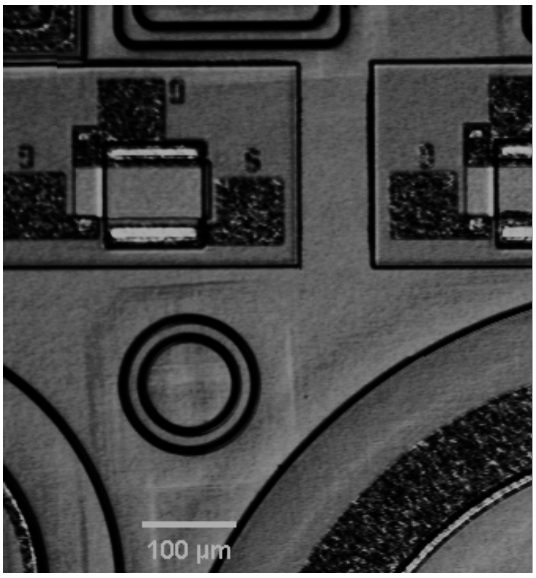

Figure 3. Slip lines at the surface can be observed after high temperature steps.

1h at 1050°C. This diffusion step is sufficient to form low resistive trench side walls. The diffusion temperature and time, on the other hand, are low enough in order to avoid the formation of defects. During this step the n^+- and p^+-contact implantations are activated. A 0.8 μm thick TEOS oxide is deposited followed by a polysilicon deposition of 3 μm. The excess polysilicon is removed with a CMP step. The process is completed by contact hole etch and metalization.

4. Results

By moving the trench etch at the end of the process we have successfully avoided the creation of sliding planes. These sliding planes can be created during high temperature steps (RESURF and p-base drive-in). Figure 3 shows a wafer from a former process, where the process started by etching and refilling the trenches. The slip lines can clearly be seen at the round structure. These defects have been created around all trenches. Figure 4 shows a wafer from our modified process, where we did not get slip dislocations.

In order to compare the electrical characteristics of our components with earlier results [1], we have fabricated a number of different devices with three different RESURF terminations. The first termination is implemented with a constant doping profile and stretches over 120 μm. The second and third termination have the same dimensions (80 μm), but differ according to their doping profiles. The former has a step doping profile, whereas the latter has a graded doping profile. The RESURF terminations have been designed to withstand voltages $>$500 V, as can be seen in fig. 5. We have varied the gate length of our transistors between 8 μm and 12 μm and the width between

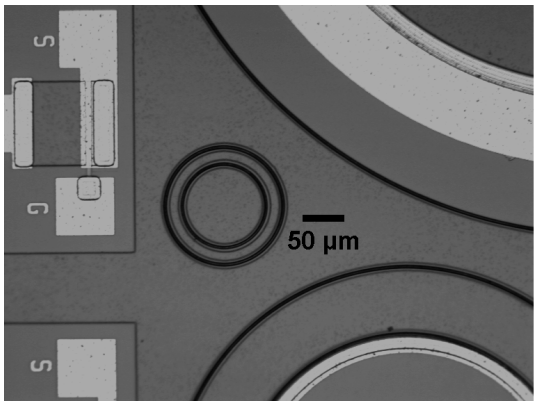

Figure 4. This picture shows a wafer of our modified process. Sliding planes do not emerge, because the trenches are not exposed to high temperature steps.

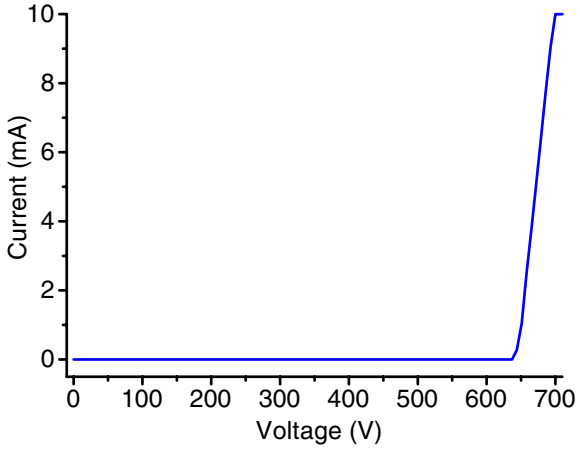

Figure 5. Breakdown of a RESURF-n$^-$-diode occurs at 630 V.

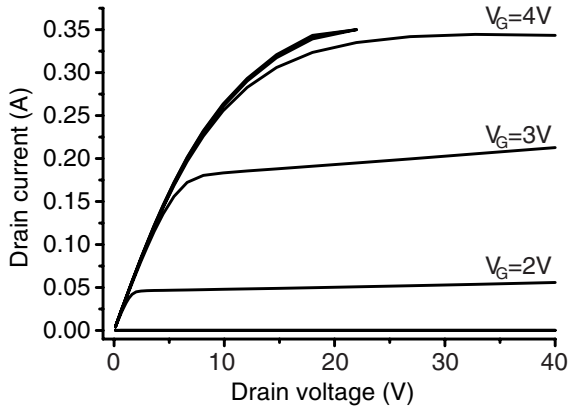

Figure 6. IV-characteristics of a 30 mm transistor with gate voltages 0-7 V, step 1 V.

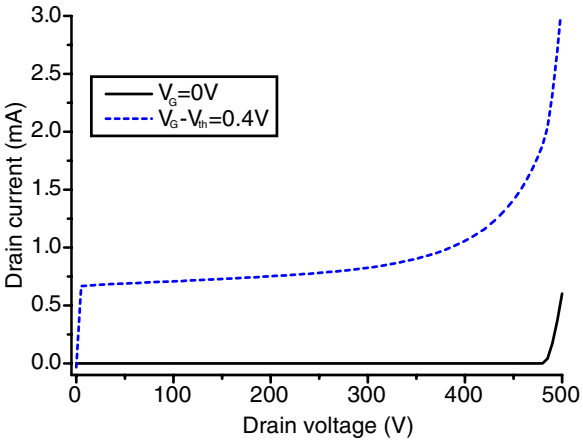

Figure 7. Breakdown of a typical VDMOS at 480 V.

18.8 mm and 40.2 mm. The measured IV-characteristics of a 30 mm device with a gate length of 12 μm is shown in fig. 6. The specific on-resistance is 0.17 Ωcm^2 and the breakdown voltage is 480 V (see fig. 7). If we compare the breakdown voltage with the breakdown voltage of the RESURF-n$^-$-diodes, we can conclude that the breakdown of the transistors occurs at the curvature of the p-base. Table 1 summarizes the electrical characteristics of the different devices. The breakdown voltages are not affected by the gate length. The influence of the different RESURF terminations on the specific on-resistance can clearly be seen from this table.

In fig. 6 a quasi-saturation behavior can be seen for higher gate voltages. This is caused by the saturation of the electron drift velocity in the drift region, which leads to a higher voltage drop in the drift region between the p-base areas under the gate and lowers the potential at the drain end of the channel region [7]. A similar effect has been observed for lateral DMOS transistors [8]. This effect is more pronounced for devices with shorter gate length as can be seen from fig. 8. We can see that the transconductance of the devices with shorter gate drops to low values at lower gate voltages compared to the devices with longer gate. And even though the former devices are wider than the latter do they have lower saturation currents.

5. Conclusion

We have presented vertical high voltage devices on thick SOI with a modified process flow. The creation of sliding planes has been avoided successfully by moving the trench etch at the end of the process. By doing so the trenches are not exposed to high temperature steps which trigger the formation of these defects. The electrical characteristics of the fabricated devices have not been altered by these process modifications.

Table 1. Specific on-resistance of VDMOS transistors on thick SOI

Gate length (μm)	Width (mm)	$R_{on,spec}$ (Ωcm^2)	RESURF
12	33.8	0.16	step/graded
12	30	0.17	step/graded
12	22.8	0.22	constant
12	18.8	0.23	constant
10	35.3	0.16	step/graded
10	31.7	0.16	step/graded
10	24.3	0.22	constant
10	20.9	0.21	constant
8	40.2	0.15	step/graded
8	33.8	0.16	step/graded
8	28.2	0.22	constant
8	22.7	0.21	constant

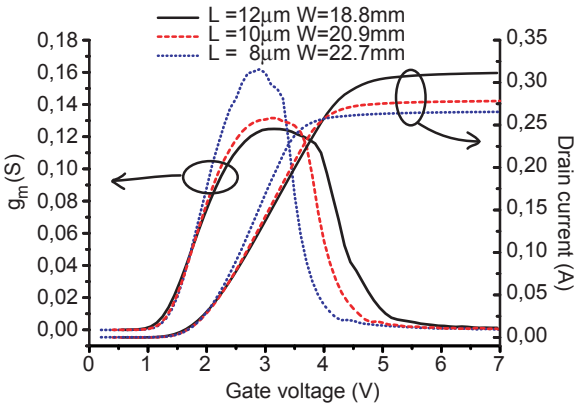

Figure 8. Comparison of devices with different gate lengths. The devices with 8 μm gates have lower saturation currents than the devices with larger gates due to quasi-saturation.

6. Acknowledgment

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