A MOS Nanogap Device Structure for Characterisation of Nano-scale Objects

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Abstract

A silicon - silicon dioxide – silicon nanogap device structure has been investigated as a potential candidate to use for studying electrical properties of species in the nanometer regime. The structure, based on the Metal-Oxide-Silicon Field-Effect Transistor (MOSFET) gate stack, demonstrates a possible route to the construction of an anchoring element for interfacing CMOS and nano-scale objects. After gate stack formation, the structure is subsequently anisotropically etched to expose the stack of polycrystalline silicon-silicon dioxide-silicon substrate to any foreign element desired. The nanogap consisting of the silicon dioxide film can be controlled down to 2 nm in thickness. Its electrical characteristics show very low as-grown leakage currents, dominated by tunnelling through the oxide. When being subjected to exposure to foreign elements, the structure displays a high sensitivity for such treatments in its current-voltage characteristics. We propose this structure as a potential candidate to use for studying electrical properties of species in the nanometer regime.

1. Introduction

The formation of nanogaps to facilitate studies of electrical conduction in nanoscale elements such as molecules or carbon nanotubes normally employs gold contacts, which display excellent contacting properties and chemical stability. The formation and control of such a nanogap is however very difficult [1]. In a wider perspective such contacts and nanogaps will not constitute a viable route for connecting nano-scale objects, such as molecules, to silicon for future hybrid circuits. In this study we present a simple method to form a nanogap between two silicon contacts. The basic structure we use is the gate stack of the Metal-Oxide-Silicon Field-Effect Transistor (MOSFET). By etching through the gate stack the silicon dioxide nanogap is exposed to any foreign element desired. In this study, a variety of samples were investigated, including both highly doped and medium doped silicon materials and structures with different silicon dioxide thickness.

2. Experimental details

The starting material for device manufacturing are standard n- or p-type <100> silicon wafers. Some wafers were given highly doped surface regions before oxide growth. The high doping is to minimise effects of surface depletion layers in the silicon. During subsequent oxidation, the oxide growth will be enhanced for high substrate doping. We focus on three samples in this report numbered 5, 6 and 7 in a batch called Tunnel Oxide as Molecular Interface (TOMI). In all these three cases 1-10 Ωcm n-type substrates were used. Sample type 5 and 6 received highly doped n^+ surfaces to a surface resistance lower than 1 Ω/square before nanogap oxide growth. The thin oxide growth was conducted at 800 °C in dry oxygen for 40 minutes for wafers 5 and 7 resulting in approximately 14 and 7 nm oxide thickness respectively, where the difference is

due to the higher doping of wafer 5. Wafer 6 received oxidation at 800 °C for 6 minutes, yielding an approximately 5 nm oxide. The oxides were given a post-oxidation anneal in Ar/H_2 at 900 °C for 5 minutes to improve oxide quality. Polycrystalline silicon was deposited using Low Pressure Chemical Vapour Deposition (LPCVD) technique and the poly-Si gate electrode was diffusion doped with phosphorous to a concentration of almost 10^{20} cm^{-3}. The structure is subsequently anisotropically etched to expose the stack of polycrystalline silicon-silicon dioxide-silicon substrate to any foreign element desired. In Figure 1 the device structure is shown in a cross-section SEM-picture. The polysilicon gate has been covered with aluminium, and a reactive ion etch has been employed to expose the front side (leftmost edge in Figure 1) with its silicon-oxide-silicon stack.

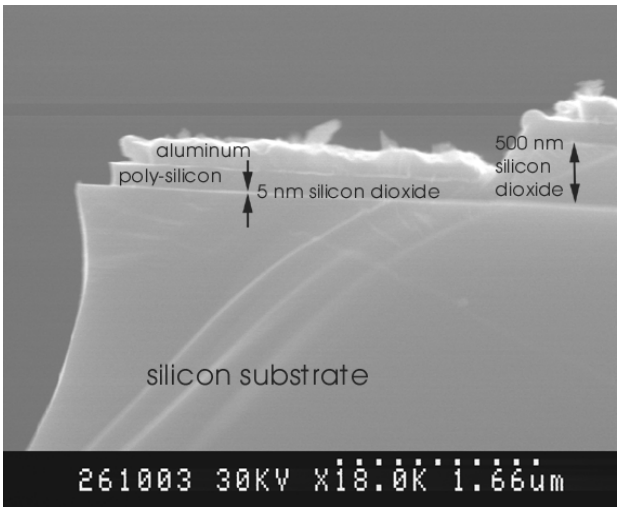

Figure 1. Cross-section of device structure. The thin silicon dioxide layer acts as an insulating barrier that can be short-circuited by externally applied species.

3. Experimental results and discussion

The electrical properties of the pristine device structure, the properties after exposure to diluted HF mixtures as well as the properties of the nanogap device structure after exposure to nano-objects dissolved in solvents were investigated using normal electronic device characterisation set-ups. Figure 2 shows current-voltage characteristics for the thickest oxides (14 nm, wafer 5) without any exposure to HF or nano-objects. As can be seen from Figure 2 the leakage current in the as-manufactured devices is low. These devices display Fowler-Nordheim tunnelling current at high enough bias, with good breakdown characteristics (>10 MV/cm). This is shown for different devices by the dot-dashed curves of Figure 2. HF-etching and exposure to CdSe nanocrystals in a toluene solution gives an order of magnitude impact on the current, as shown by the solid lines (HF-etching) and dashed curves (nano-crystals) in Figure 2.

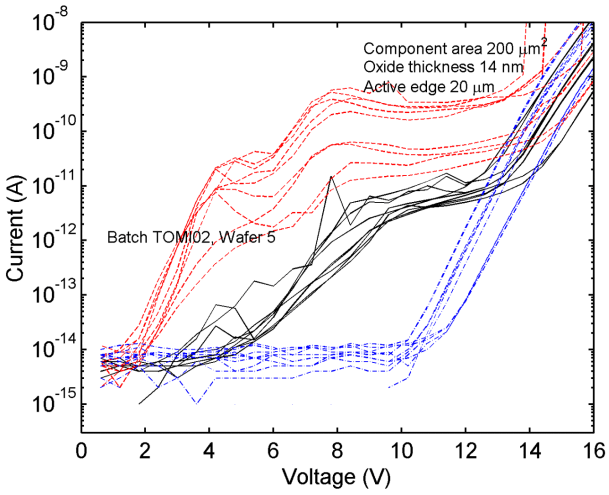

Figure 2. Current *vs.* voltage characteristics for 14 nm nanogap devices with n^+-substrate. The low current, dot-dashed curves are pristine devices, solid lines are HF-etched and the feature rich, dashed curves are after exposure to nanocrystals dissolved in toluene. The I-V characteristics are clearly sensitive to surface treatments.

Wafer 6 of the batch has an oxide thickness of approximately 5 nm. These devices show an even stronger sensitivity to surface treatment as can bee seen in Figure 3. The results of Figures 2 and 3 clearly show that the leakage current from the polycrystalline gate electrode to the substrate is largely influenced by the surface treatment, whether it is an HF-dip or exposure to nanocrystals. All devices reported in Figures 2 and 3 were exposed to etching in a $HF:H_2O$ solution before immersion in the solvent containing the nanocrystals. Although the effect is clear it is not, at this stage, completely understood if the current *vs.* voltage curves obtained after exposure to nanocrystals constitutes the true characteristics of the nanocrystals on silicon.

Figure 4 reveals one serious problem with the design and measurements in air; the current-voltage characteristics are not stable during continuous

measurements. The curves of Figure 4 refer to measurements on a device of sample type 7, not being highly doped before oxide growth. The oxide thickness of the sample is approximately 7 nm.

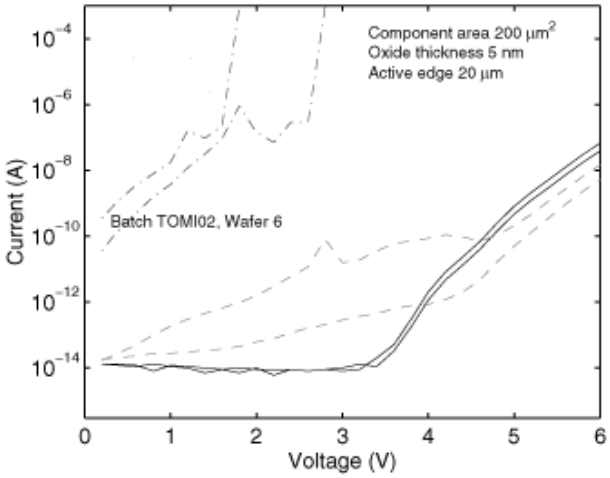

Figure 3. Current-voltage characteristics for n^+-type substrate devices with 5 nm oxide nanogap without any treatment (solid), after an HF-etch (dashed) and after subsequent exposure to nanocrystals in toluene (dot-dashed).

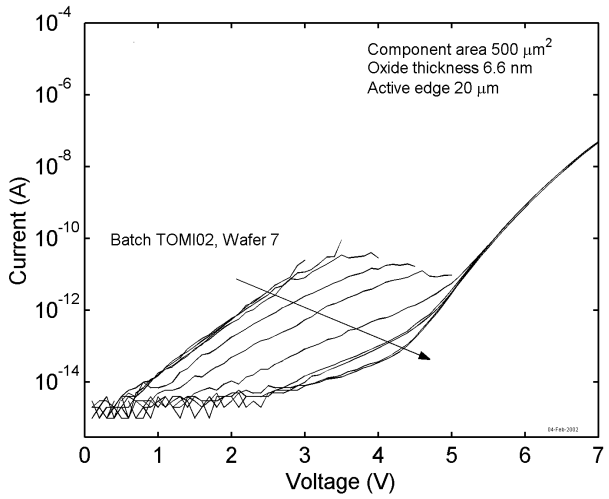

Figure 4. Consecutive sweeps of the voltage gives a reduction in current approaching the characteristics of the pristine device. Oxidation of the surface is a possible explanation.

The device from wafer 7 has been exposed to a nanocrystal solution, but after putting high enough bias on the device, the current goes back to a pristine state, possibly due to oxidation of the silicon surface during measurements. This observation is further supported by the fact that measuring in air ambient gives significantly higher low-voltage leakage currents than measuring in helium for HF-etched device structures. This is demonstrated in Figure 5.

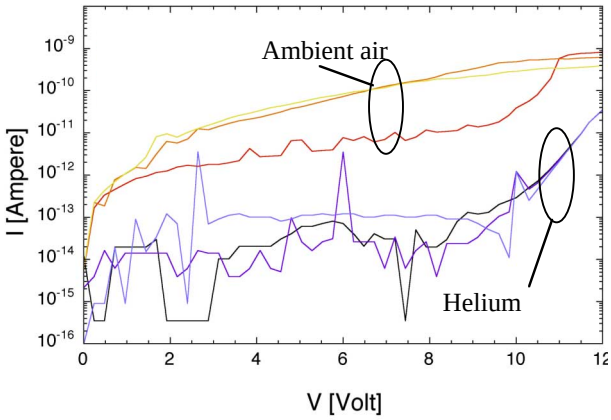

Figure 5. Measuring in air ambient gives significantly higher low-voltage leakage currents than measuring in helium for HF-etched device structures.

This instability of the silicon contact shows one of the problems related to using bare silicon as contact electrode. Instead the silicon surface should be terminated or covered with a CMOS-compatible material allowing stable contact formation to the nano-objects. This issue besides forming good chemical/electrical contact with the appropriate nanoelements are obvious challenges for future work.

Although the devices presented here had nanogaps being 5 nm or larger, structures with nanogaps down to approximately 2 nm can easily be controlled. The limit at 2 nm is set by the rapid increase in direct tunnelling current across the insulator below 2 nm in thickness.

4. Conclusions

A silicon nanogap device structure has been studied as a potential candidate to use for studying electrical properties of species in the nanometer regime. The structure is based on MOSFET gate stack and allows the formation of nanogap consisting of silicon dioxide film down to 2 nm in thickness. The electrical characteristics of the manufactured structures show very low as-grown leakage currents, dominated by tunnelling through the oxide. When being subjected to exposure to foreign

elements, the structure displays a high sensitivity for such treatments in its current *vs.* voltage characteristics. We propose this structure as a potential candidate to use for studying electrical properties of species in the nanometer regime. Further work is needed on controlling oxidation of the silicon surfaces.

5. Acknowledgements

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6. References

[1] M. A. Reed, "Molecular-Scale Electronics", *Proceedings of the IEEE*, **87**, 652 (1999).