Optimising High-Voltage Devices in a Smart Power Technology, using the RESurF-effect and TCAD.

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Abstract

Smart power technologies, i.e. the monolithic integration of high voltage devices in a digital sub-micron CMOS technology, have become a popular topic. In developing such a technology, the aim is to optimise the high-voltage devices for a maximum off-state breakdown voltage V_{break} and a minimum on-state specific resistance R_{on}.Area. This paper contributes to this art in three different ways. A general usable methodology is formulated to optimise the breakdown voltage using TCAD (Technology CAD). A new RESurF (Reduced Electric Surface Field) effect is reported for the special case $N_{sub} \geq N_{epi}$, which is typical for high voltage devices implemented in a digital CMOS technology and finally, a method is shown to increase the breakdown voltage of a RESurF device above its vertical plane junction breakdown.

1. Introduction

TCAD simulations have become an indispensable tool for the study, design and optimisation of smart power technologies. Besides being faster and cheaper than silicon experiments, they allow insight in the distribution of the internal electrical quantities during device operation. Although this information is very valuable for designing competitive high-voltage devices [1,2], the optimisation is often hampered by the complexity of the two- or three-dimensional internal field distributions.

In a first part of this article, a methodology is formulated that transforms the complex two- or three-dimensional field distribution during breakdown to a more familiar one-dimensional situation, hereby greatly facilitating the optimisation of high-voltage devices, using TCAD.

The RESurF technique on the other hand, is one of the most widely used methods for the design of high-voltage, low on-resistance devices. Although original conceived to reduce the surface electric field in a planar device, its concept is transferable to two-dimensional field manipulation in general. The RESurF technique is well understood and described in literature for dedicated high-voltage technologies [3, 4 and references herein]. In a smart power technology however, at least part of the process layers are optimised for digital design. This leads to some new observations, which are, to the best of our knowledge, not reported in literature yet. These new phenomena are demonstrated and explained using TCAD simulations on a dedicated structure. Finally, the preceding optimisation procedure is applied to increase the breakdown voltage of the RESurF structure above its plane junction breakdown. This is not possible in a dedicated high-voltage technology and therefore not reported before. All three results, described in this paper, are immediately applicable in designing high-voltage devices in smart power technologies.

2. Optimising impact ionisation related breakdown

A guideline is formulated to optimise the breakdown voltage in a general device, based on the following considerations. For an arbitrary device under impact ionisation breakdown, there exists at least one path L for which the ionisation integral becomes unity [5]

$$\int_0^L \alpha_p(E)\exp\left[\int_0^s (\alpha_n(E)-\alpha_p(E))dx\right]ds = 1$$

with α_n and α_p the impact ionisation coefficient for electron and holes, respectively:

$$\alpha_{n,p}(E) = A_{n,p}\exp\left(-\frac{B_{n.p}}{E}\right) \quad [1/cm]$$

According to Maxwell's law, the breakdown voltage supported by the device equals the integrated electric field along this 'ionisation integral=1' path L:

$$\int_0^L \bar{E}\cdot\bar{ds} = \int_0^L |E|\cdot ds = \text{ Breakdown Voltage } [V]$$

Because the impact ionisation coefficient α_n and α_p are exponential functions of the electric field, only the peak of highest electric field along the 'ionisation integral=1' path is mostly responsible for the breakdown condition. The following simple guideline is therefore suggested:

To optimise the breakdown voltage, the device needs to be engineered in such a way that the integrated area of the electric field along the 'ionisation integral=1' path *is as large as possible. This is obtained by either decreasing the slope of the electric field peak or by introducing as many peaks as possible. The optimum breakdown voltage is usually obtained when all peaks are equal in height, as this corresponds to a maximum integrated surface.*

Unfortunately, the 'ionisation integral=1' path is a theoretical concept and cannot be calculated during TCAD simulations. The average spatial path that the carriers follow during breakdown is therefore suggested as an approximation for the 'ionisation integral=1' path. This path is called the *mid-current line* and is easily calculated from the simulated current flow-lines during breakdown.

This method reduces the complex two- or three-dimensional field distribution problem of a device to a more familiar one-dimensional problem and is recently successfully applied by the authors to optimise nDEMOS devices in a 0.35µm smart power technology [6].

The methodology is further demonstrated at the end of this paper for a RESurF-device in the special case of $N_{sub} \geq N_{epi}$.

3. The RESurf effect

The simulated cross-section of Figure 1 shows the outline of the RESurF-device as originally conceived by J. A. Appels [7]. The principle is well known: the vertical p-epi/n-sub junction depletes the epitaxial layer and modifies the depletion region of the planar n^+/p-epi junction, increasing its breakdown. The breakdown voltage is a function of the epitaxial thickness t_{epi} and lateral spacing l. This is simulated in Figure 2.

For a large lateral spacing l, i.e. line ABCD, the breakdown has an optimum as a function of the epitaxial thickness t_{epi}. See Figure 3. This optimum breakdown voltage is determined by the vertical p-epi/nsub junction breakdown. In a dedicated high-voltage technology, the substrate is always doped much lower than the epitaxial layer. Indeed, for $N_{sub} << N_{epi}$, the breakdown voltage is determined by the low doped substrate and the on-resistance by the high doped epitaxial layer. This separation of regions, that determine the on- and off-state, allows a RESurF device to obtain a good V_{break}-R_{on}.A trade-off.

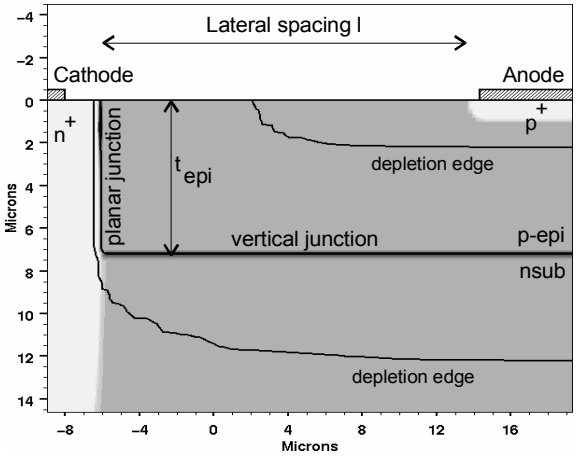

Figure 1. Simulated RESurF device for $N_{sub}=N_{epi}=4e15cm^{-3}$

4. The RESurF effect for $N_{sub} \approx N_{epi}$

In the case of a high-voltage device implemented in a digital CMOS technology, the available wells are optimised for digital devices and N_{sub} is no longer necessarily smaller than N_{epi}. This is for example the case in [8].

The RESurF structure of Figure 1 is therefore simulated for $N_{sub}=N_{epi}=4e15cm^{-3}$, which is a realistic situation in a digital CMOS technology. It is found that for the optimum epitaxial thickness t_{epi}, i.e. line CEF in Figure 2, the breakdown has an optimum as a function of the lateral spacing l. See Figure 4.

For a large lateral spacing l, the breakdown is determined by the breakdown of the plane n-sub/p-epi junction under the anode contact, i.e. at 160 V.

For smaller lateral spacing l, the breakdown voltage increases above the plane breakdown value of the vertical junction. Comparing the potential lines and mid- current line in point C and E in Figure 5 and 6, respectively, explains this. In point E, the planar junction influences the depletion region under the anode and as a result the potential lines are curved. This results in a rerouting of the mid-current line, a smaller slope of the electric field and a larger integrated area along the mid-current line. This is shown in Figure 7. In other words, this is a RESurF effect where the lateral junction also influences the vertical junction.

For a smaller spacing, lateral n^+pp^+ punch-through eventually decreases the breakdown voltage.

No report of this is found in literature. There are several reasons for this. In the analytical model, on which most articles [3, 4 and references herein] are based, the modified poisson equation incorporates the modulation of the vertical junction on the planar junction, but never the modulation of the planar junction on the vertical junction. Furthermore, the width of the anode is taken infinite to obtain an easy boundary condition. All articles also report about devices where the substrate is much lower doped than the epitaxial layer to benefit as much as possible from the RESurF effect. In these devices, the

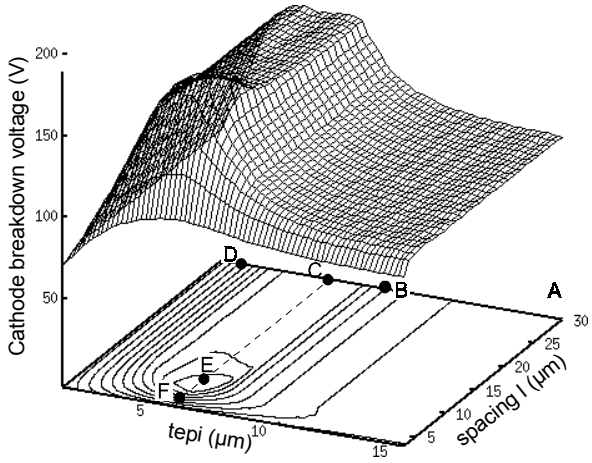

Figure 2. Simulated breakdown as a function of tepi and l for $N_{epi}=N_{sub}=4e15/cm^3$.

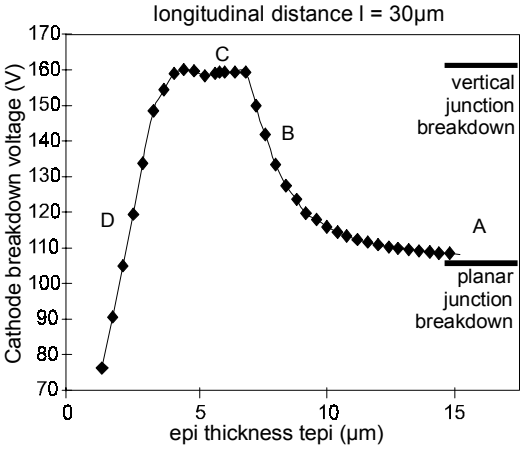

Figure 3. Simulated breakdown as a function of t_{epi} for a large lateral distance l.

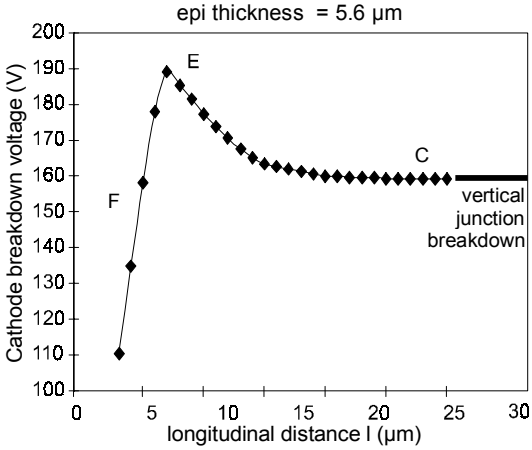

Figure 4. Simulated breakdown as a function of longitudinal distance l for an optimal epitaxial thick-

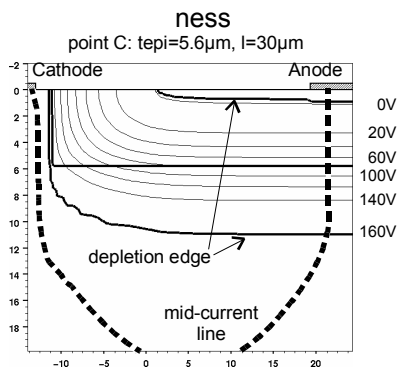

Figure 5. Simulated potential line distribution and mid-current line for key point C.

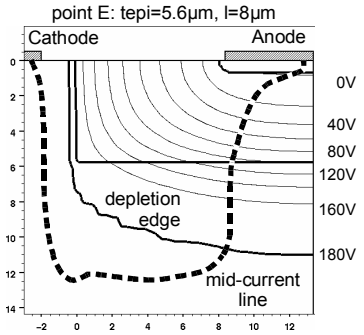

Figure 6. Simulated potential line distribution and mid-current line for key point E.

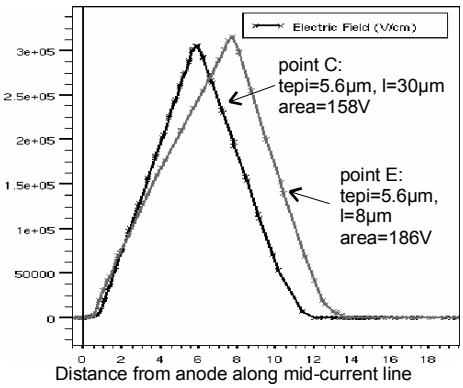

Figure 7. Electric field along the mid-current line of figure 5 and 6, respectively.

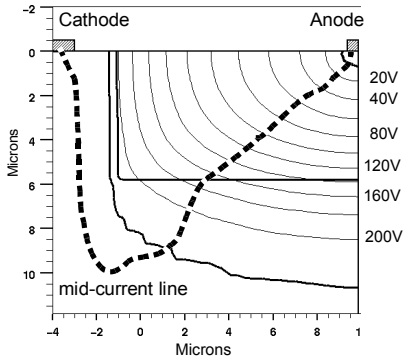

Figure 8. Simulated potential line distribution and mid-current line for an optimised anode contact.

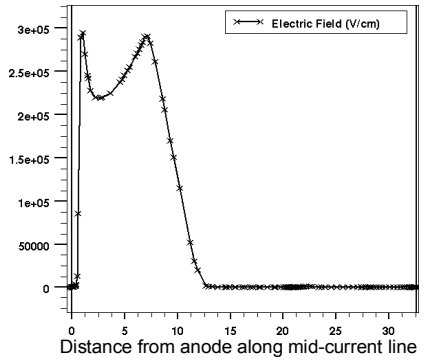

Figure 9. Electric field along the mid-current line of Figure 8.

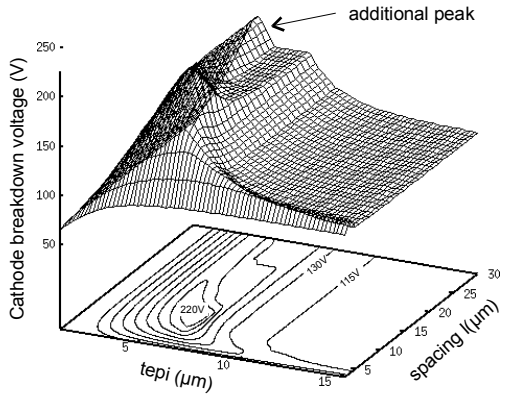

Figure 10. Simulated breakdown using the curvature effect to increase the breakdown voltage.

above mentioned phenomena do not appear because the depletion layer extends mostly in the substrate and the influence of the planar junction on the depletion layer in the epi layer is negligible.

As the specific on-resistance $R_{on}.A$ is a square function of the lateral distance l, an optimum lateral distance l exists for an optimum V_{break}-$R_{on}.A$ figure. This can be applied in the design and optimisation of high-voltage devices in a smart power technology.

5. Optimising the anode contact

Figure 7 shows the electric field along the mid-current line for the RESurF structure with an optimum epitaxial thickness. The previous formulated optimisation procedure can now be applied to increase the breakdown voltage.

Because the process layers are usually fixed by the digital design constraints in a smart power technology, the doping levels and thus the slope of the electric field cannot be modified.

An alternative solution is therefore to introduce a second electric field peak along the mid-current line by forcing the mid-current line through the corner of the p^+p-anode contact. See Figure 8. By optimising the width and doping gradient of the contact, both peaks can be made equal, see Figure 9, and the breakdown voltage is optimised above the plane pn^+ junction breakdown. Figure 10 clearly shows the extra peak. The maximum simulated voltage equals 220V, which is a significant increase compared to the original vertical plane breakdown value of 160V in Figure 2. This effect has not been reported before.

6. Conclusion

A general usable methodology is formulated to optimise the breakdown voltage using TCAD (Technology CAD). This method reduces the complex two- or three-dimensional field distribution problem of a device to a more familiar one-dimensional problem, which greatly simplifies the study of high-voltage devices. It is explained that in a smart power technology, N_{sub} is no longer necessarily smaller than N_{epi} for a RESurF device. This constraint leads to a new observation, which is demonstrated and explained using TCAD. Finally, using the optimisation procedure, it is demonstrated that in the special case of $N_{sub} \geq N_{epi}$, the anode contact can be optimised to obtain a breakdown higher than the plane vertical junction breakdown.

All these results are immediately applicable in the design and optimisation of high-voltage devices in smart power technologies.

8. References

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