Pseudo Dynamic Gate Design based on the Resonant Tunneling-Bipolar Transistor (RTBT)

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Abstract

In this paper the design and measurement results of RTBT monosatble-bistable transition logic element (MOBILE) gates are analyzed. By taking advantage from the multi-state behavior of resonant tunneling devices (RTD) the logic depth and the circuit complexity per logic function is reduced at the gate level. Due to the combination of a three terminal device (HBT) with the two terminal RTD the vertical RTBT has enhanced driving capabilites and is a promising candidate as a precursor for future nano-scaled ULSI circuits.

1. Introduction

Resonant tunneling devices play an important role as precursors for future nano-scaled ULSI circuits because at present they are the most mature type of quantum-effect devices. Compared to single electron transistors and more advanced quantum dot architectures resonant tunneling devices are already operating at room temperature. Figure 1 and 3 show the measured I-V characteristics of the RTBT66-M1882A and its layer structure. The technological advances, such as the development of a III-V Large Scale Integration Process [7], and the demonstration of a Si/$Si_{0.5}Ge_{0.5}$/Si resonant interband tunneling diode [8], are a motivation for circuit designers to investigate digital logic families and memory cells [3, 4].

The basic idea behind resonant tunneling device circuit design is to exploit the nonlinear I-V characteristics with the typical negative differential resistance (NDR) region. In this context the isolation of the gate input and output signals is of fundamental relevance and has motivated the implementation of different three terminal tunneling devices. The common feature of these different devices is the combination of electronic amplification and NDR. In addition to the technologically oriented research a further prerequisite for nano-scale integration is the investigation of suitable logic families, architectures and the development of a design framework [6, 1].

In recent years high speed logic families based on the monostable-bistable transition logic element (MOBILE) have been proposed for tunneling devices [2, 9]. The

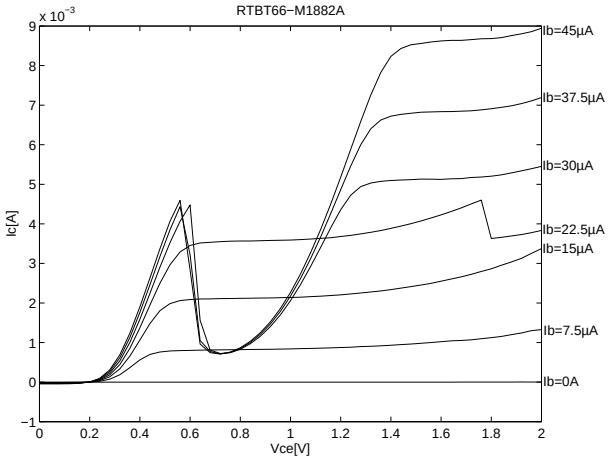

Figure 1. Measured I-V characteristics of the RTBT66-M1882A.

RTBT MOBILE gate is a pseudo-dynamic, clocked logic gate and consists of two resonant tunneling devices which are operated in a monostable and bistable state depending on a pulsed clock signal. The term pseudo-dynamic refers to the special circuit style in the sense that the logic transition of the gate is controlled by a clock similar to dynamic circuits. But in contrast to dynamic circuits where the logic state is represented by the electrical charge on a capacitor, RTBT MOBILE circuits are in a static, self-stabilizing state due to the inherent bistability of the devices. Consequently, they are more robust against charge leakage and pre-charging is unnecessary.

2. RTBT MOBILE

Figure 2 shows the monostable-bistable transition of an RTBT input stage. The areas of the RTD's are chosen so that the peak current of the load RTD_1 is larger than the current of $RTBT_{clck}$, but smaller than the current sum of $RTBT_{clck}$ and $RTBT_a$. From this follows that the gate switches to the logic low voltage V_L if the input $RTBT_a$ is off. If $RTBT_a$ is on, the current sum of $RTBT_{clck}$ and $RTBT_a$ exceeds the current of the load RTD_1 and the gate switches to the logic high voltage V_H.

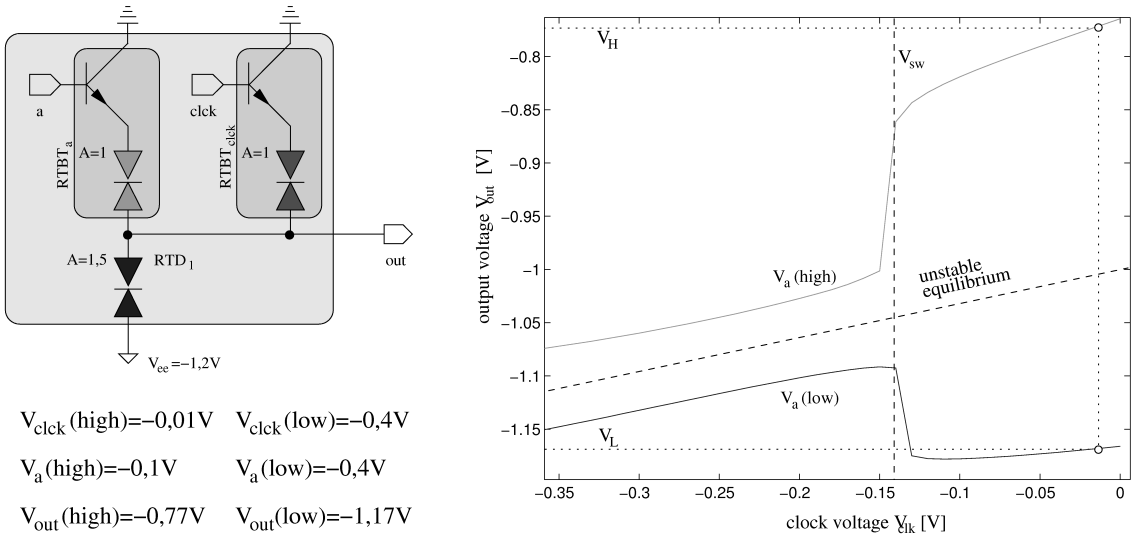

Figure 2. Monostable-bistable transition of an RTBT input stage

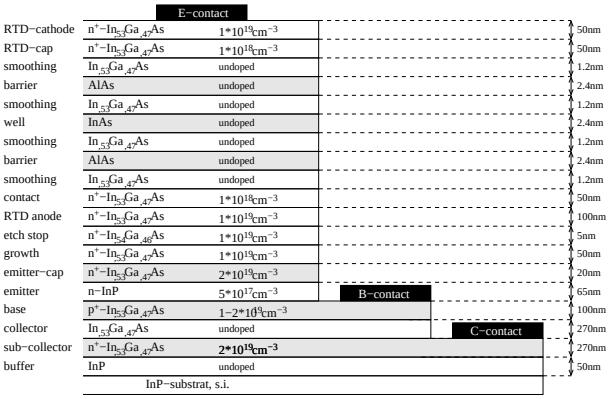

Figure 3. layer structure of the InP-based RTBT

The threshold is determined by the peak current of RTD_1 while the input weight is represented by the peak current of $RTBT_a$. An input weight of $w = 1$, for example, is characterized by the minimum square section of the resonant tunneling structure in the emitter branch of the HBT. This scales the peak current to its minimum and is symbolized by $A = 1$. The gate switches from the monostable state into the bistable state if the clock voltage V_{clck} drives RTD_1 over its peak voltage. The bistable states represent the two logic levels 0 (low) and 1 (high). At the switching point the gate follows the upper or lower gate characteristics depending on the input voltage V_a. The peak voltage V_P and the clock voltage V_{clck} is $0.18\,V$, and $-0.1V$ respectively. This leads to a voltage swing of $\Delta V = 0.4V$. During the active clock phase the voltage drop $V_{clck} - V_{be} - V_{ee} = 0.53V$ across the two resonant tunneling devices lies between $2V_p = 0.36V$ and $3V_p = 0.54V$ and drives the MOBILE from the monostable into the bistable state.

Since the heterojunction bipolar transistor (HBT) is a current driven device we use an emitter-follower configuration. This keeps the input impedance high and the transistor is not operated in saturation. On the contrary to the differential output buffer proposed in [1], in this article we achieve negative input weights and a input-output compatible I-V characteristics at the gate level by applying emitter-follower buffer (fig. 4 b)) with negative current feedback. As we will see in the subsequent chapter this approach consumes less power than a differential output buffer.

As the MOBILE is a clocked and current controlled gate with integrated latch function it suites well to the also current controlled RTBT. Furthermore, the lack of a reliable enhancement-type HFET is no issue for the RTBT because of its build in potential that depends on the base and emitter bandgap.

3. RTBT MOBILE NOR Gate

A regenerative I-V characteristics at the gate level is of fundamental relevance for any logic family and strongly depends on input-output compatible voltage levels of the input and output [5]. As an example, the RTBT MOBILE NOR gate is completed by an emitter-follower (fig. 4 b)). By applying a negative current feedback the temperature dependence of HBT_{out} has been reduced and saturation has been omitted. This output buffer version only offers a single-ended output in comparison to the in [1] proposed differential buffer. The output voltage can approximately expressed by:

$$V_{out} \approx V_{gnd} - \frac{R_1}{R_2}\left(V_{ee} - V_m - V_{be}\right) \qquad (1)$$

It follows that the logic voltage levels of the unloaded output can be resumed as:

$$V_{out} = V_{gnd} \qquad \text{(logic 1)}$$

$$V_{out} = V_{gnd} - \tfrac{R_1}{R_2}\left(V_{ee} - V_m - V_{be}\right) \qquad \text{(logic 0)}$$

Figure 5 shows the microfoto of the RTBT MOBILE NOR gate. The wiring has not been optimize at the early stage of test circuit. Approximately, the averaged current at the switching point correspondence to the half peak current. Assuming a similar voltage swing $\Delta V \approx 2V_P =$

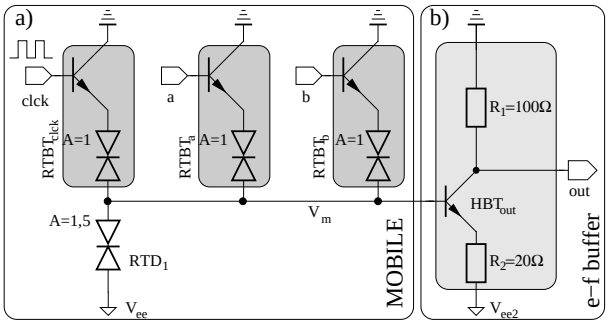

Figure 4. RTBT MOBILE (a) NOR gate with emitter-follower buffer (b)

$0.4V$ like in [1] the peak current of the emitter-follower is revealed by $I_{EF} \approx \frac{400mV}{100\Omega} = 4mA$. As a figure of merit for the switching speed the speed-index $SI = \frac{I_P}{C_{RTD}}$ can be approximated with respect to the parasitic capacitances for a fan-out of two by $SI_{EF} \approx \frac{4mA/2}{40fF} = 50V/ns$.

With reference to the first order approximation of the underlying scaling law (table 1) the MOBILE speed-index can be assumed to $SI_{MOB} = 7.6\,V/ns$. Due to $\Delta V_m = 0.4V$ and $\Delta V_{out} = 0.3V$ the intrinsic gate delay is about $47\,ns$. Therefore, the estimation of $f_{clk} = 1/(10_{int}) \approx 2.1\,GHz$ gives clear evidence that the RTBT MOBILE in combination with the emitter-follower is capable of operation frequencies in the giga hertz regime.

In contrast to the differential buffer used in [1] the fan-out of the emitter-follower buffer can only slightly be increased by enlarging I_{ee2}. The emitter-follower is designed to drive the following stage and is overloaded by the characteristic impedance (50 Ω) of the measurement setup. Therefore, the correct logic function (fig. 6) could only be traced up to a clock frequency of $93\,MHz$ at $I_{EE2} = 8\,mA$.

4. Power Dissipation

With reference to [1], the power dissipation during switching P_{MOBsw}, the static power dissipation $P_{MOBstat}$ and the dynamic power dissipation P_{MOBdyn} of the RTBT MOBILE can be approximated:

$$P_{MOBsw} = 2\overline{I_{SW}}V_{SW}\frac{t_{CR}}{T} \approx \frac{3}{5}I_P V_P \qquad (2)$$

and

$$P_{MOBstat} = I_V|V_{EE}|\frac{t_{CH}}{T} = I_V(2,5V_P + V_{be})\frac{2}{5} = I_V(V_P + \frac{2}{5}V_{be}) \approx \frac{3}{5}V_P I_P \qquad (3)$$

and

$$P_{MOBdyn} = C_M\overline{V_m^2}f \approx C_M V_P^2 f \qquad (4)$$

The share of the emitter-follower buffer in the static power dissipation dependence on the logic state of the gate. For the logic 1-level HBT_{out} is for all practical purposes quiescent and does not consume any power. On the contrary, it can be stated for the logic 0-level that there is a static current of $I_{EF} = 4mA$. The averaged current $\overline{I_{av}} = \frac{1}{2}I_{EF} \approx \frac{1}{2}I_P$ is responsible for the static power dissipation of the emitter-follower buffer:

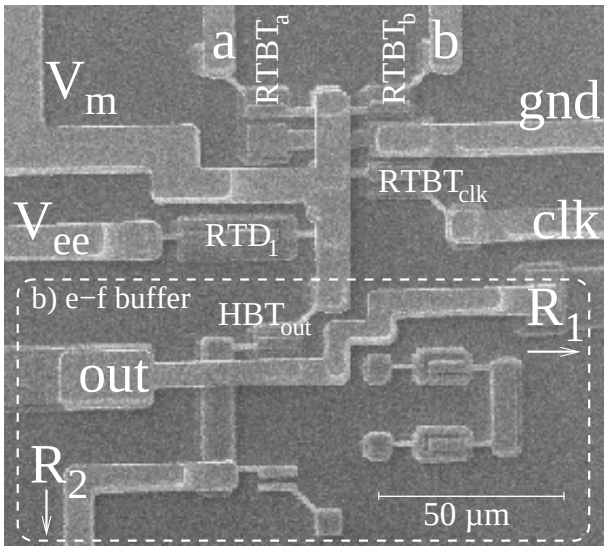

Figure 5. microfoto of the RTBT MOBILE NOR gate ($A \approx 163\mu m \cdot 145\mu m$) incl. emitter-follower buffer (b)

Table 2. Comparison between the differential buffer [1] and the emitter-follower buffer in terms of power dissipation

term	parameter	unit
stat. pow. dif.	$P_{DIFstat} = \frac{28}{5}\ I_P\ V_P$	μW
stat. pow. e-f	$P_{EFstat} = \frac{12,5}{5}\ I_P\ V_P$	μW
dyn. pow. dif.	$P_{DIFdyn} =$	
	$C_{Diff-L}\lvert V_{EE}\rvert\Delta V_{out} f$	μW
dyn. pow. e-f	$P_{EFdyn} = C_{EF-L}\lvert V_{EE}\rvert\Delta V_{out} f$	μW

$$P_{EFstat} = |V_{EE}|\overline{I_{av}} \approx (2,5V_P + V_{be})\frac{1}{2}I_P \approx 2,5V_P I_P \qquad (5)$$

The dynamic power dissipation of the emitter-follower buffer P_{EFdyn} depends on the clock and its related charging and discharging of all involved capacitances. Assuming a fan-out of two and an approximated load capacitance of $C_L = C_{sc} + 2(C_{sc} + C_{de})$, the dynamic power dissipation can be expressed like:

$$P_{EFdyn} = C_L|V_{EE}|\Delta V_{out} f \qquad (6)$$

The emitter-follower buffer reduces the static power dissipation by 55% in comparison to the differential buffer described in [1], since the unloaded buffer is in a quiescent state for the logic 1-level (table 2).

5. Conclusion

In this paper we have investigated a new circuit design strategy that bases on the RTBT MOBILE. Measurement results prove correct circuit operation and regenerative i/v characteristics at the gate level. A first order estimation gives clear evidence that the RTBT MOBILE in combination with the emitter-follower buffer is capable of operation frequencies in the giga hertz regime while the static power consumption is reduced by more than a factor of

Table 1. Speed-Index of the RTBT MOBILE in connection with the emitter follower

term	**parameter**	**unit**
MOBILE load capacitance	$C_M = C_{rtd} + C_{sc} + C_{de} + C_{se}$	fF
MOBILE speed-index	$SI_{MOB} = I_P \ / \ 2C_M$	V/ns
e-f cap. (Fan-out 2)	$C_{EF-L} = C_{sc} + \ 2(C_{sc} + C_{de})$	fF
e-f speed-index	$SI_{EF} = \frac{I_{EE}}{2C_{EF-L}} \approx \frac{I_P}{2C_{EF-L}}$	V/ns
intr. gate delay	$t_{int} = \frac{\Delta V_M}{SI_{MOB}} + \frac{\Delta V_{out}}{SI_{DIF}}$	ns
clock cycle	$T = 10\ t_{int}$	ns

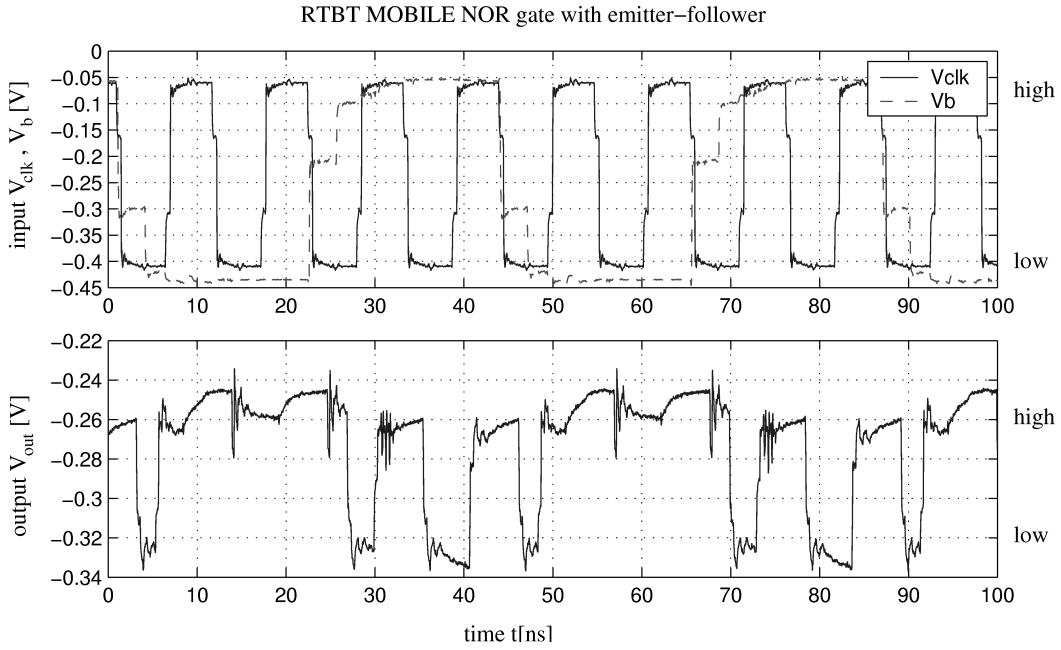

Figure 6. measurement results of the RTBT MOBILE NOR gate ($V_a = -0.4\ V$, f(V_{clk})= 93 MHz)

two in comparison to the RTBT MOBILE in connection with the differential buffer.

6. Acknowledgment

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