

TCAD Based Design Methodology for Substrate Current Control in Smart Power ICs

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Abstract

A new TCAD (Technology CAD) guided methodology developed for substrate current safe smart power IC design under both majority and minority carrier injection is introduced. Design recommendations derived from full-chip 3D device simulations are presented.

1. Introduction

Aim of the European ESPRIT project 29647 SUBSAFE was to develop a design methodology to control carriers, which are injected into the substrate by parasitic bipolar structures [1,2,3] created by power transistors, e.g. in H-bridge topologies (Fig. 1). Substrate effects due to carrier injection, which affect the controlling circuitry, are a major risk for smart power IC functionality [1,2,3] and may lead to costly redesigns or even loss of IC projects. Because of the distributed 3D behaviour and relevance of majority and in particular minority carriers [1,2,3] the goal was a 3D device simulation-guided methodology in contrast to the largely empirical approach commonly used.

2. Methodology

First, calibration [4], proof of feasibility and validation [5] of full-chip 3D device simulation by means of specially designed test structures on a test chip (Fig. 2) has been performed. Then, protective measures, namely substrate contact placements, have been investigated by means of full-chip 3D device simulation and recommendations for IC designers have been defined. The investigations have been compared on the basis of substrate current collected by a positively biased n-well and substrate potential shift.

The challenge of full-chip 3D device simulation lies in a strategy to simplify the complicated chip topology or to omit irrelevant structures (i.e. topology reduction). Without simplification, complexity of the device simulation structure goes far beyond today's computing power.

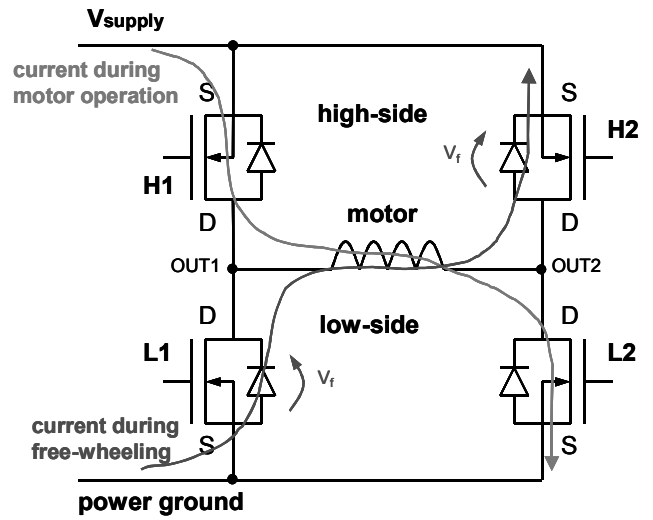


Figure 1. Motor control H-bridge with two high-side pLDMOS transistors (H1 and H2) and two low-side nLDMOS transistors (L1 and L2). During switching (all four power transistors are turned off to prevent short circuit between V_{supply} and ground) the inductive load drives the current through the free-wheel diodes which leads to below-ground voltage at OUT1 and above-supply voltage at OUT2 and turns on the parasitic bipolar transistors.

3. Calibration and validation

As important parameters, substrate doping N_A , minority carrier lifetime τ_n , and the Schottky-type characteristics of chip backside contact has been identified [3,4]. All these parameters have been calibrated by comparing measurements and simulation results as shown in Fig. 3 and 4.

The calibration procedure as well as application of transient full-chip 3D device simulation has been validated by good agreement of measurements and simulation results of minority carrier collection and substrate potential shift as shown in Fig. 5 and Fig. 6, respectively.

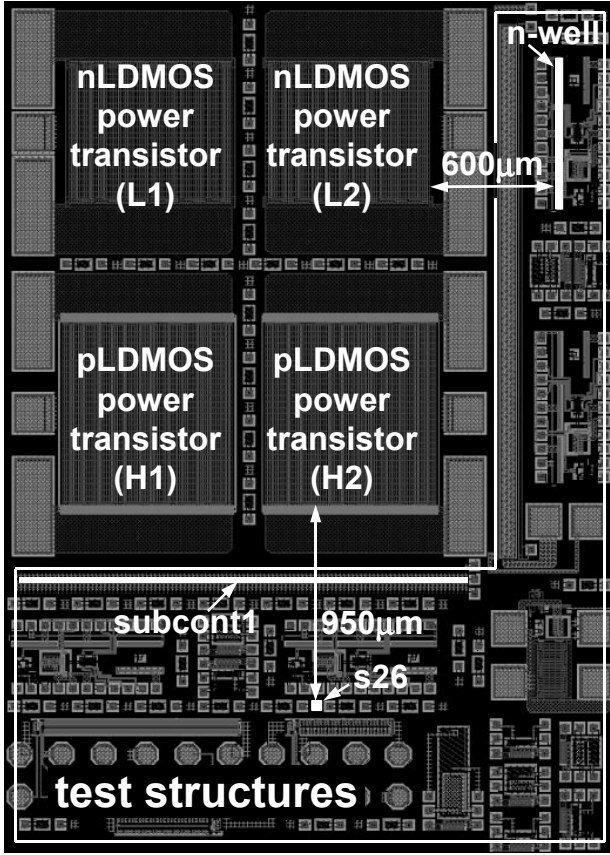


Figure 2. Test chip layout with four individually controllable LDMOS and a set of test structures, located where devices susceptible to substrate currents are implemented on product chips.

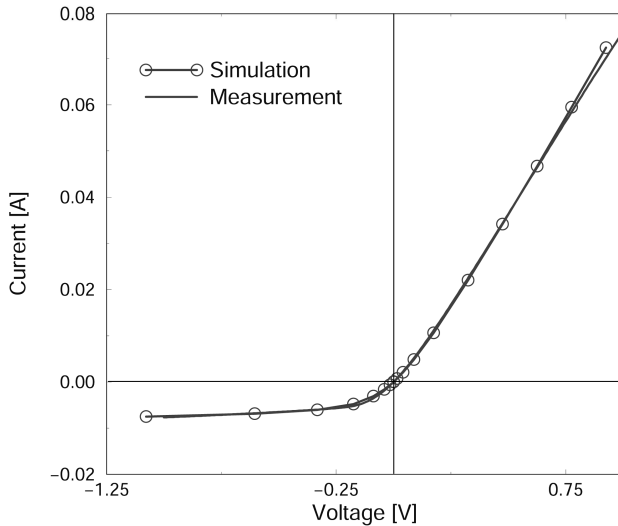


Figure 3. Calibration of Schottky-type characteristic of chip backside contact. Due to formation of an unknown alloy at the chip backside the Schottky barrier height Φ_{Bp} had to be calibrated whereas the recombination velocity at the interface had to be modified to account for higher leakage current.

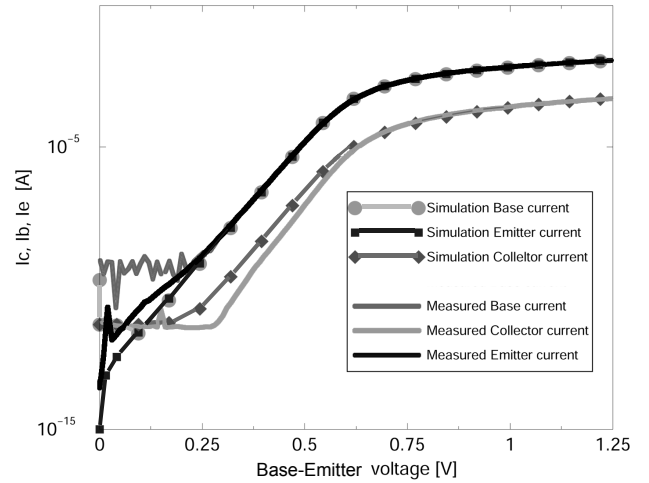


Figure 4. Minority carrier (electron) lifetime τ_n and substrate doping N_A calibration by comparing measurements and simulation results of a parasitic NPN transistor. The collector current strongly depends on the minority carrier lifetime, which allows calibration by fitting to measurements. In the high current regime the current is limited by the substrate doping which can be calibrated, therewith.

For minority carrier collection validation, minority carriers have been injected at the low-side transistor L2 and collected at the positively biased n-well located 600 μm away (Fig. 2). The substrate potential shift has been measured at the substrate contact s26 (Fig. 2) while injecting majority carriers at the 950 μm away high-side transistor H2, whereas the substrate has been grounded at the backside and the substrate contact subcont1.

The achieved agreement by a factor of about 2 is considered accurate enough to make important design decisions. The accuracy is limited by the amount of finite element mesh points in the simulations.

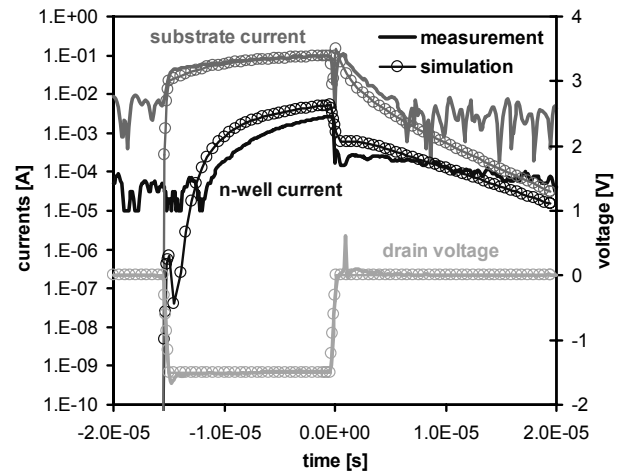


Figure 5. Validation of transient full-chip 3D device simulation by comparing measurement and simulation of transient injected minority carrier (electron) collection.

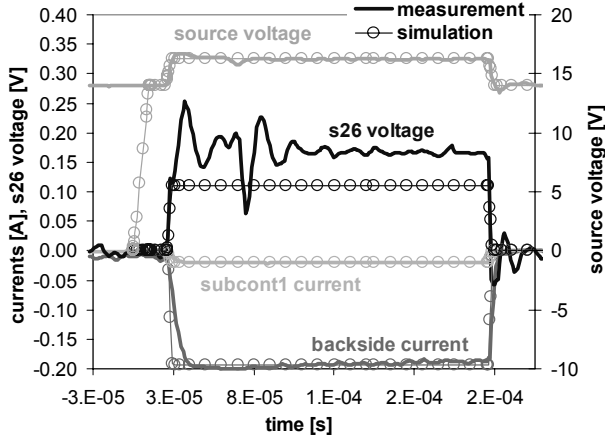


Figure 6. Validation of transient full-chip 3D device simulation by comparing measurement and simulation of transient positive potential shift due to majority carrier (hole) injection.

4. Substrate contact placement

4.1. Simulation structure

Figure 7 shows the application-near simulation structure used for substrate contact placement investigation. The two low-side transistors have been modelled by their minority carrier injecting buried layer to substrate junction. The majority carrier injecting parasitic PNP transistors of the high-side transistors have been replaced by p^+ -diffusions in the substrate. Through these p^+ -diffusions the substrate current determined by parasitic PNP transistor measurements has been injected. The substrate can be grounded at the Schottky-type backside contact and the substrate contacts on top. Substrate contact subcont1 is located directly in front of the high-side transistors, subcont2 behind the low-side transistors, and subcont3 adjacent to the minority carrier collecting n-well. In addition, a small, floating, substrate potential sensing substrate contact subcont4 has been placed beside the n-well.

4.2. Results

Influence of different substrate grounding configurations has been investigated by comparing the current collected by a $2.6 \cdot 10^4 \mu m^2$ n-well (Fig. 8) and the substrate potential at subcont4 (Fig. 9). Application-near below-ground and over-supply voltages and voltage slopes have been applied. Default configuration has been a grounded backside and a grounded subcont1 near the high-side power transistors. Figure 7 shows the hole quasi-fermi potential at the chip surface of the default configuration when electrons and holes are injected. The 3D nature of the problem becomes evident as the injection takes place crosswise, i.e. at L1 and H2 or at L2 and H1.

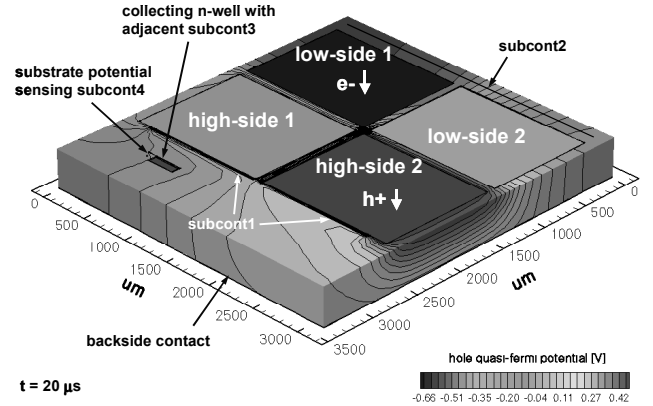


Figure 7. Simulation structure and hole quasi-fermi potential at chip surface calculated by means of full-chip 3D device simulation. The observed quasi-static potential shift at the n-well location is negative and does not lead to junction isolation failures in the controlling circuitry.

Current collection at different substrate grounding configurations in quasi-static conditions (at $20 \mu s$, Fig. 8) as well as at highly dynamic turn-off (displacement current) is listed in Table 1.

Table 1. Collected n-well currents

| grounded substrate contacts | quasi-static n-well current [A] at $20 \mu s$ | displacement n-well current [A] at turn-off |
|------------------------------|---|---|
| subcont1, backside (default) | $1.2 \cdot 10^{-7}$ | $5.0 \cdot 10^{-5}$ |
| subcont2, backside | $3.7 \cdot 10^{-8}$ | $6.1 \cdot 10^{-5}$ |
| subcont1, ohmic backside | $1.0 \cdot 10^{-8}$ | $7.8 \cdot 10^{-6}$ |
| subcont1, subcont3, backside | $2.9 \cdot 10^{-7}$ | $1.9 \cdot 10^{-5}$ |
| subcont1, without backside | $3.9 \cdot 10^{-7}$ | $5.8 \cdot 10^{-5}$ |

With a grounded subcont2 behind the low-side power transistors the quasi-static n-well current is almost one order of magnitude smaller than in the default configuration because of the build-up of a retarding field for electrons in the substrate, whereas the displacement current increases slightly. An ohmic backside contact leads to an even lower collected current in both cases. A grounded subcont3 near the collecting n-well results in a higher quasi-static current but in a lower displacement current because subcont3 ties the substrate to ground potential in the vicinity of the collecting n-well. Without grounded backside the quasi-static current is highest and the displacement current is also high.

Collected current during quasi-static substrate current injection does not exceed $1 \mu A$. However, capacitive displacement current during switching can reach $50 \mu A$.

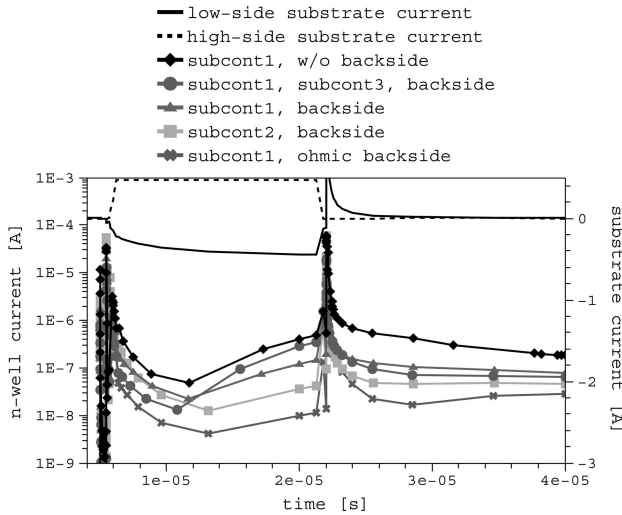


Figure 8. Comparison of collected n-well current for different substrate grounding configurations.

Substrate potential shift at quasi-static conditions is slightly negative and does not exceed -200 mV. During switching potential shifts can reach ± 0.5 V and can lead to junction isolation failure, therefore. If the backside is not connected, the substrate potential shift at substrate current turn-off can even reach several volts due to the high reverse recovery current peak of the low-side buried layer to substrate junction (Fig. 9).

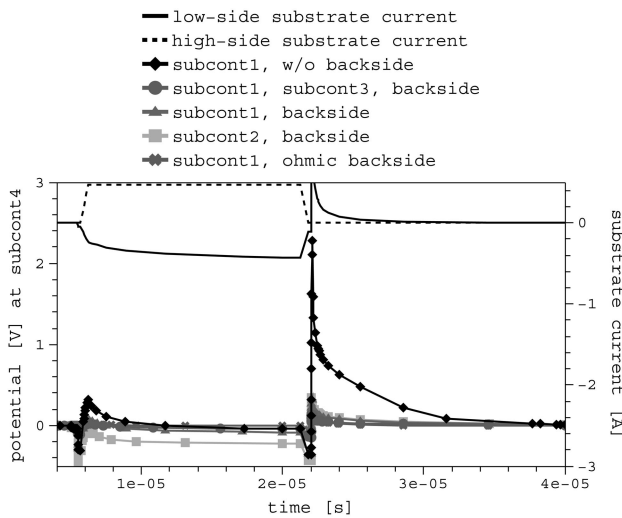


Figure 9. Comparison of substrate potential shift for different substrate grounding configurations.

Lowest collected current and substrate potential shift can be reached by an ohmic backside contact. A not connected backside leads to the highest n-well current and the highest substrate potential shift and should therefore be avoided whenever possible. Substrate contact grounding on top of the chip shows counteracting effects, e.g. a substrate contact near an n-well reduces displacement current and substrate potential shift but increases the quasi-static current. The magnitude of these

effects highly depends on the specific configuration and conditions (e.g. below-ground and above-supply voltages and voltage slopes).

5. Conclusions

A new methodology for substrate current safe smart power IC design has been developed, including calibration procedure with appertaining test structures, topology reduction methodology and transient full-chip 3D mixed-mode simulations. For the first time full-chip 3D device simulations of substrate current effects have been successfully validated and applied to a state-of-the-art smart power technology. Design recommendations for substrate contact placement have been presented.

6. Acknowledgement

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7. References

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