High-performance Silicon-On-Glass VDMOS transistor for RF-power applications

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Abstract

A complete analysis of DC and RF performance of a novel SOI vertical DMOS transistor on glass and a conventional LDMOS transistor for RF power applications is presented. The analysis is based on MEDICI device simulations and the "Smoothie" database model for FET devices. An SOI VDMOST on glass with a breakdown of 115V, a specific on-resistance R_{ONSP} of 3mΩcm^2, an f_{Tmax} of 7.4 GHz at V_{DS}=26V and a saturation current of 1.25·10^{-4} A/μm at V_{DS}=10V is demonstrated. A device with 1mm long gate has PAE of 43% and power gain of 18.5 dB with 1dB compression point at P_{OUT}=26dBm. Since this SOI VDMOS device shows better linearity and higher power gain compared to conventional LDMOST, it would be the device of choice for RF power applications. Moreover, silicon-on-glass technology offers integration with high quality passives and the possibility to electroplate copper heat sinks only a few microns away from the active device area. Both features are very important for development of integrated power amplifiers.

1. Introduction

Highly linear and highly efficient power amplifiers are needed in all kinds of personal communication systems. Until recently, bipolar power transistors were the main products on the market that target RF power applications since conventional VDMOS transistors could not operate at frequencies high enough for such applications.

LDMOS transistors for RF power applications [1],[2] have been designed driven by the advantages of VDMOS transistors over bipolar transistors mainly with respect to linearity. Although, these devices show very good RF performance, reliability issues have to be addressed as, for instance gate oxide degradation due to hot carrier generation and self-heating effects. Moreover, integration with high quality passive components is hampered by silicon substrate losses.

Another important technology made its breakthrough during the last decade. Substrate transfer technology called Silicon-on-Anything (SOA) [3] offers an integration of high quality active devices with high quality passive components. It has become possible to produce back-wafer contacted devices [4] in which substrate capacitance and common lead inductance are completely eliminated. Besides, an efficient heat sinking can be realized by means of copper electroplated on the back-wafer only a few microns away from the active device area. Therefore, silicon-on-anything technology has become very attractive for development of integrated power amplifiers.

We propose and analyse a new device that combines advantages of LDMOS transistors with those of Silicon-on-Anything technology. An SOI vertical DMOS transistor on glass for RF power applications is demonstrated in this paper using device MEDICI simulations and the "Smoothie" database model for FET devices (see [9] and Section 3.2). Device RF performance is simulated in details under realistic circuit conditions since it is of a crucial importance for RF power applications. Moreover, a systematic comparison to a conventional LDMOS transistor is also performed.

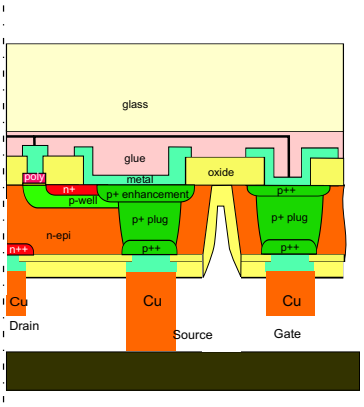


Figure 1. Schematic cross-section of SOI VDMOST on glass - basic layout.

2. Device structure

A schematic cross-section of an SOI VDMOS transistor on glass is presented in Fig. 1. The drain is contacted via the back-wafer, while the source contact on the front-wafer is fed through to the back-wafer via highly doped plugs and contacted to the back-wafer as well. The two gates share a common drain. All the gate fingers on the front-wafer are first connected and then fed through to the back-wafer. The gate, drain and source contacts are contacted using the low-temperature, low-ohmic back-wafer contacting [4]. A two level, few microns thick copper, electroplated on the back-wafer, assures good thermal management and minimizes debiasing due to voltage drops over the metalization lines [5]. The source is thus bonded to the thermal and RF ground which maximizes heat sinking and minimizes common lead inductance.

The channel underneath the gate is formed by the lateral diffusion of the p-well implantation. Both the thickness and doping of the epi-layer can be chosen to control the breakdown voltage. Moreover, these two parameters together with the gate configuration, layout topology and gate to drain distance can be used to control the electric field distribution, saturation current, device capacitances and specific on-resistance. The parameters can be optimized to make SOI VDMOST on glass suitable for RF-power application in cellular base stations.

2.1. Layout topology

A single front-wafer metal stripe-gate topology similar to LDMOS stripe-gate topology is used rather than cellular approach since the latter requires multi-level interconnection layers to integrate the unit cell. Moreover, in cellular approach, thick interlevel dielectric films and metal interconnection films are required to sustain high voltage and high current density [6]. The proposed stripe-gate topology is shown in Fig. 2. This configuration provides maximum decoupling and prevents cross-talk since the signal lines are shielded from the outside world by grounded source lines similar to ground-signal-ground configuration. An arbitrary long device can be formed using an array of stripe-gate devices.

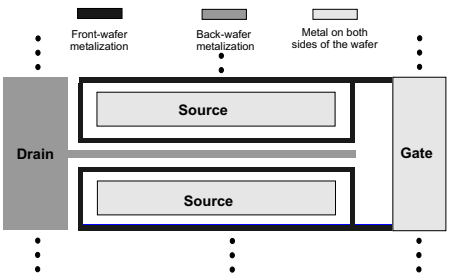


Figure 2. Schematic of proposed stripe-gate topology.

2.2. Field-plating electrode

Four gate configurations of choice have been investigated in details in [7]. The best flexibility with respect to different demands of RF-power applications is achieved using the device with two short gates separated by a field-plating electrode that is shortened to the source [8]. The device schematic cross-section is given in Fig. 3. The field-plating electrode minimizes the gate-drain capacitance and short channel effects by redistributing potential lines in gate and drain regions. The position and height of the field-plating electrode can be adjusted to find the optimal compromise between linearity, wide-band operation and hot carrier effects.

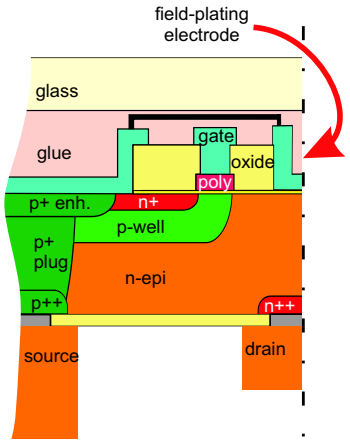


Figure 3. Schematic cross-section of SOI VDMOST on glass with field-plating electrode that is shortened to source.

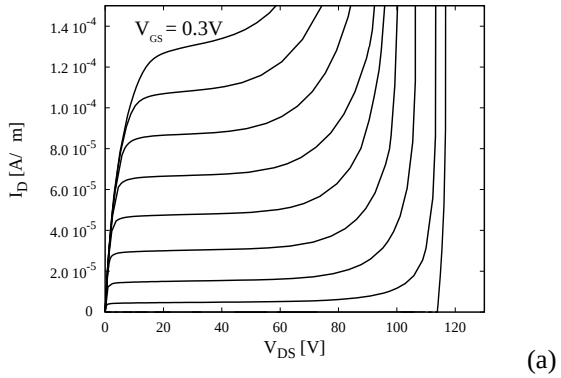
3. Device simulations

In all the simulations presented in this paper, lattice heating effects have been neglected. This is reasonable since in the devices presented, thick copper on the back-wafer is electroplated only few microns away from the area where the heat is generated and therefore it serves as an excellent heat sink. In power devices such waferscale solutions are usually necessary for relieving self-heating and thermal runaway problems. Replacing silicon by copper as is done here in the Silicon-On-Anything approach is an excellent solution due to superior thermal conductivity and high specific heat of copper.

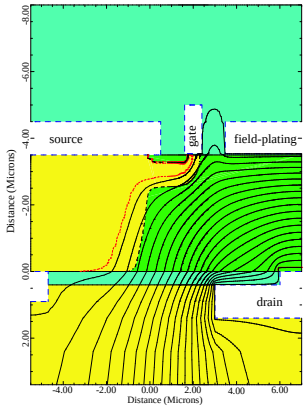
TSUPREM-4 process simulations were used to simulate and optimize device doping profiles. The data from TSUPREM-4 were imported into MEDICI where device DC and AC simulations were performed. Since RF characteristics such as power added efficiency, gain and intermodulation distorsion are the parameters of the most concern for analysed devices, the simulations were completed using the ”Smoothie” database model for FET devices [9].

3.1. DC and AC MEDICI simulations

Two examples of SOI VDMOS transistors on glass are analysed here along with a conventional LDMOS transistor for base station applications. A comparative study of the three devices has been conducted. An LDMOST with a gate length of 0.8μm, a gate oxide thickness of 60nm and a drain extension of 3.75μm has been simulated. An epi thickness of 4μm, gate oxide thickness of 60nm and gate length of 0.8μm have been chosen for the first SOI VDMOST on glass (called here VDMOST 4μm). The second analysed SOI VDMOST on glass (called here VDMOST 3.5μm) has epi thickness of 3.5μm, gate oxide thickness of 40nm and gate length of 0.8μm. These VDMOS devices have different doping profiles, so the oxide thickness is adjusted to compensate for the different doping profile and assure that both devices have same threshold voltage.



(a)



(b)

Figure 4. MEDICI simulated (a) output characteristics for VDMOST 3.5μm and (b) potential contours at breakdown voltage for Poisson-only simulation. Threshold voltage is V_{TH}=3.5V.

In order to support variations in RF voltage the device breakdown should be at least 3 times the operating voltage which is 26V for the base station applications. MEDICI simulated output characteristics for VDMOST 3.5μm are shown in Fig. 4a. It can be noted that the breakdown voltage is sufficient to meet the requirements. The distribution of potential contours at the breakdown shown in Fig. 4b is simulated using a Poisson-only calculation with impact ionization included. The ionization path is far from the surface and near the drain edge. Therefore, degradation of gate oxide due to hot carrier generation is not of a concern. The most important DC characteristics along with f_{Tmax} at V_{DS}=26V for the three devices are shown in Table 1.

Table 1. Simulated DC characteristics and f_{Tmax} at V_{DS}=26V. I_{DSAT} is extracted for V_{DS}=10V.

Device type	LDM	VDM 3.5μm	VDM 4μm
BV_{DS} [V]	100	115	120
R_{ONSP} [mΩcm^2]	1.5	3	4
I_{DSAT} [A/μm]	$2{\cdot}10^{-4}$	$1.25{\cdot}10^{-4}$	$1{\cdot}10^{-4}$
f_{Tmax} [GHz]	7.4	7.4	7.1

Simulated off-state capacitances are shown in Fig. 5. A significant reduction of gate-drain capacitances of VDMOS transistors with respect to LDMOS transistor is observed due to presence of a field-plating electrode. This suggests that linearity of VDMOS transistors on glass is improved compared to conventional LDMOST. An increase of capacitances with decreasing gate oxide thickness is noticeable as well.

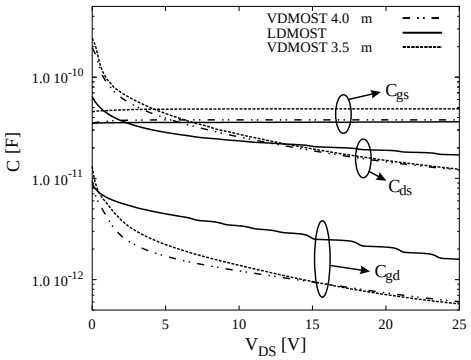


Figure 5. MEDICI simulated off-state capacitances of device with W_g=70mm (30W device).

3.2. RF performance

There is no possibility of performing harmonic balance analysis in MEDICI that therefore is not able to handle RF performance of devices. RF performance was studied using the "Smoothie" database model based on the approximation of simulated or measured device Y-parameters. The model is implemented in Agilent Advances Design System program [10] and is used to evaluate the device performance in realistic circuit conditions. The model was fed with MEDICI simulated Y-parameters. The simulations did not include any package parasitics, so only Y-parameters from MEDICI were used as starting data around which an impedance matching network was built. Fig. 6 shows the circuit schematic, in which ideal λ/4 power supply lines have been used to facilitate short and

open conditions for the even and odd-order harmonics, respectively. Load and source impedance for the fundamental frequency have been optimized for maximum output power and best linearity. Large signal AC analyses of both SOI VDMOST on glass and conventional LDMOST have been performed to determine the P_{IN}-P_{OUT}, gain characteristics, PAE and two-tone inter-modulation distorsion for a 1mm gate width device when matched for best linearity in class AB. Power gain versus output power is presented in Fig. 7, while PAE versus input power is given in Fig.8. Third-order intermodulation distorsion versus output power is shown in Fig. 9.

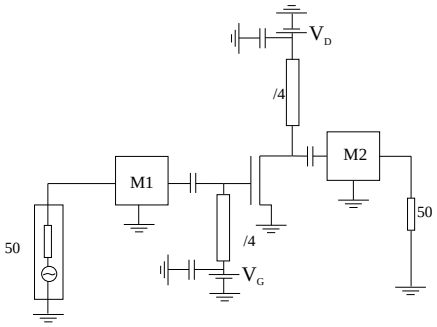


Figure 6. Schematic of the circuit with matching networks, used in ADS for the RF performance simulation.

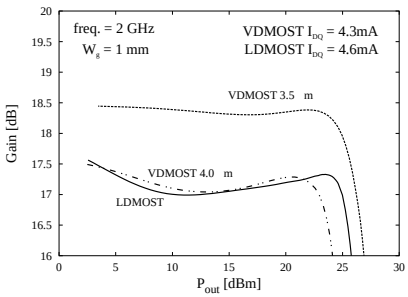


Figure 7. "Smoothie" simulated power gain versus output power.

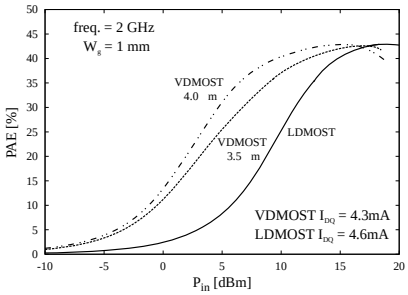


Figure 8. "Smoothie" simulated PAE versus input power.

These results suggest that the technological parameters of SOI VDMOST on glass can be adjusted to achieve a

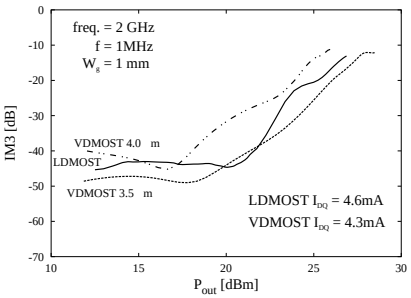


Figure 9. "Smoothie" simulated IM3 versus output power.

noticeable improvement of device power gain, 1dB compression point and intermodulation distortion as compared to respect to LDMOS counterpart.

4. Conclusions

A novel high-performance vertical DMOS transistor on glass for RF power applications is presented and studied using AC and DC MEDICI simulations and the "Smoothie" database model for FET devices. In the device configuration chosen, the Silicon-on-Glass technology is used to achieve several improvements over the comparable LDMOS devices: degradation due to generation of hot carriers is eliminated, heat sinking is improved and debiasing in metalization lines is eliminated by copper electroplated on the back-wafer. Moreover, this device is suitable for integration with high quality passives and therefore it is very promising for integrated power amplifiers. A device is demonstrated with a breakdown of 115V, specific on-resistance R_{ONSP} of 3mΩcm^2, an f_{Tmax} of 7 GHz at V_{DS}=26V and a saturation current of $1.25{\cdot}10^{-4}$ A/μm at V_{DS}=10V is demonstrated. A device with the gate width (W_g) of 1mm shows maximum PAE of 43% and power gain of 18dB when matched for best linearity. Compared with conventional LDMOST, a novel VDMOST on glass shows better linearity and higher power gain while providing high PAE. Such devices are now being processed in a collaboration between the Nijmegen and DIMES cleanroom facilities.

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