Realization of a SCR on an Epitaxial Substrate Using Al Thermomigration

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Abstract

The thermomigration of Al/Si liquid droplets in silicon by means of a vertical temperature gradient has been studied as an alternative to boron diffusion for the realization of deep p^+ peripheral zones enabling reverse voltage-blocking capability of a power SCR. The process involves liquid state diffusion phenomena so that realization of those p^+ zones takes a few minutes only compared to hundred hours with boron solid state diffusion. The thermal budget is therefore compatible with an epitaxial substrate giving an innovative structure for power thyristors. This paper includes a presentation of the thermomigration process together with the results obtained so far.

1. Introduction

The manufacturing of power devices involves processes that do not belong to mainstream silicon ICs roadmap. SCRs, Triacs, and power ICs such as ASD™ are vertical devices where current flows through the whole thickness of the die and they often require both direct and reverse voltage-blocking capability. While forward blocking capability is ensured by the p zone in the active region (see figure 1), the reverse blocking capability requirement leads to the necessity of total vertical insulation of the device by the extension of the p-n backside junction to the device surface. This peripheral junction termination consists of p-doped vertical walls. The technique mostly employed to realize those walls is double-side boron implantation followed by a diffusion annealing at temperatures superior to 1250 °C during a few hundred hours. This enormous thermal budget has many severe drawbacks: deformation of silicon wafers, creation of microscopic defects, heavy metal contamination, surface consumption and concentration gradient due to isotropic diffusion, impact on cycle time. Moreover, it is not compatible with the use of epitaxial substrates which purpose is to reduce the low doped n layer thickness in order to minimize the serial resistance. Indeed, the p-substrate would diffuse in the n-epitaxial layer, and then this n-layer would be too thin to handle high voltages. Therefore, a low thermal budget alternative to boron diffusion for p-wells has to be found to allow SCR realization on epitaxial wafers.

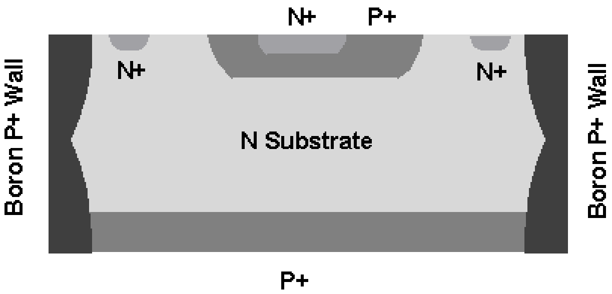

Figure 1. Silicon structure of a boron p^+ wall SCR

One of these alternatives is the thermomigration of aluminum/silicon droplets in silicon by means of a vertical temperature gradient [1]. The aim of this paper is to present the application of thermomigration to the realisation of SCRs on epitaxial substrates.

2. Thermal gradient setup and apparatus

The thermomigration process is based upon the setting of a vertical thermal gradient within the thickness of a silicon wafer. The annealing furnace that was used for this study is a Rapid Thermal Processor (RTP) specially designed to fulfill this requirement. The upper part of the furnace consists of a row of halogen lamps, while the lower part is an absorbing body instead of the second series of lamps or reflective wall found in a conventional RTP. The lamps provide infrared energy to the front side of the silicon wafer; this energy is transmitted through the wafer by thermal conduction and then the backside of the wafer freely radiates towards the absorbing body. This body is specially designed to have its emissivity close to one so that absorption is optimal and is maintained at a low temperature so as to avoid radiative reemission to the wafer. Under the assumptions that (i) there is no reemission to the wafer and (ii) silicon is opaque to infrared radiation, the thermal gradient G_{theo} is given by the following expression:

$$G_{theo} = \frac{\Delta T}{t} = \frac{\varepsilon\sigma T^4}{K_{Si}} \quad (1)$$

where σ is the Stefan-Boltzmann constant (σ = 5.62 10^{-12} $Wcm^{-2}K^{-4}$), ε the emissivity of silicon wafer backside surface (dimensionless), T the absolute temperature of the wafer backside surface (K), K_{Si} the thermal conductivity of silicon ($Wcm^{-1}K^{-1}$), ΔT the temperature difference between both sides of the wafer and t the wafer thickness (cm). This theoretical gradient is temperature dependent through T^4, K_{Si} and to a less extent . Its value ranges from 50 °C/cm at 1150 °C to 140 °C/cm at 1412 °C.

Details, layout and main issues of this RTP processor can be found in previous papers [2, 3]. One of the specificity of this apparatus is the presence of viewports allowing the observation of wafer illuminated surface. A video camera and a recorder are available together with a laser reflectometry system, allowing the endpoint detection of the process.

3. Thermomigration process

The thermomigration process is based on the migration of an Al/Si liquid alloy through a silicon wafer under the influence of a vertical temperature. The result is the formation of a p^+-Al-doped trail extending from back to front side of the wafer.

Before thermomigration, an aluminum layer is evaporated on the silicon wafer. This layer is submitted to proximity photolithography and etching so as to delineate Al patterns, i.e. doping zones. The wafer is then heated up in the RTP apparatus with the Al-patterned side facing the absorbing body. The thermal cycle is composed of a ramp-up segment where power is linearly increased followed by a power plateau and then a ramp-down part which onset is controlled by emergence observation (camera and/or reflectometry system).

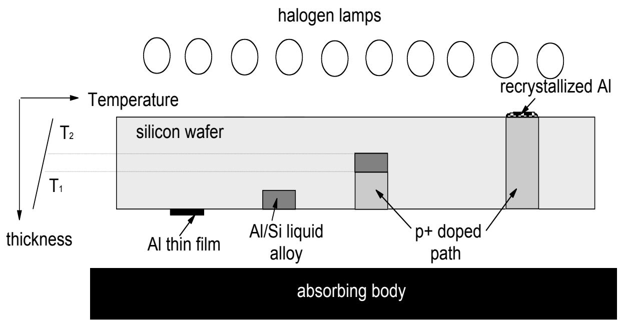

Figure 2. Simplified mechanism of thermomigration process. Typical steps are chronologically shown from left to right

The process temperature is well above Al/Si eutectic temperature (577 °C) so that a liquid Al/Si alloy forms on the back surface of the wafer (see figure 2). The vertical temperature gradient imposed within the wafer thickness is reflected in the liquid alloy. Therefore, as silicon solubility increases with temperature, silicon concentration is higher at the hot side of the alloy (temperature T_2 - front end) than at the cold side (temperature T_1 - rear end). This slight concentration gradient thus induces silicon diffusion from rear to front side of the liquid droplet, leading to undersaturation at the front side and supersaturation at the rear side, as regards equilibrium values. As a consequence, the front side continuously dissolves silicon atoms while the rear side rejects silicon that recrystallize within the silicon host matrix. These two phenomena leads to global migration of the droplet as a vain attempt to reach silicon concentration equilibrium values. The solid rejected at the cold side of the droplet is a solid solution of monocrystalline silicon doped with aluminum to the solubility limit (approximately 10^{19} atoms/cm^3). Therefore, the droplet migration along the vertical thermal gradient leads to the formation of a uniform, Al-p^+-doped path.

The velocity V of liquid droplets and thus the speed of doping can be expressed under the simplified form below [4]:

$$V = \frac{D_0 e^{-\frac{Q}{RT}}}{1 - X} \frac{\partial X}{\partial T} G_l \quad (2)$$

where $D_0 e^{-Q/RT}$ is the interdiffusion coefficient in the liquid alloy, X the mean silicon atomic fraction in the droplet, $\partial X/\partial T$ the liquidus slope and G_l the value of the vertical gradient in the liquid alloy. The interdiffusion coefficient is about $2\ 10^{-4}$ cm^2/s at 1300 °C, which is seven orders of magnitude greater than the boron solid-state coefficient diffusion at the same temperature. This is the main reason why droplet migration is very fast even though temperature differences between the two sides of the wafer (2 °C at 1300 °C) or of the liquid droplet (0.1 °C at 1300 °C) are very small. The curve displayed in figure 3 shows a theoretical assessment of the migration velocity as a function of temperature, with = 0.6, G = G_{theo}, K_{Si} as a function of temperature [3], X and $\partial X/\partial T$ from Al/Si phase diagram assessment, D_0 = $5\ 10^{-4}$ cm^2/s and Q = 12.54 kJ/mol [4].

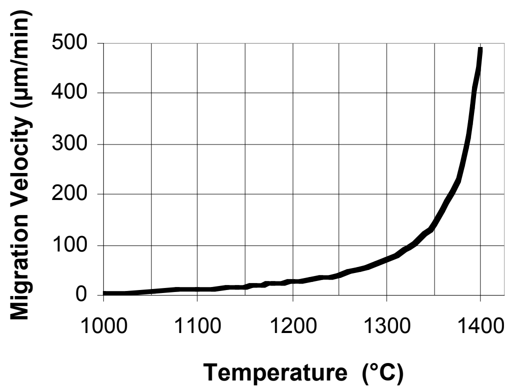

Figure 3. Migration velocity as a function of annealing temperature

From this curve it can be seen that velocity is about 100 µm/min between 1300 and 1350 °C. Realization of deep p^+ zones extending from side to side of a 200 µm thick wafer thus takes about two minutes only, compared to a few hundred hours with boron solid-state diffusion. One can immediately see the benefit of thermomigration in terms of thermal budget. As the temperature difference between both sides is very small, the solubility limit and thus the path doping level remain constant through the whole thickness. Finally, if the migration is only gradient-driven, there is theoretically no lateral silicon dissolution and therefore no lateral doping.

The thermomigration process involves the formation of an Al/Si liquid alloy at the onset of the migration on the back surface of the wafer. This alloy can be affected by a few instabilities that are described in paper [3]

4. Experimental results

4.1. Deep doping by thermomigration

Figures 4 and 5 show one of the typical experimental results obtained on a FZ-grown, 30 Ωcm, 250 µm thick, (111) wafer with a 6-µm thick, 190 µm wide, grid-like Al pattern. The plateau temperature was about 1250 °C during 9 minutes with N_2 processing gas. The first photograph (figure 4) is a cross-section of the wafer where the deep p^+ zone was chemically revealed. This observation gives the evolution of the path width in the wafer thickness but tells nothing about lines morphology in the two other dimensions. The second view (figure 5) corresponds to a piece of wafer that has been polished and revealed. It gives the information of continuity and morphology of doped zones in the wafer plane.

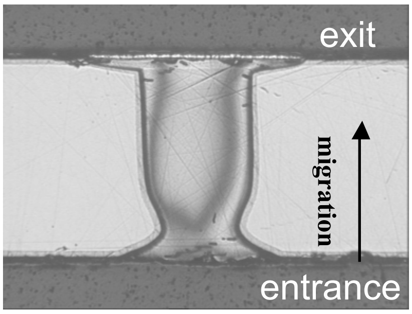

Figure 4. Cross section of an Al doped wall after chemical etching. Wafer thickness is 240 μm

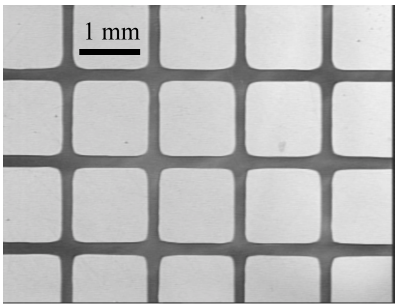

Figure 5. Front (top) view of Al doped walls after chemical etching

As can be seen, the cross-section exhibits a narrowing of the doped path at the onset of the migration. The penetration angle increases with the temperature and the Al layer thickness and is not orientation-dependent. For the (111) cross-section shown, we observe that, after initial narrowing, the droplet shape flattens in a plane parallel to the wafer surface and gradually reaches a constant steady-state width. For (100) wafers, the initial narrowing is immediately followed by steady-state migration without droplet flattening.

SIMS analyses were performed so as to evaluate the chemical profile of aluminum in TGZM p^+-doped zones. The result is that the Al level is constant in the bulk at about 10^{19} at/cm^3, as theoretically predicted.

Spreading Resistance Profile (figure 6) across a TGZM line confirms that the doping level corresponds to the aluminum concentration. This means that a major part of aluminum atoms are electrically active, i.e they are in a substitutional position. This is not surprising because Al-doped silicon recrystallization during TGZM is similar to a liquid phase epitaxy process leading to the formation of a substitution solid solution of aluminum in silicon.

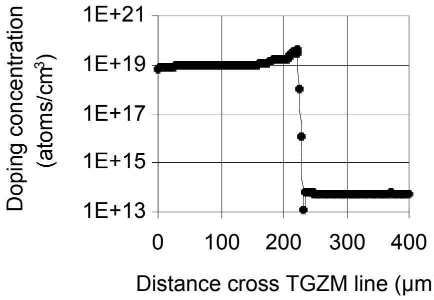

Figure 6. spreading resistance profile of an aluminum doped wall

4.2. Epitaxial thyristor

The low thermal budget associated with thermomigration is compatible with the use of epitaxial substrates: a minimum solid state diffusion of the doping species of the substrate rear p^+ layer will take place, and the thin n layer, which purpose is to minimise the serial resistance of the thyristor will be preserved. On the contrary, the classical process detailed in section 1 would drastically reduce the n layer thickness, which then would not be enough to handle high voltages (superior to 400 V typically).

So generally, bulky n-wafers are used to manufacture high voltages SCRs. The residual n layer thickness enabling voltage handling (usually too large) is a function of both the diffusion depth of the various p^+ zones and the wafer thickness. It has to be minimized so as to reduce the on-state serial resistance of the SCR and therefore power consumption. To avoid a thick n layer, the wafer thickness is usually minimized with the risk of increasing wafer deformation and breakage. In other words, when thermomigration together with an epitaxial substrate are used, the n layer and wafer thicknesses can be adjusted independently.

In order to check the compatibility of thermomigration with an industrial thyristor process, we have manufactured the structure depicted in figure 7 on (111)-orientated wafers.

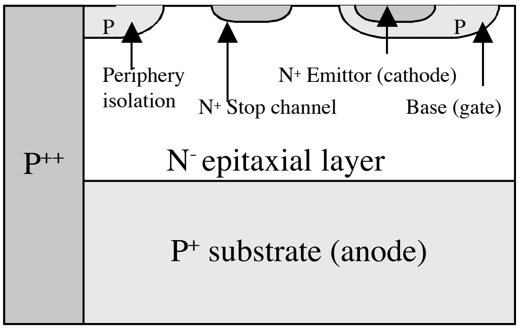

Figure 7. Structure of thyristor on epitaxial substrate – only one Al wall and stop channel are depicted

A cross section of the manufactured structure is shown in figure 8. It can be seen that the droplet migration was not affected by the P^+ substrate / N epitaxy interface. Moreover the small growth of the P^+ layer due to the thermal budget associated to the manufacturing process, including thermomigration, is visible (horizontal grey strip). We may observe that thermo-migrated trails are uneven (hole on the left path and sudden enlargement on the right one). These irregularities are due to the 4° off-axis wafer cut necessary for good epitaxial growth on (111) substrates.

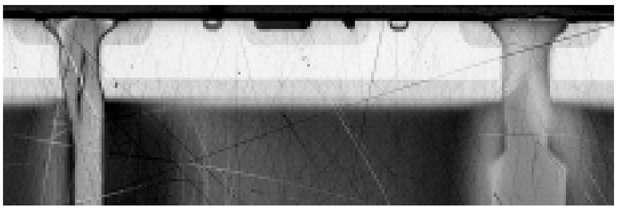

Figure 8. Cross section of thyristor and insulating walls after chemical etching. Wafer thickness is 260 μm – Initial epitaxial layer thickness is 120 μm. For clarity vertical and horizontal scales are different.

The theoretical voltage handling capability obtained by DESSIS-ISE simulator is 475 and 465 V for direct and reverse bias respectively. Experimental results are shown in figure 9. It can be seen that they are very close to theory, that is 450 and 480 V respectively. Furthermore, avalanche breakdowns are very abrupt and leakage currents are under 10 nA (direct bias) and 100 nA (reverse bias). The gate triggering current could not be measured (less than 50 nA) because of the extreme sensibility of the SCR. Gold doping or electron irradiation could be used to lower the transistor gains in the structure, in order to increase gate current for off/on state switching.

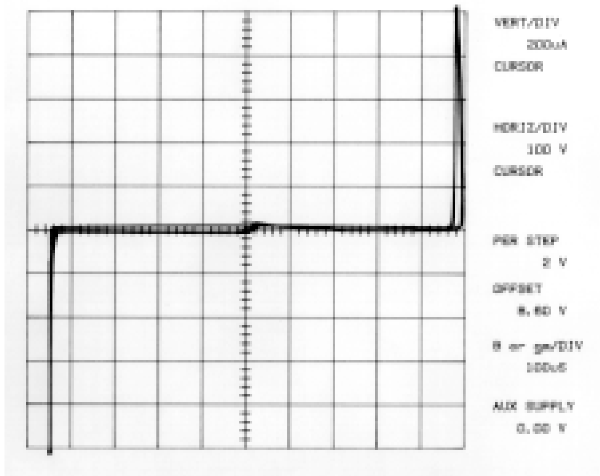

Figure 9. Voltage handling capability of epitaxial thyristor. Hor/div = 100V – Vert/div = 200 μA. Direct bias is on the left.

5. Conclusion

The study of thermomigration allowed us to determine the main issues and vulnerabilities as regards process industrialization [3]. Furthermore, the electrical characterization of the "epitaxial SCR" has shown promising results. The answers given to those two main issues (process and functionality) demonstrate the great potential of the thermomigration as an alternative technique to boron solid-state diffusion for bidirectional power devices. Yet, further investigations are still necessary in order to reach a thorough knowledge of the process. In the same manner, global process uniformity must be improved so as to reach yield objectives.

6. References

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