Design Guidelines for Linear Amplification and Low-insertion loss in 5-GHz-band SOI Power MOSFETs

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Abstract

This paper describes guidelines for designing thin-film SOI power MOSFETs for linear-amplification and SPDT-switch applications. A fabricated device shows power-added efficiency of 61% at 5.25 GHz (Vdd @ 3.0 V). For linear-amplification, it is important to suppress the parasitic bipolar effect and reduce the on-resistance. For a SPDT-switch, it is important to reduce Ron and use high-resistivity Si substrate.

1. Introduction

Si LSI technology is attractive for the fabrication of RF front-end circuits because it enables the development of all-Si MMICs [1]. In addition, it provides a high level of integration. MMICs contain both active and passive devices integrated on the same chip. For this reason, the high-frequency performances of both the active and passive devices are quite important. When the active devices are fabricated by using bulk-Si process, their performance is suitable for the 2-GHz band [2]. However, with the bulk-Si process, it is difficult to make high-performance passive devices, such as inductors, because it is hard to use a high-resistivity Si substrate [2], which will reduce the loss due to substrate conductivity.

In such a scheme, RF devices fabricated on a thin-film SOI substrate are promising candidates for high-performance MMICs [3][4]. RF-CMOS devices and on-chip inductors made in this way exhibit acceptable performance at 2 GHz [3]. In addition, highly efficient RF power MOSFETs have been fabricated on SOI substrate for power amplifiers for multi-gigahertz applications, and their performance was suitable for both 2 GHz-band [5][6] and 5 GHz-band [6]. A power amplifier is quite important, for example, in cellular phone applications, because it accounts for approximately half the power consumed. In recent wireless access systems using digital modulation, for the power amplifier, linear amplification is required under lower power consumption. RF power MOSFETs must therefore operate effectively with good linearity. However, a device structure suitable for linear-amplification characteristics in thin-film SOI power MOSFETs has not been studied yet. Another attractive application of RF power MOSFETs is an SPDT-switch, which is a key component of the RF front-end circuits; however, it also has not been studied yet. This paper describes guidelines for designing SOI power MOSFETs for linear-amplification and SPDT-switch applications.

2. Device structure and fabrication process

A schematic cross section and top view of the SOI RF power MOSFET are shown in Figs. 1 (a) and (b). The self-aligned drain offset structure and titanium salicide process were employed to increase the power-added efficiency [6]. The body contacts were formed to suppress the parasitic bipolar effect [6]. The poly-Si gate electrode was doped by ion implantation to match the salicide process. The main structural parameters are listed in Table 1. The target breakdown voltage was 10 V, which is sufficient for power supply voltage of 3.3 V and the use of a lithium ion battery as a power source.

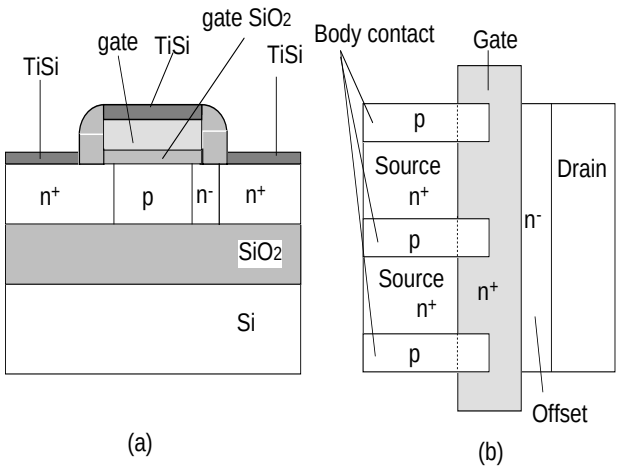

Fig. 1 (a) Schematic cross section and (b) top view of an SOI RF power MOSFET having the self-aligned drain offset structure.[3]

Table 1 Main structural parameters.

Top silicon layer thickness (μm)	0.16
Buried oxide layer thickness (μm)	0.40
Channel length (μm)	0.4 ~ 0.8
Gate oxide (nm)	13
Finger length (μm)	20

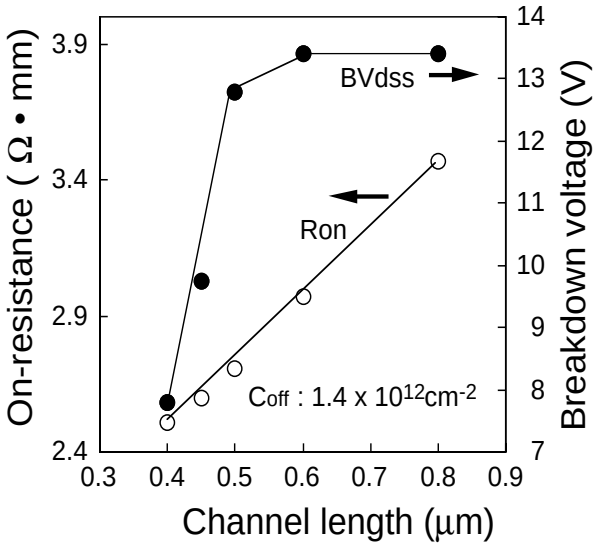

Fig. 2 Dependence of the on-resistance and breakdown voltage on the channel length.

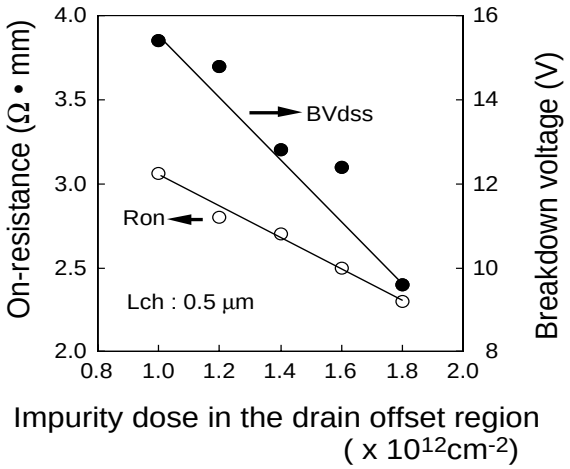

Fig. 3 Dependence of the on-resistance and breakdown voltage on the impurity dose in the drain offset region.

3. Results and discussions

The dependence of on-resistance and breakdown voltage on channel length is shown in Fig. 2. The on-resistance and breakdown voltage increase with channel length. The target breakdown voltage of 10 V is exceeded when the channel length is 0.5 μm. The channel length of 0.5 μm is the best taking into consideration the breakdown voltage.

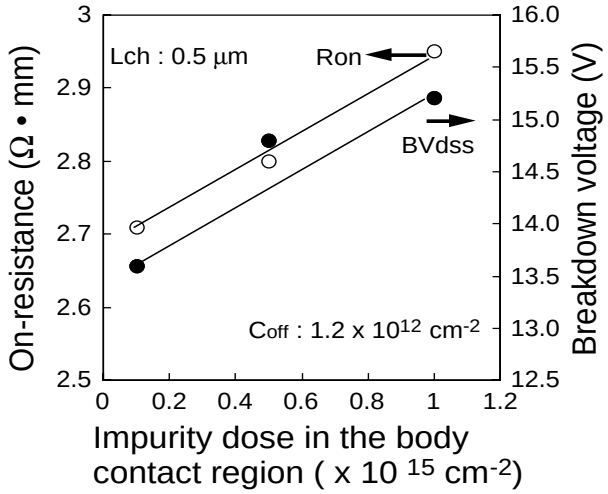

Fig. 4 Dependence of the on-resistance and breakdown voltage on the impurity dose in the body contact region.

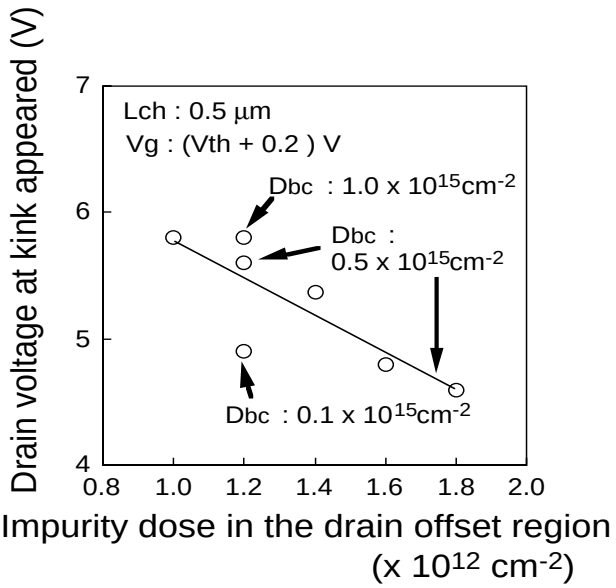

Fig. 5 Dependence of the drain voltage at kink appeared on the impurity dose in the drain offset region.

The dependence of on-resistance and breakdown voltage on impurity dose in the drain offset region is shown in Fig. 3. The channel length is 0.5 μm. On-resistance and breakdown voltage decrease with increasing impurity dose in the drain offset region.

The dependence of on-resistance and breakdown voltage on impurity dose in the body contact region is shown in Fig. 4. The channel length is 0.5 μm. On-resistance increases with increasing impurity dose in the body contact region because the depletion of the poly-Si gate electrode caused by inter-diffusion of the Born and As ions in the poly-Si gate electrode (Fig. 1(b)) was promoted by

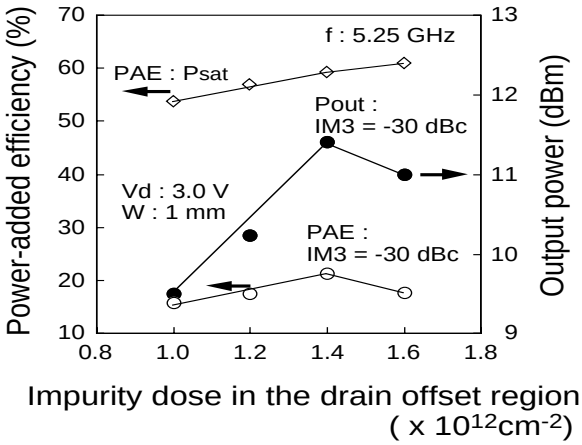

Fig. 6 Dependence of the power-added efficiency and output power on the impurity dose in the drain offset region.

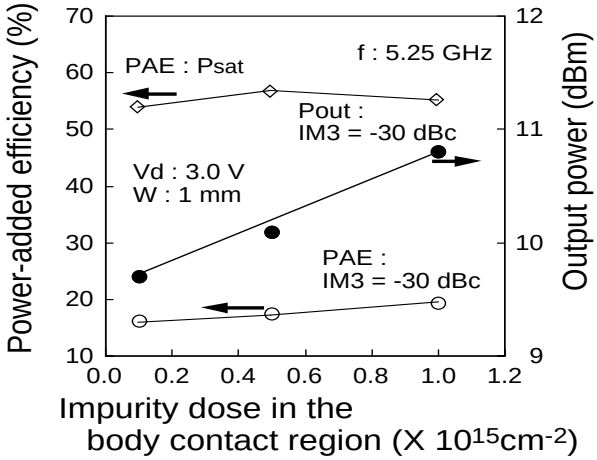

Fig. 7 Dependence of the power-added efficiency and output power on the impurity dose in the body contact region.

increasing the impurity dose in the body contact region. Breakdown voltage also increases with increasing impurity dose in the body contact region.

The drain voltage at which kink appeared (Vk) was measured to evaluate the parasitic bipolar effect. Dependence of the Vk on the impurity dose in the drain offset region is shown in Fig. 5. The impurity dose in the body contact region was used as a parameter. The channel length is 0.5 μm. Vk increases with decreasing impurity dose in the drain offset region. Vk also increases with increasing impurity dose in the body contact region. This means that parasitic bipolar effect is suppressed by decreasing the impurity doses in the drain offset and body contact regions.

The dependence of power-added efficiency and output power on the impurity dose in the drain offset region at the third-order intermodulation distortion (IM3) of -30 dBc is shown in Fig. 6 to evaluate the linear amplification characteristics. The channel length is 0.5 μm. The drain bias was 3.0 V. The frequency was 5.25 GHz. Power-added efficiency at the saturation output power (Psat) is also shown. Power-added efficiency at Psat increases with increasing impurity dose in the drain offset region because the on-resistance decreases. Power-added efficiency of 61 % was obtained at impurity dose in the drain offset region of 1 .6 x $10^{12}cm^{-2}$ at a Vdd of 3.0 V and frequency of 5.25 GHz. There is an optimum impurity dose in the drain offset region that gives the highest power-added efficiency and output power for IM3 of -30 dBc (under linear-amplification condition). This is, increasing the impurity dose in the drain offset region decreases the on-resistance and this increases the output power and power-added efficiency, but excessive increases in the impurity dose enhances the parasitic bipolar effect. The parasitic bipolar effect induces nonlinear characteristics in tranceconductance (gm) and drain conductance (gd). These nonlinear characteristics degrade the linear amplification characteristics.

The dependence of power-added efficiency and output power on impurity dose in the body contact region is shown in Fig. 7. The channel length is 0.5 μm. The drain bias was 3.0 V. There is an optimum impurity dose in the body contact region that gives the highest power-added efficiency at Psat because increasing the impurity dose in the body contact region suppress the parasitic bipolar effect but excessive increases in the impurity dose increases the on-resistance. The power-added efficiency and output power at IM3 of -30 dBc increase with increasing impurity dose in the body contact region because parasitic bipolar effect is suppressed with increasing it.

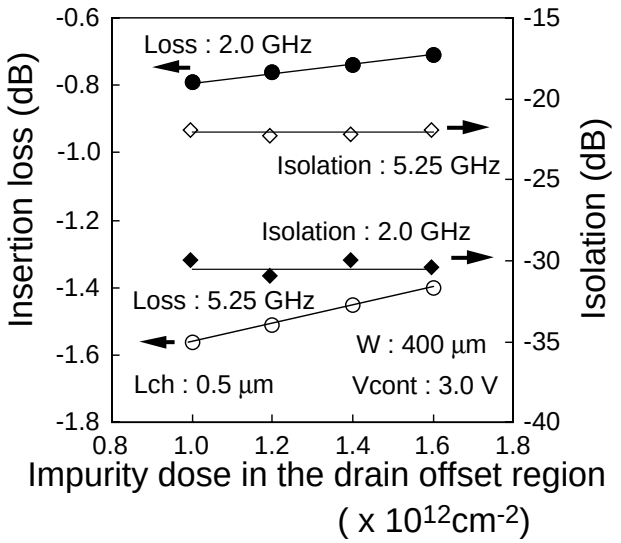

Fig. 8 Dependence of the insertion loss and isolation on the impurity dose in the drain offset region.

Dependence of the insertion loss and isolation on the impurity dose in the drain offset region is shown in Fig. 8 to evaluate the performance of the SPDT-switch. The gate control voltage was 3.0 V. Insertion loss at 2.0

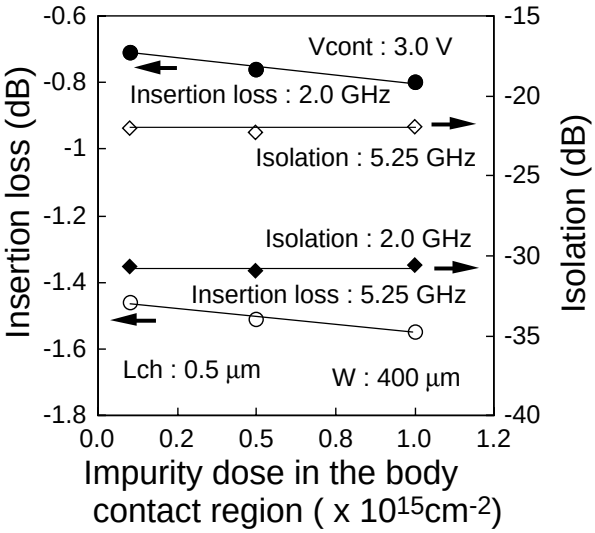

Fig. 9 Dependence of the insertion loss and isolation on the impurity dose in the body contact region.

GHz is smaller than that at 5.25 GHz and isolation at 2.0 GHz is larger than that at 5.25 GHz. The SPDT-switch performance at 2.0 GHz is better. Insertion loss decreases with increasing impurity dose in the drain offset region because the on-resistance dcrases as shown in Fig. 3. However, the isolation was almost the constant regardless of the impurity dose in the drain offset region. The insertion loss of -0.71 dB and isolation of -30 dB at a frequency of 2 GHz is almost the same as those of compound semiconductor devices.

The dependence of the insertion loss and isolation on the impurity dose in the body contact region is shown in Fig. 9. The gate control voltage was 3.0 V. Insertion loss increases with increasing the impurity dose in the body contact region because the on-resistance increases as shown in Fig. 4. However, the isolation is the almost the same regardless of the impurity dose in the body contact region.

The RF performances of the thin-film SOI power MOSFETs using high-resistivity Si substrate and conventional resistivity substrate are compared in Table 2. The DC characteristics, f_T, fmax, power-added efficiency, and linear amplification characteristics are almost the same. The insertion loss of the thin-film SOI power MOSFET fabricated using the high-resistivity Si substrate is lower and its isolation is slightly better. For the SPDT- switch, high- resistivity substrate is preferable.

4. Conclusion

Guidelines for designing high-efficiency operation at linear amplification and lower insertion loss in 5-GHz-band SOI power MOSFET were proposed. For linear amplification characteristics, there is an optimum dose in the drain offset region that gives the largest output power and highest power-added efficiency because there is a trade-off between the on-resistance and parasitic bipolar effect. The impurity dose in the body contact region should be as high as possible. For the SPDT-switch, the impurity dose in the drain offset region should be as high as possible taking into consideration of the breakdown voltage and the impurity dose in the body contact region should be as low as possible and a high-resistivity silicon substrate should be used as a supporting substrate.

Table 2 Comparison of the electrical performances of thin-film SOI RF power MOSFETs fabricated using high-resistivity and normal resistivity Si substrates.

	High-resistivity	Conventional
Substrate resistivity	> 1000 Ω • cm	10 ~ 30 Ω • cm
Threshold voltage	0.58 V	0.58 V
On-resistance (a	2.93 Ω • mm	2.95 Ω • mm
Breakdown voltage	15.2 V	15.2 V
Cutoff frequency (b	14.3 GHz	14.3 GHz
Maximum oscillation frequency (b	20.9 GHz	20.7 GHz
Power-added efficiency (c	58.1 %	57.6 %
Power-added efficiency (d	19.4 %	19.1 %
Output power (d	10.8 dBm	10.6 dBm
Insertion loss (e	-0.78 dB	-1.60 dB
Isolation (e	-30.6 dB	- 30.3 dB
Insertion loss (f	-1.55 dB	- 2.48 dB
Isolation (f	-22 dB	- 21.2 dB

Impurity dose in the drain offset region : 1.2 x 10^{12}cm^{-2}
a) Vg : 5.0 V
b) Vd : 3.0 V
c) f : 5.25 GHz, Vd : 3.0 V, Saturation output power
d) f : 5.25 GHz, Vd : 3.0 V, IM3 : -30dBc
e) f : 2.0 GHz, Vcont : 3.0 V
f) f : 5.25 GHz, Vcont : 3.0 V

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