Nano-Crystal Memory Devices Characterization using the Charge Pumping Technique

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Abstract

In this work, we present for the very first time, at our knowledge, results obtained by performing the two level charge pumping (CP) technique on nano-crystal memory devices. The charge pumping method allows the determination of the silicon dots characteristics such as their density, their spatial distribution within the dielectric and their effective diameter.

1. Introduction

Memory-cell structures employing discrete-trap type storage nodes, thus operating with a small finite number of electrons, have recently attracted much attention as very promising scalable ultra-dense low power memories [1], capable of exceeding the performance limits of conventional floating gate devices in terms of write/erase speed, endurance and refresh time. Because of its very high sensitivity, the charge pumping technique is an excellent tool to determine the characteristics of the traps within the dielectric of MOS transistors [2,3].

In this work, we investigate the charge pumping response of nano-crystal memory devices and we compare the electrical behaviour of silicon dots with that of SiO₂ traps. This analysis will allow the determination of the effective diameter and the spatial distribution of the dots.

2. Technological Details

Charge-trap memories used in this work are large area (W=L=10μm) n-channel Si-dot MISFETs. The tunneling insulating layer, T1, is a SiO₂ of different thickness (from 1.3 to 2.3 nm), thermally grown on Si(100) substrate. The silicon dots were self-assembled in a LPCVD system. After the fabrication of the Si-dot layer, the memory samples were completed by depositing a 8 nm-thick SiO₂ (T2) over the dots. The

studied devices are referenced as D-x, where x is the tunneling dielectric thickness T1 expressed in nanometers (c.f. Table 1). Reference devices (named "Ref") without dots have also been fabricated. The mean diameter of the dots is about 3 nm with a size dispersion inferior to 30% and the dot density is around 2-4×10¹¹ cm⁻².

Sample	D-1.3	D-1.5	D-1.8	D-2.3
T1(nm)	1.3	1.5	1.8	2.3

Table 1: Summary of samples and corresponding tunneling dielectric thickness (T1).

3. Charge pumping experimental results

Fig. 1 shows that the sinusoidal two level charge pumping current versus the minimum of the gate signal, I_{CP}(V_{GBI}), performed on the reference device, has a traditional shape [3]. Moreover, the maximum charge pumped has a linear dependence with the frequency (Fig. 2).

Figure 1: Two level charge pumping current versus the minimum value of gate pulse for the reference device and for the memory device D-1.3 ($DV_{GB}=2.5V$, $F=100KHz$).

This means that there are no traps at the interface between the two dielectric layers (i.e. T1 and T2) but all the measured traps are at the interface between T1 and the bulk. The trap density and capture cross section extracted for the reference device are $3.4 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ and 10^{-17} cm^2 respectively, which are usual values for a standard process.

The $I_{CP}(V_{GBI})$ characteristic performed on the device D-1.3 (Fig. 1) clearly shows an additional contribution, due to the presence of the silicon dots. Fig. 2, with $\Delta V_{GB}=3\text{V}$, puts in evidence the increase of the charge pumped at low frequencies. Indeed, at low frequencies, the device is polarised for a longer time in strong inversion and accumulation regimes so that the traps far away from the interface are able to respond.

Another possibility to probe the traps far away from the interface, at a given frequency, is to increase the gate pulse amplitude, in order to increase the free carrier densities at the interface during the strong inversion and accumulation regimes. This is also shown in Fig. 2, where three different regions can be clearly detected: (I) no response of the traps far away from the interface and complete response of the interface traps, (II) partial response of the traps far away from the interface, (III) complete response of the traps far away from the interface.

Figure 2: Charge pumped versus the pulse frequency for the memory device D-1.3 with several gate pulse amplitudes ($\Delta V_{GB}=2\text{V}, 3\text{V}, 5\text{V}, 6\text{V}, 6.5\text{V}$).

From the linear shape of the region (III), for $\Delta V_{GB}=6.5\text{V}$, it is possible to extract the trap density far away from the interface and a good approximation of the capture cross section. These values have been found equal to $1.9 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$, and $1.23 \times 10^{-22} \text{ cm}^2$, respectively. Indeed, this last value (σ_{nT1}) correspond to the capture cross section of the traps (located at the distance T1) seen from the interface with the silicon. We can determine the true capture cross section of the traps (σ_n) by taking into account the WBK transparency and the following equation [4]:

$$\sigma_{nT1} = \sigma_n \exp\left(-\frac{T1}{\lambda_n}\right) \quad (1)$$

where λ_n is the tunnelling constant which depends on the effective mass and barrier height of carriers. We found finally $\sigma_n=9.5 \times 10^{-16} \text{ cm}^2$ for the traps located at 1.3nm from the interface, which is close to the value previously found for the traps situated at the T1/bulk interface.

Fig. 3 illustrates the two level charge pumping measurements (with a square gate pulse) performed on the different silicon dots devices. An additional hump on the traditional plateau [2] due to the interface traps, located at the right of $I_{CP}(V_{GBI})$ curve clearly appears.

Figure 3: $I_{CP}(V_{GBI})$ curves performed on different samples with a square gate pulse $F=100\text{Hz}$, $\Delta V_{GB}=6\text{V}$.

4. Simulations

In order to understand these results we have performed some simulations. In particular, in a first time we have considered that the additional response was due to the contribution of traps around the dots or to a “trap-like behaviour” of the dots while, in a second time, we have assumed that the additional response was due to the tunnelling of electrons or holes between the bulk and the dots.

The $I_{CPA}(V_{GBI})$ curve of Fig. 4 shows the contribution of the traps located at the interface between T1 and the bulk. This curve corresponds to a classical “bell” shape with a plateau. The $I_{CPB}(V_{GBI})$ curve shows the contribution of the traps located at 1.3 nm from the interface. In this case we observe that the hump is located at the left of the plateau. Indeed, this is due to the better capability of tunnelling through the dielectric for electrons compared to holes. These results indicate that the additional contribution is not due to a classical Shockley-Read-Hall (SRH) response of the traps located around the dots, consequently excluding a dots’ “trap-like” behaviour. On the contrary, the $I_{CPC}(V_{GBI})$ curve shows the contribution of the dots located at 1.3 nm

from the interface, once they are filled and emptied by the electrons which tunnel from/to the bulk. In this case the hump is located on the right of the plateau, agreeing with the experimental data. Indeed, during a CP cycle the following phenomena takes place: in strong inversion, the electrons tunnel from the substrate to the dots, which are initially intrinsic. As a consequence, the dots become almost degenerated. When the device is polarized in accumulation, the electrons tunnel from the dots to the bulk (with a better ability than from the bulk to the dots due to the Fermi level position in the dots) where they recombine with holes. Finally, the I_{CPD} curve, corresponds to the hole tunneling contribution which is considerably lower than the electron contribution and can therefore be neglected. These simulations coupled to the experimental data clearly demonstrate that the dots present a "floating-gate like behavior", as it has been invoked in previous works [5].

Figure 4: Simulations of the contribution of the interface traps (I_{CPA}) and of the traps located at 1.3 nm from the substrate within the dielectric (I_{CPB}). Simulation of the contribution of the dots if we assume a classical tunneling of electrons (I_{CPC}) or holes (I_{CPD}). Parameters have been fixed as follows: $S_{np}=10^{-17} \text{ cm}^2$, $DV_{GB}=6\text{V}$, $V_{FB}=-1\text{V}$, $V_T=0.3\text{V}$, $F=10 \text{ KHz}$.

5. Dots parameter extraction

We will now apply the CP theory to the Silicon dots devices. It is well known that the use of the CP technique with a square gate pulse allows the determination of the spatial distribution of the traps within the dielectric [3]. With this kind of signal the emission phenomenon from the traps can be neglected, being the capture phenomenon the limiting factor. Based on the classical SRH theory, we can express the current resulting from the electron capture as [6]:

$$j_{\text{trap}} = \sigma_n Q_n F_{\text{imp}} T_E \quad (2)$$

where Q_n is the inversion charge, F_{imp} the impact frequency ($\approx 10^{13} \text{ Hz}$), σ_n the capture cross section of the trap and T_E the transparency of the oxide T1 (which

depends on the electric field in the WKB approximation). The current due to the tunneling of electrons to the silicon dots can be expressed as:

$$j_{\text{tun}} = S_{\text{eff}} Q_n F_{\text{imp}} T_E \quad (3)$$

where S_{eff} is the effective area of the dots. From Eqs. 2 and 3, it is clear that the effective area of the dots plays the role of the trap capture cross section. If we consider a square gate pulse, the emission of the electrons to (or from) the dots occurs during half of the measurement period. In the strong inversion regime, for a given polarization, the time constant of the dots which can respond is lower than the half period of the gate signal ($1/2F$, being F the gate signal frequency) and we obtain from Eq. 3:

$$\frac{q}{S_{\text{eff}} Q_n F_{\text{imp}} T_E} < \frac{1}{2F} \quad (4)$$

As a first approach, we can assume that all the dots are at the distance T1 from the bulk, and that the variation of Q_{CP} is due to a non-constant value of S_{eff} for the dots. From the measurement of $Q_{CP}(F)$, it is possible to determine the variation of S_{eff} (or of the effective diameter D_{eff}) and the histogram of the density of dots, D_{dot} (given per surface unit), versus S_{eff} using the following set of equations:

$$\begin{cases} S_{\text{eff}}(F) = \frac{2qF}{Q_n F_{\text{imp}} T_E} \\ D_{\text{dot}}(F) = \frac{1}{qA_{\text{eff}}} (Q_{CP}(F) - Q_{CP}(F - \Delta F)) \end{cases} \quad (5)$$

where A_{eff} is the surface of the device and ΔF is the frequency step.

A typical evolution of the pumped charge versus the gate pulse frequency (here for the device D-1.3) is shown at Fig. 5. The increase of the charge pumped at low frequency is due to the contribution of the dots. The Fig. 6 presents the histogram $D_{\text{dot}}(D_{\text{eff}})$ and shows that the effective mean diameter is close to 3 nm which agrees with the device technological characteristics.

A second approach is the following. From the variation of the maximum charge pumped versus the frequency (with a square gate pulse) and considering a constant value of σ_n ($=9.5 \times 10^{-16} \text{ cm}^2$, as previously found), we can estimate the spatial distribution of the dots within the dielectric [3].

This result is illustrated in Fig. 7 where the dot densities can be extracted by integrating the curves (c.f. Table 2). These values, as well as the position of the maximum density of the dots, are in good agreement with the device technological characteristics.

Finally, we can suppose that the real spatial distribution and the effective diameter of the dots is a mix between the curves $N_{\text{dot}}(x)$ and $D_{\text{dot}}(D_{\text{eff}})$.

Figure 5: Evolution of the charge pumped versus the frequency of the square gate signal ($\Delta V_{\text{GB}}=6\text{V}$) for the device D-1.3.

Figure 6: Histogram of the density of the dots versus their effective diameter.

Figure 7: Spatial distribution of the dots within the dielectric.

Sample	D-1.3	D-1.5	D-1.8	D-2.3
Dot Density ($\times 10^{11} \text{cm}^{-2}$)	2.3	4	4.2	–

Table 2: Estimated values of the dot density for the different samples.

6. Summary

In summary, the nano-crystal memory devices have been characterized for the very first time, at our knowledge, by means of the charge pumping technique. Experimental results and simulations demonstrate that the response of the silicon dots does not correspond to a "trap-like" behavior but it is closer to a "floating gate like" behavior, confirming results of previous works [5]. Moreover, we have shown that the use of the CP technique with a square gate pulse allows the determination of the spatial distribution of the dots within the dielectric, the extraction of the effective surface of the dots and an estimation of the silicon dots density. The determination of the distribution of the Si-dot density as a function of the effective diameter, $D_{\text{dot}}(D_{\text{eff}})$, can be used to evaluate the effective shape repartition of the dots for a given process.

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