Reducing the Threshold Voltage Deviation for Sub-100 nm Transistors using Midbandgap-Gatematerials

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Abstract

Throughout the progressive miniaturization in microelectronics the processing of integrated-circuit elements must be very exacting. The 2001 update of the International Technology Roadmap for Semiconductors predicts minimal feature sizes down to 30 nm for the year 2014 [1]. At the same time the operating voltage should be decreased from actually 1.5 V down to 0.6 V and the $3\sigma$ threshold voltage deviation from 50 mV to 17 mV. The latter is most critical, as the deviation of the threshold voltage normally increases with decreasing geometrical dimensions.

This paper describes the advantages in the use of midbandgap materials substituting polysilicon as gate electrode. Using a deposition and etchback technique, transistors with gatelengths in the sub-100 nm region have been fabricated with excellent homogeneity over a 100 mm wafer. Due to their working functions one material can be applied for both NMOS- and PMOS-transistors. In addition to this process simplification, the channel implantation can be reduced and thereby the threshold voltage deviation decreases.

1. Introduction

Belonging to the progressive development of microelectronic components, whenever limitations have been surmounted the MOS-process is limited by other parasitical effects. Most critical are physical limitations as for example the threshold voltage deviation, which is based upon the statistical effect of the channel doping [2]. Through the scaling of the gate area the doping per unit area is constant but the absolute deviation is increasing.

The use of Metals with working functions in the middle of the bandgap of silicon as gate material makes it possible to decrease the threshold voltage deviation although decreasing channel length and width.

In addition to this there is still the advantage of process simplification in the application of metal gates. Due to their high conductivity the doping step necessary for polysilicon layers can be omitted and one metal layer can be applied for both NMOS and PMOS transistors.

This article first describes the preparation of Sub-100 nm transistors with metal gates using a modified LPCVD-deposition (low pressure chemical Vapour deposition) and RIE-etchback (reactive ion etching) technique. With this technique only standard process steps and conventional optical lithography are necessary to produced structures down to 25 nm. Therefore this structure definition technique is simply transferable to any technology line.

In the third section of this article the processed devices are electrically characterised. This is the first time that NMOS transistors with pure molybdenum silicide gate have been fabricated to utilize the major advantages of midbandgap gate materials. For these metal gate transistors with a gatelength of 90 nm we present I-V characteristics in comparison to that of polysilicon gate transistors with comparable dimensions.

2. Device preparation

Metals of interest for MOS processing are aluminium, tungsten, molybdenum, titanium nitride, copper and some silicides of these metals. Most suitable are metals with a work function near the middle of the bandgap of silicon ($\phi = 4.61$ eV); the so-called midbandgap materials. Thus the MOS processing is simplified by using one midbandgap gate material instead of two different doped polysilicon layers respectively for NMOS- and PMOS-transistors. Suitable from the above-mentioned metals are tungsten, tungsten silicides, molybdenum, molybdenum silicides and titanium nitride.

At increased temperature most pure metals tend to form silicides or produce stress as a consequence of a different expansion coefficient in comparison to the oxide subsoil. So the deposition and etchback technique used for the definition of sub-100 nm polysilicon structures [3,4] has to be modified. TEOS-oxide and LPCVD-nitride layers are not suitable as sacrificial and masking layers, due to their high deposition temperatures beyond 600°C.

An alternative is expected by replacing them with aluminium and a special low temperature oxide (LTO) which is deposited from a diethylsilane (DES) and oxygen gas mixture in an LPCVD-process at 410°C.
Fig. 1 represents this modified structure definition technique for nanometer scale dimensions on top of a crystalline silicon wafer. After gate oxidation and metal deposition aluminium is vapour deposited as sacrificial layer. Using optical lithography and an anisotropical RIE step the aluminium is etched selectively down to the polysilicon layer (Fig. 1A). After resist stripping an LTO layer is conformally deposited on top (Fig. 1B). A second RIE step is performed removing the LTO from the lateral wafer surface (Fig. 1C). This etching step must be absolutely anisotropic to conserve the oxide spacer surrounding the sacrificial aluminium. The width of the oxide spacer, which is identical with the subsequent masking layer for gatelength definition, is determined by the thickness of the deposited LTO layer. Next the sacrificial aluminium layer has to be removed by a mixture of phosphoric and nitric acid in a wet chemical process most selective to the oxide spacer and the metal surface (Fig. 1D). At last the metal gate is structured by a chlorine anisotropical RIE step with high selectivity to the oxide mask and the gate oxide (Fig. 1E).

Applying this low temperature technique nanometer scale lines of molybdenum silicides depicted in figure 2, of titanium nitride and tungsten have been structured using a Cl2/SiCl4-RIE step for metal etching which has a high selectivity to silicon oxide. The molybdenum silicides line has 80 nm width at the top which is slightly decreasing towards the bottom. This can be suppressed by reducing the chlorine component of the plasma.

Comparable results have been achieved with other metals such as tungsten. Except titanium nitride has a triangular cross section caused by its superior hardness and the resulting longer etching time.

By integrating this technique into the MOS process transistors with sub-100 nm metal gates have been produced in combination with transistors with lithographically defined gatelengths. The electrical characterization of these is described in the following section.
3. Electrical Characterization of the Sub-100 nm-MoSi$_2$-Gate-Transistors

The best results after etching the metal layer are given from molybdenum silicide. Hence this midbandgap material has been selected for NMOS transistor processing.

The electrical input characteristic of a molybdenum silicide gate NMOS transistor is presented in figure 3. The geometrical dimensions of this transistor are a gate length $L$ of 90 nm, a channel width $W$ of 100 µm, a gate oxide thickness of 7 nm and a spacer width of 80 nm.

The doping impurities for these first samples are chosen nearly as reported in [5]. So the LDD implant is $5 \times 10^{12}$ cm$^{-2}$ with 20 KeV of antimony and the D/S implant is $5 \times 10^{15}$ cm$^{-2}$ with 60 KeV of arsenic. For the channel doping profile we used two boron implantations with a dose of $1 \times 10^{13}$ cm$^{-2}$ with 40 KeV as anti-punch-through implantation and $3 \times 10^{12}$ cm$^{-2}$ with 10 KeV to adjust the threshold voltage. All dopants are activated by rapid thermal annealing at 650°C for 20 s, but this temperature is only valid for our self-built facility.

To analyse subthreshold characteristics figure 4 shows the typical input characteristic for a 90 nm MoSi$_2$-gate transistor with logarithmic scale of the drain current. The three different parts of the curve - weak inversion, strong inversion and velocity saturation - can be clearly distinguished.

Below a gate source voltage of 0,5 V, there can be measured a reverse current resulting from the reverse currents of the pn-junction of drain and bulk and the pn-junction of source and bulk. With rising voltage the form of the curve is linear until reaching the threshold voltage at about 1,3 V.

The sub-threshold-slope of this transistors is $S = 125$ mV/decade. Though values for the sub-threshold slope in the region of 80 mV/decade are desirable the device shows a good functionality.

| Table 1. Process parameter of the NMOS-transistors with molybdenum silicide gate |
|---------------------------------|-----------------|
| parameter                      | Value           |
| gate length                    | 90 nm           |
| gate width                     | 100 µm / 10 µm  |
| gate oxide thickness           | 7 nm            |
| spacer width                   | 90 nm           |
| boron channel doping           | $3 \times 10^{12}$ cm$^{-2}$ 10 KeV |
|                                | $1 \times 10^{13}$ cm$^{-2}$ 40 KeV |
| LDD implantation               | $5 \times 10^{12}$ cm$^{-2}$ 20 KeV |
| D/S implantation               | $5 \times 10^{15}$ cm$^{-2}$ 60 KeV |
| activation of dopant ions       | RTA, 650°C, 20s |

In comparison to these parameters, the threshold voltage of polysilicon-gate-NMOS-transistors with 70 nm gate length and nearly the same process parameters is 0,65 V [5]. So as proposed by the theory for midbandgap gate materials the channel doping of the molybdenum silicides transistors can be decreased by at least one decade to reach threshold voltages near 0,5 V.

Breakdown of this transistor, taken from the output characteristic in figure 5, occurs at drain-source voltage of 3.3 V due to punch through.
4 Threshold voltage deviation

To determine the threshold voltage variation, the threshold voltage is measured at 64 transistors arranged in an array of 8 lines and 8 rows in a common-source layout. The choose of a transistor is done by feeding the drain-source voltage to one of the 8 lines and the gate-source voltage to one of the 8 rows. In comparison to a single transistor measurement the reverse drain current of the 7 other transistors is overlaying the measured drain current. Thus it is not possible to measure subthreshold characteristics of only one transistor in this layout.

In comparison to the results of Ref. [5] the subthreshold deviation is six times larger than that of polysilicon transistors. For more concrete measurements, it is useful to process transistors with both types of gate material and with the same dimensions to compare their characteristics.

In conclusion a simple way to integrate alternative nanometer scale metal gates on silicon has been demonstrated. The next step is reducing the channel implantation to adjust a lower threshold voltage for the midbandgap transistors. After this reduction the threshold voltage deviation has also to be measured for these transistors.

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6 References


Figure 6. Threshold voltage deviation of 90 nm MoSi$_2$-gate transistors; $\text{L} = 10 \, \mu\text{m}$

Figure 6 shows a histogram of the threshold voltage of 90 nm molybdenum silicide NMOS transistors with gatewidth of 10 $\mu$m. The mean value of the threshold voltage is 1.67 V, the standard deviation is 65.2 mV. A Gaussian curve that bases on these values is overlaying the bar graph.

In comparison to the results of Ref. [5] the subthreshold deviation is six times larger than that of the 70 nm polysilicon gate transistors with the same width of the gate electrode.

One reason for this may be the gate oxide thickness, which is two times larger than that of the polysilicon transistors. To compare both types of transistors a new charge of wafers has to be started where polysilicon and molybdenum silicide transistors are processed with the same parameters.

5 Conclusions

The quality of the deposition and etchback technique to integrate metal gates with sub-100 nm linewidth in a standard CMOS process with superior homogeneity and reproducibility has been demonstrated. This technique is capable to replace critical resist mask levels like transistor’s lenght and width definition. For metal layers which are heat sensitive a low temperature technique on the base of an aluminium vapour deposition and a LPCVD / LTO process at 410°C is available for nanometer scale structure definition. Using a standard resist mask in combination with the presented deposition and etchback technology it is possible to integrate both, gate electrodes with lithography defined and nanometer scale geometries on the same chip.

First devices of sub-100 nm-NMOS-transistors with molybdenum silicide gate have been processed on top of 100 nm silicon wafers. These devices show typical input- and output-characteristics comparable to polysilicon-gate-transistors of the same dimensions.

The threshold voltage deviation is much higher than that of polysilicon transistors. For more concrete measurements, it is useful to process transistors with both types of gate material and with the same dimensions to compare their characteristics.

In conclusion a simple way to integrate alternative nanometer scale metal gates on silicon has been demonstrated. The next step is reducing the channel implantation to adjust a lower threshold voltage for the midbandgap transistors. After this reduction the threshold voltage deviation has also to be measured for these transistors.