A New S-parameter Measurement-Based Method for MOSFET Gate Resistance Extraction

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Abstract

A method to extract the MOSFET’s gate resistance directly from S-parameter measurements is presented and demonstrated on an advanced 0.18μm CMOS technology. Unlike previously reported methods, the one proposed here facilitates the extraction of the gate resistance when the distributed effect of the intrinsic channel resistance is taken into account. Measurements performed on transistors with different geometries are used to show the good agreement between extracted values and those calculated from transmission line theory.

1. Introduction

It is well known that the effect of the MOSFET gate resistance ($R_g$) has to be taken into account for RF and noise modelling due to its strong influence on the input port impedance. The origin of this resistance clearly comes from the poly-silicon resistive electrode, but its effect in the input port is often analysed together with the distributed effect of the intrinsic channel resistance ($R_i$) [1]. When modelling MOSFET behaviour at RF, however, it is preferable to use the actual physical value for each parameter in order to maintain the model scalability.

Nowadays, in most of the RF models, $R_g$ is obtained from the simple calculation derived from transmission-line theory [2]. In reference to Fig. 1 this is:

$$R_g = R_{sh} \cdot \frac{W_f}{3L_f NF}$$

(1)

where $NF$ is the number of gate fingers, and $R_{sh}$ is the poly-silicon’s sheet resistance. However, the determination of $R_{sh}$ can be difficult since it is dependent on the poly-silicon mask length, which is due to differences in the thickness of the gate salicide. Additionally, for RF applications the use of irregular gate layouts is very common; in such cases, poly-silicon lines are often used to interconnect the gate fingers. This complicates the calculation of $R_g$ due to the increase of the access resistance coming from the contact, which does not exhibit the distributed effect, and therefore is not divided by 3.

Alternatively, several methods have been proposed to extract $R_g$ from S-parameter measurements. In [1], $R_g$ is found by subtracting the effect of the source and drain resistances from $Re(Y_{11})$. Nevertheless, the extracted value for $R_g$ using this approach includes the effect of $R_i$, showing a clear bias dependency. In order to neglect the influence of $R_i$ in the measured S-parameters, in [3] the MOSFET is biased at $V_{gs}=V_{ds}=0$, and $R_g$ is determined by using $R_{g}=Re(Z_{11})-Re(Z_{12})$. However, $Z_{11}$ fluctuates considerably when the transistor is off due to the high gate to source impedance. Thus, the selection of a proper frequency to perform the extraction can be very difficult. In order to avoid this problem, it was proposed in [4] to use the same approach, but biasing the transistor in strong inversion and keeping $V_{ds}=0$. Due to the effect of $R_i$ in $Z_{12}$ when the transistor is on, the extractions carried out by applying this method differ from the real values. The method proposed in [5] is based on the same concept, but the effect of $R_g$ is included in the $Z$-parameters by calculating it from the channel resistance ($R_{ch}$). This approach is valid, but the calculation of $R_{ch}$ involves several unknown parameters such as mobility, effective dimensions, and threshold voltage. In consequence, the extraction becomes more complicated.

In this paper, we present a method that overcomes the drawbacks of the previously reported approaches. The extraction of $R_g$ is entirely based on S-parameter measurements, and additionally, the effect of the intrinsic channel resistance is taken into account. Hence, this method is valid for transistors with a great variety of layouts, even for long channel lengths.
2. Gate resistance determination

Fig. 2 shows the equivalent circuit of a MOSFET biased at $V_{ds}=0$ V showing the input and output ports. In this circuit, the inductive terminal elements are ignored due to their low value (a few pH). Furthermore, the substrate equivalent network is neglected since the value of the series resistances $R_i$ and $R_s$ is much smaller than the source/drain-bulk junction capacitances. The real part of the Z-parameters associated to this circuit is given as [6]:

$$\text{Re}(Z_{11}) = R_s + R/2 + R_s/3 + R_i$$

(2)

$$\text{Re}(Z_{21}) = \text{Re}(Z_{11})/2 + R_i$$

(3)

$$\text{Re}(Z_{22}) = R_s + R_s/3 + R_i$$

(4)

In order to express $\text{Re}(Z_{11})$ in terms of $R_s$, $R$, and $R_s$ only, an alternative definition for (2) can be used:

$$\text{Re}(Z_{11}) = R_s + R_s/3 + R_i$$

(5)

where $R_s$ is assumed to be a linear function of $R_s$ [7]. Hence, the effect of $R_i$ is included in the 1/3 factor multiplying $R_s$, which is expected due to the distributed nature of the channel resistance. Solving (5) for $R_s$ yields:

$$R_s = \text{Re}(Z_{11}) - R_s/3 - R_i$$

(6)

For either wide or long channel transistors $R_s$ is very low compared to $R_i$. Hence, the following assumption is valid:

$$R_s/3 + R_s/3 = R_s/3 + R_i$$

(7)

where $R_s$ is the total series resistance given by $R_s + R_i$. Therefore, equation (6) can be simplified to:

$$R_s = \text{Re}(Z_{11}) - \text{Re}(Z_{22})/3$$

(8)

For the case of transistors with a symmetrical layout, where $R_s = R_i/2$, the error introduced by (8) in the extraction of $R_s$ is $R/3$, which is insignificant as it is shown in Section 4.

3. Experiments

On-wafer small signal S-parameter measurements at $V_{ds}=0$ V and $V_{gs}=1.8$ V were performed for 10 NMOS devices fabricated in a 0.18 μm process with an oxide thickness of 3.5 nm and salicided poly-silicon. The measured devices have two gate fingers based on the layout shown in Fig. 1, the distance between the contact and the active region was selected as the minimum according to the design rules in order to reduce the resistance coming from the contact. The transistors are located in two different arrays. In the W-array, the finger width takes values of 5, 15, 20, 25 and 30 μm, while the finger length is kept constant in 0.18 μm. For the L-array, the finger length takes values of 0.18, 0.2, 0.5, 1 and 2 μm, and the finger width has a constant value of 20 μm. The measurements were performed using an HP 8510 Network Analyzer and corrected for the interconnect and bondpad parasitics by using a three-step de-embedding method [8].

In addition, the resistance of different salicided poly-silicon lines was measured on-wafer in order to obtain the sheet resistance as a function of the poly-silicon mask length. These measurements allow the accurate calculation of the gate resistance for each device by applying (1). Therefore, the calculated values for $R_s$ can be used to compare the extractions with actual data. As shown in Fig. 3, if interpolation is applied, there is a change of around 10% between the sheet resistance obtained for the minimum (0.18 μm) and maximum (2 μm) finger length used in the devices. For this reason, using a constant value for $R_s$, as extracted from example a van der Pauw test structure, introduces an error in the estimation of $R_s$ for different finger lengths.

4. Extractions

The gate resistance was extracted for the devices described above by using the proposed method and also those presented in [4] and [5]. Additionally, the results were compared to the values obtained by using (1). De-embedded S-parameters were converted to Z-parameters and the real parts of $Z_{11}$ and $Z_{22}$ were plotted.
in a frequency range from 1 to 25 GHz in order to observe the interval where these parameters show a plateau. The graphics corresponding to the device with \( W = 25 \mu m \) and \( L = 0.18 \mu m \) are shown in Fig. 4. As can be seen, \( \text{Re}(Z_m) \) is independent of frequency, but \( \text{Re}(Z_m) \) presents a variation due to the effect of the gate to source capacitance in the input impedance. However, \( \text{Re}(Z_m) \) maintains an approximate constant value in the frequency range between 5 and 10 GHz. Therefore, due to the fact that the tendency of \( \text{Re}(Z_m) \) and \( \text{Re}(Z_m) \) is approximately the same for all the short channel devices measured \( (L \leq 1 \mu m) \), the extractions were performed at a frequency of 7 GHz. Bear in mind, however, that it is necessary to observe the data corresponding to \( \text{Re}(Z_m) \) before selecting the frequency for the extraction, specially for long channel transistors, where the frequency response is much lower.

The extractions of \( R_s \) keeping the finger length constant and varying the finger width are shown in Fig. 5. A good correspondence with the calculation generated from equation (1) is observed by applying the proposed method and also those presented in [4] and [5]. However, for the case explained in [5] it is necessary to calculate the channel resistance from:

\[
R_{ch} = \frac{L_{eff}}{\mu W_{eff}(V_{gs} - V_T)} \tag{9}
\]

Hence, once the source resistance is obtained by solving (3), the gate resistance can be calculated directly from (6).

As a consequence, the complexity of the extraction presented in [5] is much higher than in the other approaches, due to the difficult determination of the mobility, the threshold voltage, and the effective dimensions for short channel transistors.

On the other hand, for the W-array the method presented in [4] shows a good agreement between extracted and calculated values. This is due to the weak influence of the intrinsic channel resistance for large \( W/L \) ratios. However, the deviation increases for longer channels. This can be clearly seen in Fig. 6, where the extracted values for \( R_s \) are performed using the L-array. In this case, the extractions carried out by using the proposed method and that presented in [5] show good agreement with the values predicted by using (1), but applying the method in [4] yields wrong data when the channel length is increased. For long devices, this method becomes inapplicable, yielding negative values for the gate resistance.

The deviation of the extracted data using the method presented in [4] is due to the high value of the channel resistance for long devices. Therefore, the assumption \( R_s = \text{Re}(Z_m) - \text{Re}(Z_m) \) is no longer valid, which can be demonstrated by subtracting equation (3) from equation (5):

\[
\text{Re}(Z_m) - \text{Re}(Z_m) = R_s - R_s / 6 \neq R_s \tag{10}
\]

According to (10), the error introduced by the use of the method in [4] can also be large when the gate resistance is very small compared to the channel resistance.

Based on this discussion, the use of the new method for the extraction of \( R_s \) is recommended due to its simplicity and reliability. Nevertheless, an additional analysis was performed in order to show the accuracy of the proposed method. As it has been explained above, the difference between the extracted and the actual value for the gate resistance is around 1/3\( R_s \) for transistors with a symmetrical layout, such as the devices measured here. Hence, the channel resistance was calculated from (9) and \( R_s \) from (3) for all the measured transistors. With these values, the impact of 1/3\( R_s \) in the total
gate resistance value was examined. For the W-array, the impact of $1/3R_s$ in $R_g$ showed the maximum effect in the structure with $W_f=5$ μm, yielding a 2% of the total gate resistance as can be seen in Fig. 7. This percentage was reduced to less than 0.1% for the structure with $W_f=30$ μm. In the case of the L-array, this impact was from 0.2% for the shortest structure to 1.5% for the longest one. These results demonstrate the accuracy of the new extraction method presented here.

5. Conclusions

A new S-parameter measurement-based gate resistance extraction method has been presented and demonstrated. The results and comparisons carried out in this work show a good agreement between extracted values and those predicted by transmission line theory.

Since the gate resistance is a crucial parameter for RF and noise modeling, the simplicity of the method presented here represents an additional advantage over the methods that try to take into account the effect of the intrinsic channel resistance in the gate resistance extraction. For this reason, the new method is a reliable alternative to extract this resistance for MOSFETs with several layouts, including multi-fingered and double-sided connected structures.

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7. References


