A Comparative Analysis of Active and Passive Pixel CMOS Image Sensors

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Abstract

CMOS imagers performance becomes critical whenever illumination reaches very low and very high optical energy levels because of the reduced signal-to-noise ratio (SNR) and blooming immmunity, respectively. In this paper we present a comparative analysis with respect to the above issues of the two major architectures used in implementing optical sensor arrays in CMOS technology: the Active Pixel Sensors (APS) and Passive Pixel Sensor (PPS) schemes. Based on both physical simulation and circuit analysis, the trade-offs between the two architectures with respect to the design constraints are highlited.

1. Introduction

Implementing imagers in CMOS technology, in either small or large arrangements, has become very common for a wide range of applications and particularly in embedded systems. Over the last 10 years, the Active Pixel Sensors architecture has become a dominant choice for implementing advanced CMOS cameras and large number of examples have been presented [1]. However, PPS schemes have recently drawn attention in literature [2] since they presents a feasible method for achieving high-density imaging arrays with high quantum efficiency due to their intrinsically greater cell fill-factor and simplicity of implementation. Sophisticated PPS structures can even be used for very short integration times [3]. Even if advantages of APS over PPS have been frequently cited, no systematic comparative analysis have been presented on the subject to our knowledge.

To make a significant comparison between APS and PPS architectures, we referred to typical readout schemes as illustrated in Fig.1 and 2. In the PPS architecture, the photodiode is left floating for a certain amount of time, called integration time, where optically generated carriers are integrated in a charge across the photodiode. At the end of the integration time, the charge is readout by using a charge amplifier determining the reset of the photodiode. Conversely, in the APS architecture, the charge is readout by sensing the voltage drop across the photodiode with a source-follower. A reset transistor has to be implemented on each cell since the readout procedure does not remove the accumulated charge.

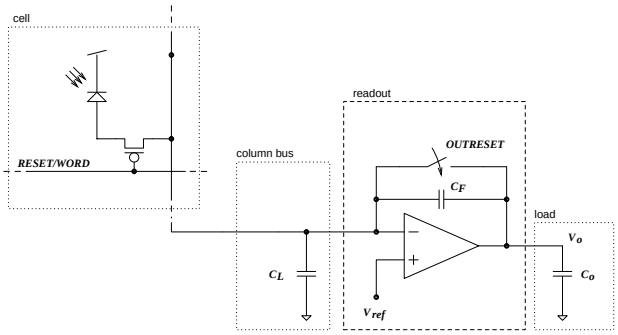

Figure 1. Simplified PPS architecture

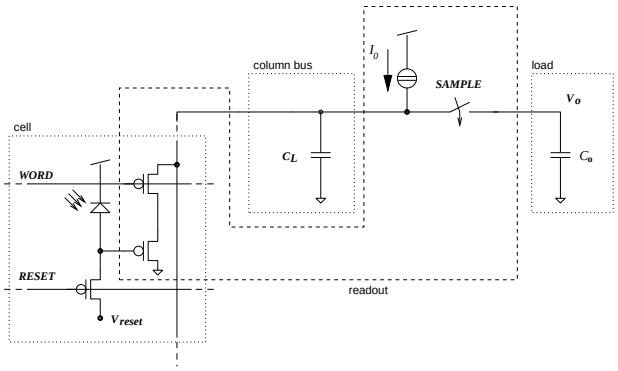

Figure 2. Simplified APS architecture

2. Thermal noise considerations

To compare the two architectures, we will not take into account $1/f$ noise, since it can be significantly reduced by a correlated double sampling (CDS) approach [7]. We also assume reset and readout noises at stationary points of operation, i.e. estimated at time intervals that are greater than any time-constant of the circuit. Even if this is not strictly true, it can be shown that it can be considered (es-

pecially for the reset noise) as a slight worst case [5] which is still significant to compare the two approaches. Before evaluating the signal-to-noise ratio (SNR) of the two configurations, we derived the equivalent thermal noise referred to the input of a charge amplifier for the PPS and of a source follower for the APS, respectively.

For the evaluation of the random noise in charge amplifiers, we will make the simplifying assumption that it is mostly generated by the noise due to the differential pair MOS transistors, represented by two gate-referred voltage sources whose mean square is: $\langle V_n^2 \rangle = \frac{8}{3}\frac{kT}{g_m}\Delta f$, where g_m is the transconductance of the MOS transistor [4]. Applying super-imposition of effects, random noise can be input-referred to an equivalent charge source applied to the charge amplifier of mean square:

$$\begin{aligned}\langle \delta Q_n^2 \rangle &= 2\langle V_n^2 \rangle (C_F + C_L)^2 = \\ &= (C_F + C_L)^2 \frac{16}{3}\frac{kT}{g_m}\Delta f,\end{aligned}$$

where C_F and C_L are the feedback and line capacitances as illustrated in Fig.1.

Assuming a single pole approximation for the operational amplifier,

$$H_{CA}(f) = \frac{V_o}{Qi}(f) = \frac{1}{C_F}\frac{1}{1 + j\frac{f}{f_{CA}}},$$

where Qi is the input charge, V_o the output voltage and

$$f_{CA} = A_0 f_0 \frac{C_F}{C_F + C_L} = \frac{1}{2\pi}\frac{g_m}{C_o}\frac{C_F}{C_F + C_L},$$

where A_0 and f_0 are the open loop gain and pole of the amplifier, respectively and C_o is the output capacitance [6]. We can refer the noise to the output of the amplifier and integrating over the frequency we get:

$$\begin{aligned}\langle V_o^2 \rangle_{CA} &= \int_0^\infty \langle \delta Q_{iN}^2 \rangle |H_{CA}(f)|^2 df = \\ &= \frac{4}{3}\frac{kT}{C_o}\frac{C_F + C_L}{C_F}. \qquad (1)\end{aligned}$$

Similarly we can get the output-referred noise expression of the source follower configuration used in APS. Using the transfer function of the source follower,

$$H_{SF}(f) = \frac{1}{1 + j\frac{f}{f_{SF}}} \text{ where, } f_{SF} = \frac{1}{2\pi}\frac{g_m^{'}}{C_L + C_o},$$

in which $g_m^{'}$ is the transconductance of the source follower transistor, we get the output-referred noise mean square voltage:

$$\begin{aligned}\langle V_o^2 \rangle_{SF} &= \int_0^\infty \langle V_N^2 \rangle |H_{SF}(f)|^2 df = \frac{8}{3}\frac{kT}{g_m^{'}}\frac{\pi}{2} = \\ &= \frac{2}{3}\frac{kT}{C_L + C_o}. \qquad (2)\end{aligned}$$

Expressions (1) and (2) are very useful to compare the APS readout (source follower) versus the PPS readout (charge amplifier) schemes:

$$\frac{\sqrt{\langle V_o^2 \rangle_{SF}}}{\sqrt{\langle V_o^2 \rangle_{CA}}} = \sqrt{\frac{C_F C_o}{2(C_o + C_L)(C_F + C_L)}}. \qquad (3)$$

Equation (3) shows how PPS readout scheme becomes critical for high values of C_L. Since C_L is monotonically related to the the number of pixel, relationship (3) shows advantages of APS with respect to PPS for large arrays. It is also interesting to note how (3) is a function of the capacitances and not of the readout time.

The signal-to-noise ratio can be estimated dividing the signal by the root mean square of noises in terms of equivalent number of electrons referred to the photosite element:

$$SNR = 20\log\frac{\overline{N_{opt}}}{\sqrt{N_{shot}^2 + N_{dark}^2 + N_{kTC}^2 + 2N_{readout}^2}}$$

where symbols are defined as the following table:

Table 1. SNR components

Symbol	Process	Mode	Electrons
			(Mean)
$\overline{N_{opt}}$	optical generation		$\frac{ASP_0T_{int}}{q}$
			(rms)
N_{shot}	shot noise		$\sqrt{\overline{N_{opt}}}$
N_{dark}	dark current noise		$\sqrt{\frac{I_{dark}T_{int}}{q}}$
N_{kTC}	photodiode kTC noise		$\frac{\sqrt{C_j kT}}{q}$
$N_{readout}$	readout noise	PPS	$\frac{\sqrt{\langle V_o^2 \rangle_{CA}}}{q\lvert H_{CA}(0)\rvert}$
		APS	$\frac{\sqrt{\langle V_o^2 \rangle_{SF}}}{q\lvert H_{SF}(0)\rvert}$

where A is the area of the photojunction, C_J is the photojunction capacitance, S is the sensitivity, P_0 is the incident optical power, T_{int} is the integration time and q is the electron charge. Note that the mean square readout noise has been doubled due to the CDS approach, usually implemented in both APS and PPS. To compare the two approaches, we make the assumptions that in PPS scheme kTC noises of the feedback capacitance C_F and of line capacitance C_L are made negligible by CDS. Furthermore, to make a fair comparison we have referred to the same pixel pitch of $20 \times 20\mu m^2$ implemented in a $0.7\mu m$ CMOS technology, where we assumed a fill-factor equal to 0.60 and to 0.40 for the PPS and APS pixels, respectively. The results of the comparison is displayed in Fig.3 where the advantages of the APS with respect to the PPS scheme for low light values are noticeable.

However, PPS and APS approaches converge at high light values, when shot noise becomes dominant with respect to other source of noise. The values of $1W/m^2$, $10^{-1}W/m^2$, $10^{-2}W/m^2$ and $10^{-4}W/m^2$ are related to

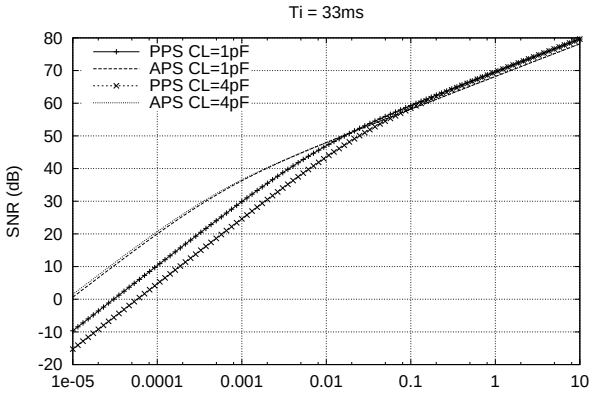

Figure 3. APS versus PPS signal to noise ratio. $A_0 = 1000$, $C_o = 1pF$, $C_F = 150fF$, $C_j(PPS) = 130fF$, $C_j(APS) = 100fF$ and $T_{int} = 33m$sec. $C_L = 1pF$ and $C_L = 4pF$ corresponds approximately to a 128×128 and 512×512 pixel array in $0.7\mu m$ technology, respectively.

illuminations of an overcast day, indoor office, twilight and full moon, respectively. Note how curves follows a 20dB/decade slope at low light levels and 10dB/decade slope at hight light levels, whenever shot noise becomes the main noise source, as highlighted by the SNR expression. Results of the comparison at a shorter integration time is illustrated in Fig.4, where advantages of APS with respect to PPS become apparent.

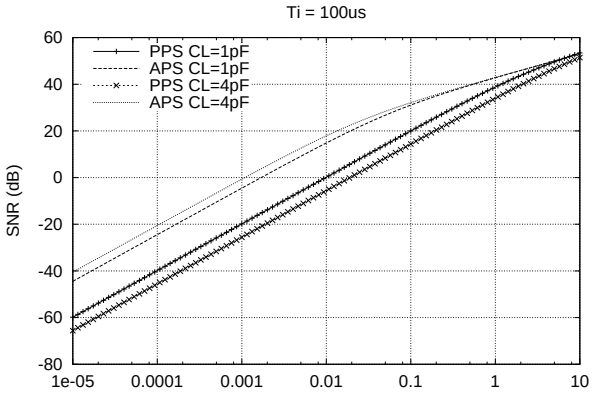

Figure 4. APS versus PPS. Same parameters as in Fig.3 with $T_{int} = 100\mu$sec

3. Blooming considerations

When a single photosite element of an array is illuminated by high optical energy, excess minority carriers may diffuse into adjacent pixels. This phenomenon is called blooming and it is one of the most critical problem of high dense CMOS camera arrays. In this section we will focus on the countermeasures that can be adopted for blooming reduction between the APS and PPS architectures. More specifically, we will show 2D simulations of the APS and PPS structures using a silicon device simulator [8] to quantify blooming currents. We have used technology profiles of a general purpose $0.7\mu m$ CMOS technology. Simulations refer to a photodiode structure embedded in a well since this structure is commonly used to reduce blooming due to infra-red radiations.

One of the most common strategy used to counteract blooming in CMOS technology is the use of a guard ring. Guard rings are diffusions that surround the photodiode, to collect excess minority carriers, that can be implemented in both APS and PPS. A cross section of a photodiode element surrounded by a guard rings is illustrated in Fig.5. The central photodiode structure is guarded on the left side by a P+ diffusion and on the right side by a N+ diffusion used as bias contacts of the well.

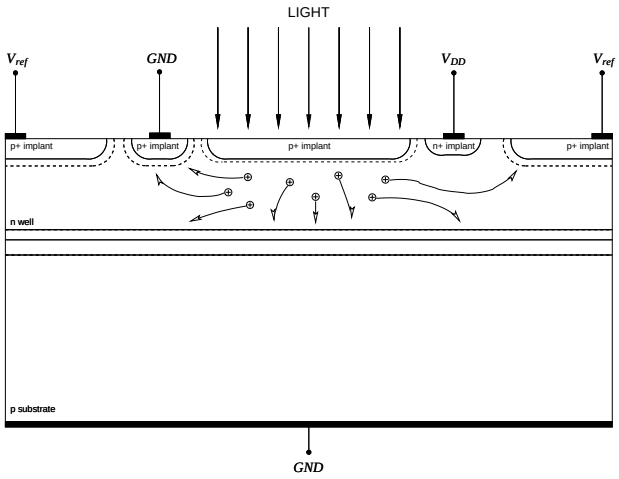

Figure 5. Cross section of a PPS structure with p+ and n+ guard rings. Optical window is $14\mu m$.

In PPS scheme, the photodiode junction is left floating during the integration time, after being reset. Due to the photocurrent, potential across the photojunction decreases during integration time with a rate that depends on the optical power. If integration time and/or optical power are larger than expected, junction reaches an equilibrium state where photocurrent equals forward-bias current. In this condition, minority carriers overflow from the photosite determining blooming on adjacent pixels.

In APS cell architecture the blooming process is similar, however, due to the presence of the reset transistor, we can limit the discharge of the photodiode by properly setting its gate voltage [9]. This is equivalent to set the reset transistor so that it sinks the excess of photocurrent. In the PPS scheme the redundant reset transistor is omitted to achieve higher fill-factors. A cross section of the APS structure where the P+ implant of the photodiode is tied to a fixed voltage is depicted in Fig.6

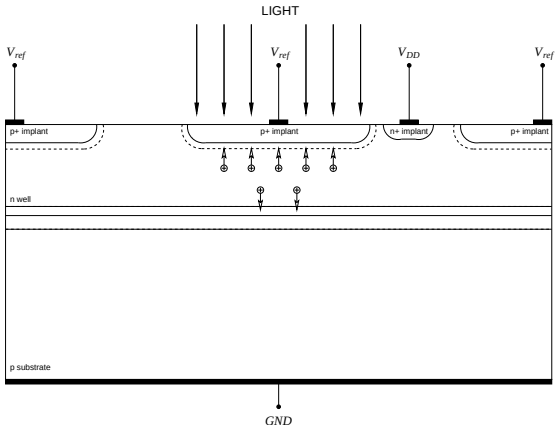

Figure 6. Cross section of an APS structure with photodiode tied to a fixed voltage ($V_{ref} = 0.V$ in simulations).

Results of simulations are illustrated in Fig.7 where currents collected on adjacent photosites per unit length of the structure ($1\mu m$) are plotted versus optical power. As clearly illustrated, N+ guard ring weakly improve the blooming process with respect to the case where no guard rings are present. On the other hand, P+ guard ring on the PPS structure greatly reduces the blooming as much as the APS structure (bottom curves).

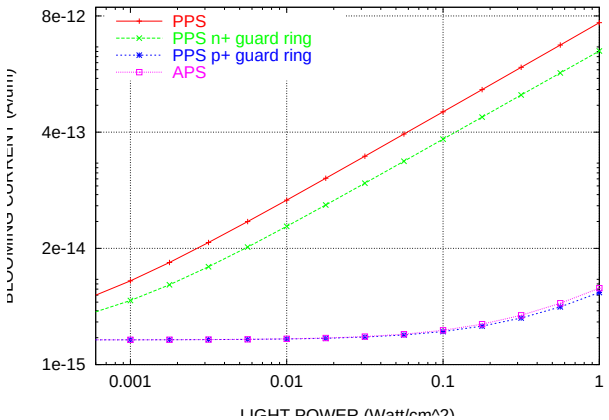

Figure 7. Blooming currents

4. Conclusions

Analysis of random noise in APS and PPS readout schemes has shown the following results:

i) APS shows better performances for low light energy whenever readout noise become relevant with respect to other noise sources;

ii) SNR gap between APS and PPS schemes at low illumination is inversely related to the line capacitance value as anticipated by equation (3);

iii) APS performance over PPS vanishes at high optical energy, and SNR improves with a 10dB/decade slope;

iv) the transition between the above mentioned regions is related to the optical energy, that is, integration time T_i times light intensity P_0.

Device simulations of the two structures have shown how blooming can be reduced by using different approaches with equal results: the reset transistor in the APS scheme and the P+ guard ring in the PPS architecture. However, one should take into account that the latter approach may significantly reduce the fill-factor of the cell thus reducing the signal-to-noise ratio.

In conclusion, PPS scheme still preserves good performances, comparable to the APS scheme for high optical energies. Blooming can be reduced as much as in the APS scheme and shows advantages due to its simplicity. However, APS approach may significantly improve the performance whenever low optical energy, large size arrays and reduced integration time occur.

5. References

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