A New Compact Horizontal Current Bipolar Transistor (HCBT) Fabricated in (110) Wafers

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Abstract

A very compact Horizontal Current Bipolar Transistor (HCBT) is fabricated and tested. It is processed in <110> bulk Si substrate where the <111> crystal plane is perpendicular to the surface and is used as the active transistor sidewall. In this way, the sidewall roughness can be minimised by using crystallographic dependent etchants making the intrinsic transistor doping process highly controllable and repeatable. Hence, unlike in the existing lateral bipolar transistors, the optimum dopant distribution can be achieved what will improve transistor’s high-frequency performance. Additionally, HCBT is processed in simple technology with only 5 lithography masks making this structure attractive for low-cost, low-power high-performance bipolar/BiCMOS applications. The improvement of $f_T$ and $f_{max}$ up to 24 and 50 GHz, respectively, can be achieved by using HCBT technology.

1. Introduction

Recently, lateral bipolar transistors (LBTs) processed in SOI substrates become attractive in low-power, low-cost, high-performance Si bipolar/BiCMOS applications [1-4]. In comparison with vertical current bipolar devices, LBTs can be processed by a simpler technology with the total area of $pn$ junctions almost equal to the area of the intrinsic transistor region. The result of the reduced volume of parasitic regions is the reduction of capacitances, which results in rather high values of maximum oscillation frequency. On the other hand, SOI LBT’s main disadvantage is low cut-off frequency (i.e. 3-16 GHz) limited by unoptimised doping profiles of the intrinsic transistor region, i.e. the base transit time. The intrinsic transistor region is usually doped by the base and emitter ion implantations separated by the spacer. Hence, the intrinsic doping profile is determined by the difficult-to-control lateral distribution of dopants and spacer geometry.

We developed a Horizontal Current Bipolar Transistor (HCBT) whose improvements to bipolar devices scaling is given in [5]. In this work, a novel approach of using the <111> vertical sidewalls is demonstrated. In that way, the intrinsic base is implanted at the sidewall as reference surface, just as in the vertical current transistors [6]. Furthermore, the polysilicon layer can be used for the emitter and the optimum doping profile of the intrinsic transistor can be obtained. Since both base and emitter are doped with the sidewall as reference plane, this approach offers the controllability and repeatability of dopant distribution. Additionally, the sidewall roughness originating from the photoresist edge roughness of can be minimised by using crystallographic dependent etchants, where <111> sidewall acts as a stopping layer. On balance, the HCBT concept combines the optimised intrinsic doping profile of vertical current transistors and reduced parasitics and simple technology of LBTs.

2. Fabrication Sequence

The HCBT is processed in 1 µm lithography resolution. In order to utilise the <111> crystal planes as the active transistor region sidewalls, the <110> $p$-type wafer is used as device substrate. In contrast to the LBTs, which are processed exclusively in SOI substrate, the HCBT structure is fabricated in bulk Si although the new concept is compatible with SOI substrate as well. The HCBT fabrication sequence is depicted in Fig. 1.

The process starts with the collector $n$-hill ion implantation. Phosphorus ions are implanted at the energy of 300 keV with the dose of $8 \times 10^{12}$ cm$^{-2}$ at wafer tilt angle of 0 degrees to increase channelling. A high thermal budget annealing is performed so that the $pn$ junction depth of around 1 µm is obtained with the doping concentration around $6 \times 10^{16}$ cm$^{-2}$ at depths where the active transistor region is (0.3 to 0.6 µm). After buffer oxidation, a 50 nm of silicon nitride protection layer is deposited.

The first mask is used to define the collector $n$-hill region. Since the active sidewall must coincide with <111> crystal plane, the mask should be aligned accordingly. Note that in the case of rectangular shape of the $n$-hill the passive (front and back) sidewalls correspond to <112> plane, which does not act as KOH etch stopping layer. The $n$-hill is etched by using time-multiplexed ICP RIE process due to its high selectivity.
and the resulting vertical sidewall angle close to the ideal 90 degrees. After RIE, a short dip in KOH etchant is done to decrease sidewall roughness and remove defects caused by RIE. A two-step etch enables one to obtain atomically flat <111> sidewalls as well as to minimise the undercut on the passive sidewall that does not act as the etch stopping crystal plane. The final height of the n-hill is around 1.8 \( \mu \)m. The structure is shown in Fig. 1.a.

Next, a thin protection oxidation is carried out and a channel stopper ion implantation is performed. The n-hills are isolated by the deposition of LTO SiO\(_2\), which is then densified, chemically-mechanically planarised (Fig. 1.b) and etched-back. The amount of the n-hill above the isolation oxide surface \( h_2 \) in Fig. 1.c) determines the active transistor height so the etch-back process must be timed.

After screening oxidation, the 2\(^{nd}\) mask is used for the base doping. It protects the collector side of the n-hill from boron penetration. First, the intrinsic base is formed by boron implantation into the sidewalls (Fig. 1.c) at wafer tilt angle of 45° energy of 20 keV and the dose of \(10^{14}\) cm\(^{-2}\). The wafer rotation angle must be adjusted so that the front and back sidewalls of the n-hill are protected from ion penetration. The extrinsic base is implanted at 50 keV and \(4\times10^{15}\) cm\(^{-2}\) at opposite tilt angle to protect the intrinsic base from the additional doping, as shown in Fig. 1.d.

A single polysilicon layer is used for the emitter and collector \(n^+\) regions. The first 0.4 \(\mu\)m of deposited film is in-situ phosphorus doped, whereas the upper part can be undoped (as depicted in Fig. 1.e) since it is removed by CMP and etch-back anyway. However, leaving the upper part undoped reduces deposition time. The crystallographic dependent etchant is used for poly etch-back. In that way, the active device sidewalls are protected by its <111> surface and the intrinsic base is left intact after poly etch. The part of the \(n^+\) poly at the passive sidewalls of the n-hill is removed by using the 3\(^{rd}\) lithography mask. The \(n^+\) collector and emitter regions are left only at the active sidewalls of the n-hill.

The passivation LTO SiO\(_2\) is deposited and implanted dopants are activated and emitter drive-in diffusion is carried out at single RTA step at 960 °C for 40 seconds. The 4\(^{th}\) and 5\(^{th}\) masks are used for contact holes.

\(\text{Figure 1. HCBT process sequence. The structure after: (a) n-hill ion implantation, annealing, nitride deposition, two-step n-hill etching by the 1\(^{st}\) mask; (b) channel stopper ion implantation, LTO deposition and CMP; (c) LTO etch-back, intrinsic base and; (d) extrinsic base ion implantation by the 2\(^{nd}\) mask: the resulting } w_{\text{ext}} = 3 \mu m; (e) in-situ doped and undoped poly silicon deposition, CMP; and (f) etch-back, poly etching by the 3\(^{rd}\) mask, passivation oxide deposition, contacts.\)
definition and deposited metal lift off. Finally, the hydrogen passivation is carried out to improve the n-hill sidewall – isolation oxide interface properties. It is performed in hydrogen plasma at 220 °C for 2 hours followed by drive-in at 400 °C for 5 minutes in N₂ atmosphere.

3. HCBT Structure Examination

The final HCBT structure is depicted in Fig. 1.f, and the SEM angle view of HCBT with emitter length of 15 µm is shown in Fig. 2.a. The magnified active transistor sidewall in Fig. 2.b shows the flat <111> sidewall surface meaning that the n-hill is not attacked by crystallographic dependent etchant during polysilicon etch-back process. Also, the poly layer is horizontal and in close contact with the n-hill sidewall, confirming the suitability of CMP and etch-back techniques for processing isolation oxide and n⁺ emitter and collector regions.

The HCBT structure is processed with only 5 lithography masks, which is the fewest number of masks required for bipolar transistor processing known to the authors, including vertical and lateral devices. Moreover, the HCBT fabrication is performed without: collector buried layer, epitaxy, trench isolation and with a single layer of polysilicon. Additionally, the use of CMP and etch-back technique for the isolation of the n-hills makes it possible to process HCBTs in bulk Si, although the concept is fully compatible with SOI substrates. The simple fabrication and the use of bulk Si wafers, makes HCBT concept a low-cost technology and easily integrable in BiCMOS applications.

The collector vertical doping profile determined by the phosphorus ion implantation and subsequent annealing is designed not only to have a higher doping concentration at depths of the intrinsic device region, but also to have a lower doping (<10¹⁶ cm⁻³) near the bottom of the n-hill to decrease the peripheral component of collector-base capacitance.

4. HCBT electrical characteristics

Fig. 3. depicts the output characteristics of the processed HCBT. The measured breakdown voltage is BVCBO=8.4 V, at Ib=10 µA, and the Early voltage calculated from output characteristics is Vₐ>120 V. Maximum DC current gain is around 40. High breakdown and Early voltages indicate a high base Gummel number (due to the high dose and energy of the intrinsic base ion implantation) and rather low collector doping (NDCmax<6.2x10¹⁶ cm⁻³). The measured Gummel plots are shown in Fig. 4. A nonideal base current at lower voltages is due to the SHR recombination at n-hill - SiO₂ interface. For the reason to decrease the interface recombination, a hydrogen passivation is performed, which results in a minimum base current ideality factor 1.2 at base-emitter voltage around 0.9 V.

The high frequency performance of the processed structure is examined by s-parameters measurement. The current dependency of ft and fmax is depicted in Fig. 6. The peak ft is 3 GHz and peak fmax is 10 GHz. Both frequencies are limited by the coarse lithography resolution used for fabrication. The extrinsic base width (w₁ in Fig. 1.d) has to accommodate the base contact as well as the worst case misalignment of 2nd mask (base formation) and the 4th mask (contact holes). The result is the extrinsic base width of w₁=3 µm, which is much larger than the intrinsic base height (hte=0.45 µm).

Such large collector-base junction area implies a large CBE that directly affects fmax, as well as fr through terms RCECBE and CBEgαm. The later is especially pronounced at lower collector currents since gαm=qIC/mVT. In addition, depending on collector-base voltage, the collector-base depletion region under the extrinsic base decreases the effective collector cross-section area thus causing the Kirk effect to occur at lower collector currents. Moreover, the electrons injected from emitter flows partly through the extrinsic base - collector depletion region increasing the effective transit time, dBC/gαm.
5. Simulation Analysis

In order to examine the extrinsic base effect on high frequency performance quantitatively a numerical simulation is performed. A two-dimensional device simulation program MEDICI [7] is used. The HCBT structure with the same geometry as the processed one is examined.

The extrinsic base width is varied from 3 μm to 0.2 μm. The n-hill width is kept constant in order to isolate only the extrinsic base effect. Actually, by lithography improvement, the n-hill width will also decrease, causing the further improvement of $f_T$ and $f_{\text{max}}$. The simulation results are depicted in Fig. 6, showing the improvement of $f_T$ and $f_{\text{max}}$ up to 20 and 39 GHz, respectively. For minimum extrinsic base width, both frequencies are limited by the base and collector doping profiles. If the base width is reduced to 50 nm with the same collector doping profile the $f_T$ of 24 GHz and $f_{\text{max}}$ of 50 GHz could be achieved. Furthermore, if a uniform collector doping of 10^{17} cm^{-3} is used, the $f_T$ of 32 GHz can be achieved, while $f_{\text{max}}$ is decreased to 42 GHz.

6. Conclusion

The fabrication of compact HCBT structure is successfully demonstrated in <110> bulk silicon substrates. The active device is formed at <111> sidewalls, which enables the use of crystallographic dependent etchants for the purpose of the minimisation of sidewall roughness and fabrication of optimum doping profiles of the intrinsic transistor region.

The high frequency performance is limited by a large collector-base capacitance due to the coarse lithography resolution employed. The simulation of the structures with the decreased extrinsic base widths shows the improvement of HCBT $f_T$ and $f_{\text{max}}$. Therefore, $f_T$ and $f_{\text{max}}$ are going to be increased with finer lithography resolution used for the fabrication.

7. References


