Hot carrier reliability improvement of PMOS I/O's transistor in advanced CMOS technology

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Abstract

Boron diffusion has previously involved Hot Carrier Injection (HCI) reliability problems for pMOS transistors. Introduction of phosphorus into channel of pMOS I/O’s transistors in 0.12µm technology enables to significantly improve HCI reliability while short channel effect is better controlled and performances are slightly improved.

1. Introduction

Scaling transistors dimensions has led to decrease operating gate and drain voltages. High voltage and analogue applications need two transistors families onto the same silicon wafer using double gate oxide process in 0.12µm technology: T1 (Lg=0.12µm @ +/− 1.2V) and T2 (Lg=0.35µm @ +/− 3.3V). Lg means gate length. Hot Carrier Injection (HCI) phenomenon becomes a stronger subject of interest since T2 high voltage transistors are fabricated with more and more complex processes.

It was observed that transient enhanced diffusion attenuates HCI effects on transistor lifetime [1]. Nevertheless, pMOS T2 transistor may be still affected by HCI degradations because of source & drain boron diffusion. It appeared that its architecture had to be optimised to balance HCI lifetimes between nMOS and pMOS I/O’s transistors.

2. Device fabrication

First, shallow trenches are etched to isolate the different active areas. Secondly, wells and channels are implanted before the two gate oxides are grown separately using 193nm photolithography. 65Å ISSG oxidization is previously used for T2 devices while oxy-nitridation is performed the latter for T1 transistors. Pre-doped polysilicon gate layers are deposited before the LDD implants and then transient enhanced diffusion anneal is performed. After Lshape spacer’s formation, source and drain areas are implanted followed by a cobalt silicidation, interdielectric layers deposition, contact etchings and copper metallization layers deposition.

Table 1. Different tested architecture of pMOS I/Os

<table>
<thead>
<tr>
<th>Implant level</th>
<th>Species</th>
<th>Dose</th>
<th>Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel</td>
<td>Arsenic (As)</td>
<td>From 6x10¹² to 2x10¹³/cm²</td>
<td>From 160 to 200keV</td>
</tr>
<tr>
<td></td>
<td>Phosphorus  (P)</td>
<td>From 3x10¹² to 8x10¹³/cm²</td>
<td>From 100 to 160keV</td>
</tr>
</tbody>
</table>

Between spacer formation and source/drain implant, an offset spacer was added shifting oxide layer deposition (usually used to protect some areas from unwished silicidation) as shown in figure 1 (Transmission Electronic Microscopy photography). This leads to artificially obtain an 800Å equivalent spacer for the I/O’s pMOS architecture.

Figure 1. TEM photography pMOS I/O’s transistor

3. Results and discussion

Because of aggressive specifications and complexity of 2-devices-technology, I/O’s architecture needs to be adjusted to answer to performances requests and to
maintain an acceptable reliability. Optimisation between device performances and reliability was focused on PMOS I/O's transistors because of boron diffusion impacts. Several arsenic doses and energies were tested for channel implant level. Figure 2 allows to extract following abacus for 65Å pMOS T2 (long transistors): +25mV per each $1 \times 10^{12}$/cm$^2$ arsenic dose and -25mV per each 10keV arsenic energy.

Figure 2. PMOS I/O's VT values versus gate length

As Expected, the more doped channel, the higher threshold voltage. When phosphorus is alone implanted (at 100keV) into pMOS channel, a strong roll-up (about 70mV) appears between long transistor and nominal lengths. Mixed channel (containing phosphorus + arsenic at deeper energy) is characterized by a light roll up on VT(L) plot while only roll-down effect occurs for pure arsenic channel as presented in figure 2; threshold voltage values (Vt) almost reach the same value for nominal length (Lg=0.35µm). Performances plots (figure 3) show that adding phosphorus into channel leads to improve performances by a 5%-10% for nominal length.

Figure 4 displays Vt(Lg) curves for different mixed channels (arsenic + phosphorus). Curve A is the reference mixed implant. Reducing arsenic dose and lowering phosphorus energy (curve B) enables to obtain a lower Vt value for long transistor while roll up is accentuated (8mV → 30mV). In the same way, comparison between curves C and D reveals a roll up increase when phosphorus implant dose is increased.

Figures 5 are extracted from TCAD simulations that were performed with the process simulator DIOS 6.1 from ISE. On figure 5a are shown the simulated profiles of the NWell for a long transistor. For a 160keV implant energy, the projected range of the phosphorus implant is much deeper than Arsenic. As it can be observed on figure 2, the threshold voltage of the long device with mixed channel (P+As) is slightly lower than mono-channel (As) even if the dose is higher (the contribution of phosphorus is too low for the long device). At energy of 100keV, the projected range of the profile of phosphorus is deeper than the profile of arsenic. The threshold voltage is therefore slightly lower for the long device as can be seen on figure 2. On an other hand, a roll up is present on the Vt(L) around 0.35µm. This effect can be explained by an enhanced diffusion of phosphorus assisted by the point defect generated by the LDD and S/D implants [2]. On figure 5b is presented a 2D cut of the PMOS 0.35µm with only Arsenic (8e12 cm$^{-2}$ at 160keV): the implant is localized and the profile is quite retrograde. On figure 5c, an implant of phosphorus (8e12 cm$^{-2}$ at 160keV) is simulated and the diffusion was enhanced by simulation in order to reproduce the roll up: the profile of phosphorus is more diffused and a significant part of doping is present beneath the gate of the MOS.
Another goal to achieve by this new architecture was to reduce Hot Carrier degradations. Figures 6a and 6b show respectively experimental change of saturation current (measured at $V_g = V_d = -3.3V$) and transconductance after stress performed at $V_d = -4V$, under $V_g$ condition corresponding to the maximum substrate current $V_{i}$ (Ibmax). These results were obtained on three different devices: a high channel implant device (As 2e13/ cm²), a light one (As 6e12/cm²) and a mixed one with phosphorus and arsenic (As 4e12/cm² + P 4e12/cm²), other implants remain unchanged. This aging mode called Drain Avalanche Hot Carrier (DAHC) [3] is above all function of the lateral field distribution, and so directly linked to the N-well/P-SD junction doping profile. It can be clearly seen that an improvement of at least one decade in DC drift-time was obtained between high dose device and mixed one, and a factor 2 -3 between latest device and light dose one. Therefore a smoother junction should be obtained for mixed channel dose device, and obviously the more abrupt one must be found for high channel dose device. Ionization ratio enables to differently quantify this new HCI endurance. Using Chung et al model [4,5], the maximum substrate current can be expressed as:

$$I_{sat} = I_{drain} \times \frac{\alpha_i}{\beta_i} \times (V_D - V_{DSAT}) \times \exp \left( - \frac{\beta_i \cdot \ell}{V_D - V_{DSAT}} \right)$$  \hspace{1cm} (1)

where $V_{DSAT}$ is the drain saturation voltage, $\ell$ the length of the velocity saturation, $\alpha_i$ and $\beta_i$ the ionization coefficients.

For oxide thickness $T_{ox} < 150Å$ and effective channel length $L_{eff} < 0.5 \mu m$ the expression of $\ell$ commonly used is [6]:

$$\ell = 0.017 \frac{T_{ox}^{1/4}}{L_{eff}^{1/4}} \times X_j^{1/3} \ (cm)$$  \hspace{1cm} (2)

with $X_j$ the N-well/P-SD junction depth.

Using expression (1), the plot of substrate/drain saturation currents ratio normalized by $(V_D-V_{DSAT})$ versus $1/(V_D-V_{DSAT})$ is presented on figure 7 for the three pMOS already mentioned. For a same $(V_D-V_{DSAT})$ value, Isub/Idrain ratio is at least four times lower for low and mixed dose devices compared to high dose one while saturation current value increases from 200µA/µm (high dose device) to 300 µA/µm (low and mixed dose devices). A slight lower injection ratio is also observed for mixed channel dose device compared to light one, in good agreement with HCI experiments.

From $V_{DSAT}$ value and effective channel length $L_{eff}$, a saturation field $E_{sat}$ value of 9-10×10⁵ V/cm was calculated for the three different device, value commonly found in literature [6,7]. Ionization threshold energy is found being the same for the three devices since slope remains constant. Using expression (2) and TCAD simulation for the N-well/P-SD junction depth evaluation, an identical ionization parameter $\beta_i$ of 3.2×10⁶ V/cm was extracted, in good agreement with earlier work [7]. Thanks to this new architecture and in spite of a 50% increase of drain current, the hot carrier injection was reduced by a factor 4. This result coupled with HCI experiments tends to prove that a higher lateral field and/or a broader high field
distribution near N-channel/P-SD junction are generated for high dose device compared to the two other ones.

Although, using quasi-two-dimensional analysis [8] and the derived expression (3) of the maximum lateral electric field \( E_{\text{max}} \), the same averaged \( E_{\text{max}} \) around \( 3 \times 10^5 \) V/cm was obtained for the three devices at \( V_D = -3.3 \) V and \( V_{g} (I_{b\text{max}}) \).

\[
E_{\text{max}} = \sqrt{\left( \frac{V_D - V_{DSAT}}{I} \right)^2 + E_{\text{sat}}^2}
\]

TCAD simulations of the lateral field distribution are presented in figure 8a and figure 8b. The origin in x direction corresponds to the middle of the channel; origin in y direction corresponds to the Si/SiO\(_2\) interface. Lateral electrical field intensity is represented by a greyscale and white colour is used for field inferior to \( E_{\text{sat}} \).

For mixed channel dose device, a wider region with a lower lateral field is obtained; this distribution shape is undoubtedly at the origin of the lower injection ratio and the higher hot carrier endurance experimentally found.

4. Conclusion

We have investigated the role of phosphorus species into N well channel of pMOS I/O's transistors (3.3V) for 0.12\( \mu \)m technology. Phosphorus introduction involves a strong roll-up when it is alone implanted, which becomes lighter for mixed channel (arsenic + phosphorus). First TCAD results tend to show an enhanced diffusion of phosphorus assisted by the PLDD-Nwell junction defects. Deeply implanted phosphorus enables to reduce arsenic concentration at the channel surface and so to obtain a slightly higher saturation current while phosphorus concentration at the junctions involves a best short channel effect control.

Reliability measurements show that lowering channel implant dose enables to improve hot carrier injection reliability. Phosphorus introduction allows to decrease arsenic dose by a factor 1.5, which improves also HCI reliability by a factor 3. The main cause is identified as coming from a smoother junction doping profile, a wider and lower electrical field distribution. It will be interesting to check if similar effects can be observed for negative bias temperature instability.

5. References