A Self-Aligned Double Poly-Si Process Utilizing Non-Selective Epitaxy of SiGe:C for Intrinsic Base and Poly-SiGe for Extrinsic Base

J. Pejnefors
Royal Institute of Technology (KTH)
Dept. of Microelectronics and Information Technology,
SE-164 40 Kista, Sweden
johanp@imit.kth.se

T. Johansson, J. Wittborn, A. Santos, H. Norström and U. Smith
Ericsson Microelectronics AB,
SE-164 81 Kista, Sweden

A. Cheshire
Applied Materials UK Ltd.,
Edinburgh, UK

T. Buschbaum, C. Rosenblad and J. Ramm
Unaxis Balzers Ltd.,
Principality of Liechtenstein

Abstract

A self-aligned double poly-Si process using non-selective epitaxy of SiGe:C for the intrinsic base and a dual stack of poly-Si and poly-SiGe for the extrinsic base is presented. Self-alignment of the extrinsic base is obtained by detailed control of the emitter window etch procedure. The etch of the extrinsic base is endpointed at the poly-Si/poly-SiGe interface, and is followed by a timed etch of the SiGe film. Due to the selectivity towards Si, the etch can be stopped at the epitaxial Si surface.

The SiGe:C epitaxy is obtained using ultra-high vacuum chemical vapor deposition (UHV/CVD). As a result of the slightly higher growth rate of the epitaxial film compared to the polycrystalline material, an almost planar surface could be obtained.

Working devices have been verified by electrical measurements.

1. Introduction

The performance of silicon-based high-speed bipolar transistors has improved greatly during the last few years. Recently, a transistor with a record cut-off frequency of 210 GHz was presented [1]. The basis of this rapid improvement is the use of an epitaxially grown SiGe base that makes it possible to engineer the band gap and to produce a very narrow base. The introduction of carbon in the epitaxial process minimizes boron out-diffusion and hence an even narrower base can be achieved [2].

A common way of introducing epitaxy in the device process is by non-selective epitaxy followed by a deposition of a dielectric layer, which requires patterning [1,3]. Thus the process becomes non-self-aligned. However, using a rather complicated process flow, including conversion of poly-Si to oxide, self-aligned transistors with a non-selective epitaxially grown base have been obtained [4]. A more straightforward way of achieving a self-aligned process is to introduce the epitaxy in the form of selective growth in the emitter window [5]. Since selective epitaxy is known to suffer from severe loading effects, the epitaxial parameters will need tuning for each layout with different device density. It is also not suitable for multi-project wafers where different circuit layouts are placed in close. Moreover, the selective process is very difficult to control, resulting e.g. in voids and poor base contacts.

A common problem in all self-aligned double-poly processes is the removal of the (poly-) silicon used for the extrinsic base in the emitter opening without etching down into the monocrystalline silicon. This problem becomes more severe for an epitaxial base process where the base layer is formed prior to the emitter window etch than for a process with the base formed by ion implantation. Many solutions are known in the literature. For non-selective epitaxial SiGe processing, the problem has recently been addressed in [6], where a boron silicate glass (BSG) landing pad is used as an etch stop and a diffusion source for a base link-up.

In this paper, we report on the use of poly-SiGe as the extrinsic base layer used in order to produce a self-aligned process utilizing non-selective epitaxy of SiGe:C. The modular concept used for the extrinsic base can also be applied to a conventional double-poly bipolar process flow that uses an implanted base.

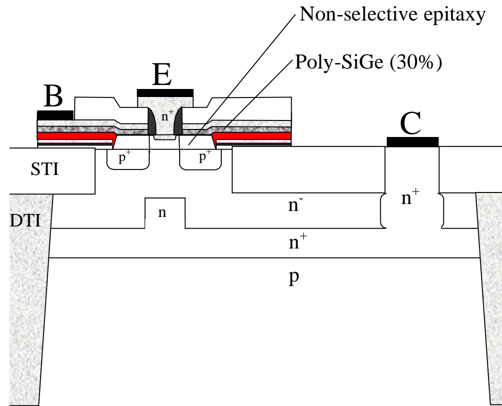

Figure 1. Schematic cross-section of the device.

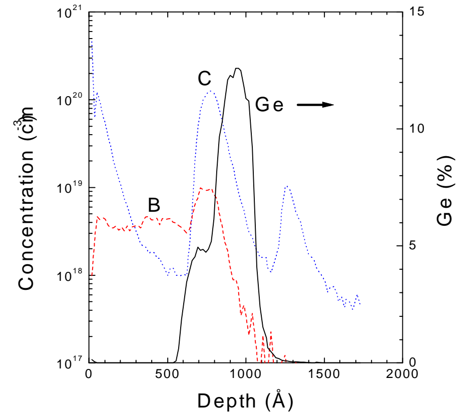

Figure 2. SIMS profile of the active area after non-selective epitaxy.

2. Fabrication of the device

The fabrication of the device begins with arsenic implantation into the wafer to form the buried collector layer, followed by the growth of an intrinsic epitaxial Si layer. Then, shallow and deep trench isolations are formed as described in Ref. [7]. After oxidation, the collector plug is made using a phosphorus implant. A nitride layer and a Si seed layer are deposited and patterned prior to non-selective SiGe:C epitaxy in an UHV/CVD reactor. Next, a bi-layer consisting of poly-SiGe and poly-Si for the extrinsic base layer is deposited. Prior to oxide deposition, the extrinsic base region is implanted with a high boron dose. The implanted boron will later be out-diffused in order to form the extrinsic base connection. The stack is then patterned and etched to form the emitter window. After selective collector implantation (SCI), a thin TEOS film is deposited and densified. Inside spacers are formed before the emitter polysilicon is deposited and implanted with arsenic. Next, outside spacers are formed and the emitter drive-in is carried out. Salicidation and metallization complete the transistor process. Figure 1 shows a schematic cross-section of the resulting transistor.

3. Intrinsic base module

The intrinsic base was grown in an Unaxis SIRIUS® UHV/CVD system. The depositions were performed at a working pressure of approximately 1 mTorr and a temperature of about 550 °C. From SIMS measurements, the oxygen concentration in the epitaxial films was found to be lower than 1×10^{18} cm^{-3}. The epitaxy consists of five different layers, which are grown in an un-interrupted sequence. The epitaxy starts from the substrate with an undoped Si buffer layer, followed by an intrinsic SiGe layer with a Ge concentration of approximately 12 %. Then follows a SiGe layer with 5 % Ge, which is boron doped to 1×10^{19} cm^{-3}. Carbon in the order of 0.2 %, is added to the highly boron doped layer in order to minimize boron out-diffusion during subsequent device processing so as to keep the intrinsic base narrow. Next, a SiGe layer (with 5 % Ge) with a boron concentration of 4×10^{18} cm^{-3} is grown. Finally, a Si cap layer is boron doped to 4×10^{18} cm^{-3}. The resulting concentration profiles after epitaxial growth, as obtained by SIMS, are shown in Fig. 2. The carbon peak at the interface between the epitaxial film and the Si substrate is due to the surface treatment before epitaxy.

A cross-sectional TEM of the non-selective epitaxy is shown in Fig. 3. It can be seen that the higher epitaxial growth rate in the active area compared to the growth rate of the polycrystalline film on the field area results in an almost planar surface after the non-selective epitaxial process. As a result of the higher epitaxial growth rate, the commonly observed shrinkage of the active area due to polycrystalline over-growth during non-selective epitaxy in RPCVD reactors is almost absent when the film is grown under UHV/CVD conditions, see Fig. 3. From an AFM analysis, the RMS surface roughness of the epitaxy and the co-deposited polycrystalline material were found to be 3 and 60 Å, respectively.

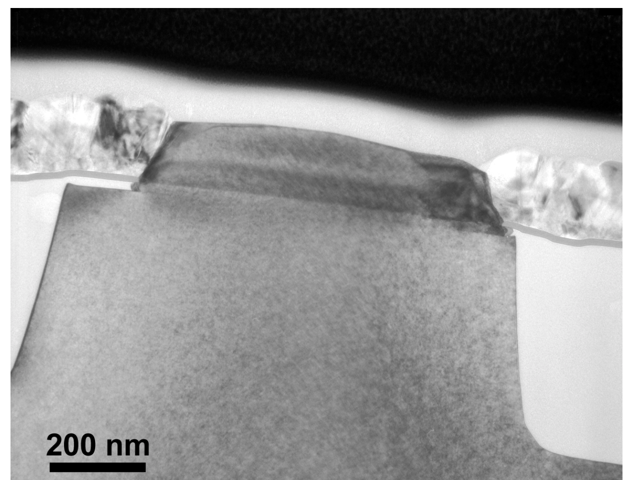

Figure 3. XTEM of the non-selective epitaxy.

4. Extrinsic base module

After the intrinsic base is grown, poly-SiGe with about 30 % Ge is deposited at low-temperature in the UHV/CVD system. The deposition starts with a thin Si seed layer in order to facilitate the nucleation of the poly-SiGe film. Then a 500 Å thick poly-SiGe film with 30 % Ge is deposited and capped with a thin Si layer. AFM analysis of the poly-SiGe film shows that the surface roughness is similar (~60 Å) in the active area and the field area. The extrinsic base is completed by the deposition of a 600 Å thick poly-Si film using an ordinary LPCVD furnace. The poly-Si layer is subsequently implanted with 2×10^{15} cm^{-2} of BF_2 at 35 keV. Finally, the extrinsic base stack is covered by a deposited oxide layer.

The emitter window is opened by dry etching in an Applied Materials (AMAT) Centura™ system. The isolation oxide is etched in an AMAT eMxP+™ chamber. This is then followed by an etch of the poly-Si and poly-SiGe layers utilizing an AMAT poly-DPS™ chamber using an HBr/Cl_2 based chemistry. Using the system monochromator the 3040 Å emission line is used to indicate the interface between poly-Si and poly-SiGe.

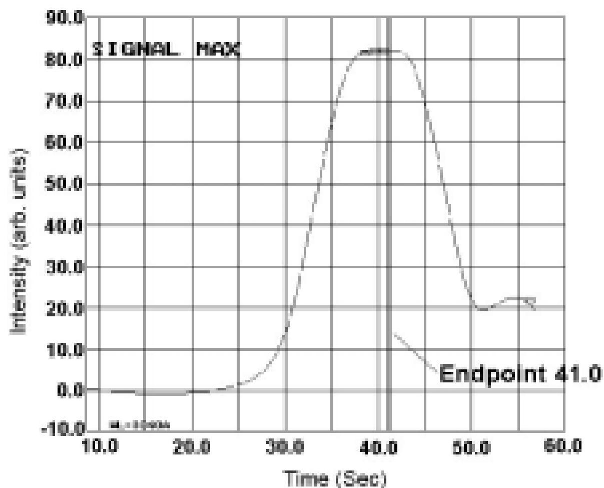

Figure. 4. Intensity of the 3040 Å endpoint trace *vs.* etching time.

The signal reaches maximum intensity at which point the endpoint is triggered as shown in Fig. 4. A timed step is then used to etch through the poly-SiGe and stop on the underlying Si epitaxy.

Figure 5 shows a cross-sectional SEM micrograph of the emitter window at the stage when the 3040 Å emission line has reached its maximum intensity. The poly-SiGe film shows up as the brightest layer. The required time for etching the poly-SiGe layer was obtained from previous determinations of the etch rate of poly-SiGe. A selectivity of approximately 2:1 between SiGe and Si films allowed a controlled etch-stop on the monocrystalline surface deemed critical to the device performance.

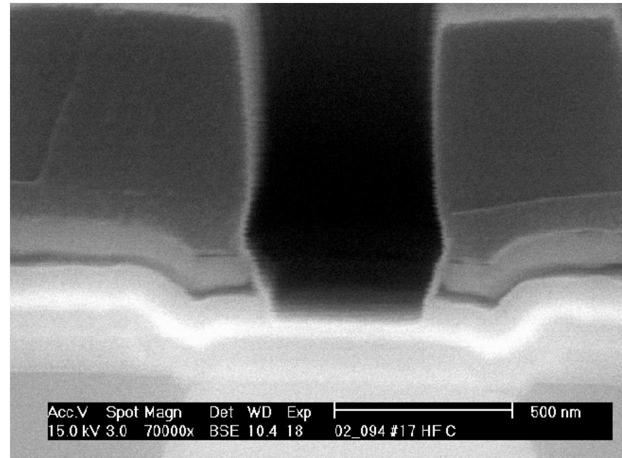

Figure. 5. XSEM of the emitter window at the end-point maximum.

The resulting emitter opening after the timed poly-SiGe etch is shown in Fig. 6. The uniformity across the wafer of the extrinsic base etch was found to be excellent and no loading effects could be detected.

Figure 7 shows a cross-section of the transistor after completed processing. Tungsten plugs and SiGe films are seen as bright layers. It has been reported [8] that the oxidation rate of SiGe is enhanced by a factor of three compared to Si and that Ge congregates at the interface of the growing oxide. However, the poly-Si layer that covered our poly-SiGe film protected the latter from oxidation during the densification of the TEOS film.

The poly-Si covering the poly-SiGe layer also facilitated the Ti salicide process in that the poly-Si was thick enough to prevent the formation of a thermally unstable germano-silicide. No difference in sheet resistance was observed between a standard Ti silicidation of Si and the silicided poly-Si/poly-SiGe film stack.

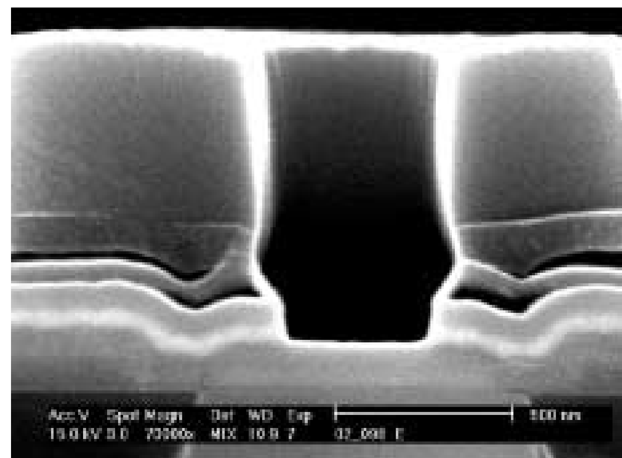

Figure. 6. XSEM of the emitter window after a timed etch of the poly-SiGe film.

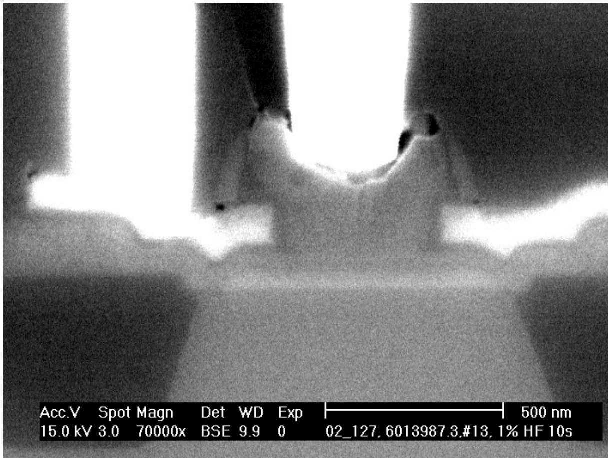

Figure 7. XSEM of the transistor after HF treatment and recorded in the backscattered mode.

5. Electrical measurements

The functionality of this modular base concept is demonstrated in Fig. 8, which shows a Gummel plot for a single transistor and an array of 3040 transistors with emitter area of 0.6×3.0 µm^2 at a base-collector voltage of 100 mV. The collector currents show ideal characteristics as a function of base-emitter voltage indicating a dislocation free epitaxy. The relatively low collector saturation current, which was extracted from a single transistor, is due to out-diffusion of boron from the SiGe layer into the Si substrate. This was confirmed by SIMS measurements performed on a transistor after processing. Since the high-frequency performance of the transistor will be negatively influenced by boron out-diffusion, further optimization of the base-collector formation must be performed. For a single device, the base current is ideal over several decades of current and a peak value of about 140 is extracted for the current gain.

For comparison, the extrinsic base resistance was measured on a reference double poly-Si transistor and a transistor that had the extrinsic base module presented above. The extrinsic base resistance was extracted using

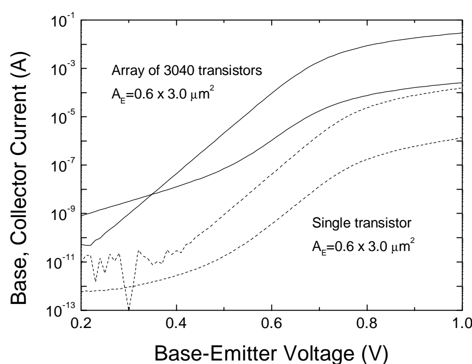

Figure 8. Gummel plot for an array of 3040 transistors with an emitter area of 3.0 x 0.6 µm^2.

the input impedance circle methodology. Values of 9.4 Ω and 4.8 Ω were extracted for the reference and the poly-SiGe extrinsic base transistors, respectively.

6. Summary

A SiGe:C bipolar process based on a double poly-Si concept has been described. The intrinsic base was formed using non-selective epitaxy of SiGe:C in a UHV/CVD system. The extrinsic base was fabricated using a dual film stack consisting of poly-Si and poly-SiGe (30 %). The extrinsic base was etched with an HBr/Cl_2 based chemistry. By tracing the endpoint signal it was possible to stop on the underlying epitaxial layer, thus permitting a self-aligned process.

The modular concept was verified by electrical measurements on arrays of transistors and the extrinsic base resistance was extracted. Further optimization of subsequent process steps to improve the high-frequency performance is in progress.

7. Acknowledgements

The authors would like to thank Professor Mikael Östling at the KTH Department of Microelectronics and Information Technology and Frank Renebo at Ericsson Microelectronics AB for valuable discussions. This work is financially supported by VINNOVA and is part of the MEDEA+ T204 Program ASGBT.

8. References

[1] S.J. Jeng *et al.,* "A 210-GHz f_T SiGe HBT with a non-self-aligned structure", *IEEE Electron. Device Lett.*, vol. 22, Nov. 2001, pp. 542-544.

[2] H. Rücker *et al.*, "Dopant diffusion in C-doped Si and SiGe: Physical model and experimental verification", *IEDM Tech. Dig*., 1999, pp. 345-348.

[3] H. Baudry *et al.*, "High performance 0.25µm SiGe and SiGe:C using non selective epitaxy", *in Proc. BCTM*, 2001, pp. 52-55.

[4] C.A. King *et al.,* "Very low cost graded SiGe base bipolar transistors for a high performance modular BiCMOS process", *IEDM Tech. Dig*., 1999, pp. 565-568.

[5] D.L. Harame *et al.*, "Si/SiGe epitaxial base transistors-part II: process integration and analog applications", *IEEE Trans. Electron. Devices,* vol. 42, 1995, pp. 469-482.

[6] F.S. Johnson *et al.*, "A highly manufacturable 0.25µm RF technology utilizing a unique SiGe integration", *in Proc. BCTM*, 2001, pp. 56-59.

[7] M. Forsberg *et al.*, "A shallow and deep trench isolation for use in RF-bipolar IC's", *in Proc. 30th ESSDERC*, 2000, pp. 212-215.

[8] F.K. LeGoues *et al.*, "The mechanism of oxidation of SiGe", *in Proc. Mat. Res Soc.*, vol. 105, 1988, pp. 313-318.