A Complete Evaluation of Trench Oxide Thickness Effect on Advanced ULSI

E. Perrin, G. Imbert, M-T. Basso, O. Callen
ST Microelectronics, Crolles, France
emanuel.perrin@st.com

R. Braspenning, V. De Jonghe
Philips Semiconductors, Crolles, France
richard.brasperning@philips.com

Abstract

This paper proposes a review of the various consequences of the Shallow Trench Isolation (STI) oxide thickness variations on different process steps and electrical parameter for advanced ULSI. CMP was used to obtain a large window of STI thickness. In addition to usual electrical parameters like reverse narrow channel effect (RNCE), we demonstrated the STI thickness role on the active area stress, on the contact leakage, on the poly CD, and on the isolation. The deterioration of 1 Mbit SRAM yield is observed if STI is too thin.

1. Introduction

STI planarity obtained by Chemical and Mechanical Polishing (CMP) is a key parameter for the control of the device electrical behavior. CMP polishing time controls the STI thickness before the poly deposition. This STI thickness controls partly the local oxide edge recess and thus the narrow channel effect [1].

Usually, for advanced ULSI, RNCE is the main response analyzed. Stress in active area leads to dislocation study. In addition, we present here the effect of performance shift related to the stress function of the STI thickness. Then, isolation is impacted as the STI is masking the implantation. Depending on the gate patterning process, it is found that the poly CD can be related to the STI thickness. Finally, junction leakage impacted by the contact etch may be related to the STI thickness, it depends on the etching recipe. At the end, SRAM behavior will be analyzed as a function of the STI thickness.

2. Process results

STI process flow contains a 70Å pad-oxide, a 1600Å nitride and the trench depth is 3000Å. A single High Density Plasma (HDP) deposition is used to fill the trench and planarisation is obtained with standard CMP. STI thickness has been varied thanks to CMP overpolish (OP) after the end point detection triggering.

The resulting STI thickness has been varied from greatly higher than the active area to greatly lower than the active area. The figure 1 shows the nice correlation between the CMP overpolish time and the STI thickness before poly deposition.
The figure 2 and 3 illustrate by SEM cross sections the extreme variations of the STI thickness. The sections have been made in structures dedicated to misaligned contact junction leakage monitoring. It clearly shows that the STI thickness changes the W-plug to junction distance.

3. Electrical results

3.1 Stress effects on the electrical performances

Because of thermal treatments and of oxide growth after active patterning and box filling, stress fields in the active area can reach very strong values. The stress results either in dislocations [2], or at least in mobility shift and thus a performance shift [3].

The figure 4 defines what we call active length (2*SD length + gate length = active length). We plot in the figures 5 and 6 the Beta parameter of 10x0.11μ NMOS and PMOS for two different active lengths (0.8μ and 10μ).

Figure 4. Definition of the active length for a constant poly length

Figure 5. Beta variation between two different active lengths for a 10x0.11μ NMOS.

Figure 5 and 6 show an increase of the beta when the CMP overpolish is the longest. This can be related to both RNCE and CD Poly as it will be developed in the next paragraphs. The relevant parameter to be observed is the beta variation and not its intrinsic value.

If we assume that the beta variation is corresponding to the stress variation, these results show a decrease of the stress variation for NMOS and an increase for the PMOS for the thinnest STI. This has to be taken into account for further modeling of the stress consequences.

3.2 Impact on the isolation

Wells and Vt adjusts are implanted after the active patterning and STI planarisation. The figure 7 describes an example of structure used to test the Nwell-Pwell isolation, which is particularly critical for SRAM consumption in stand-by mode [4]. The STI thickness is represented equal to the trench depth on this figure, but it is usually not the case as shown in figures 2 and 3.

Figure 7. Schematic of the structure used to measure the Nwell-Pwell isolation before Wells implantations.

The figure 8 represents the leakage obtained when the N+ and P+ plugs in the Nwell are polarized and all other active are grounded. That shows a strong improvement of the isolation when the STI thickness decreases for the most aggressive structure (W STI = 0.24μ). The effect is less important on other geometries, but it goes in the same direction. Decreasing the STI improves isolation.

The figure 9 confirms in a way what is already observed in the figure 8. It shows the increase of the Nwell and Pwell resistances with the increase of the STI thickness. This makes sense simply because more doping species are lost in the STI when this one is thicker. Implantation profile peak for Nwell or Pwell is generally close to the bottom of the STI. Effects appear to reach more than 5% shift on a reasonable variation window of +/- 300Å.
Conclusion on isolation is that effect of STI thickness remains relatively limited, except for Nwell-Pwell leakage at the smallest dimension. Such dimension is used in sub-90nm technology SRAM by example.

### 3.3 Poly CD control

An increase of 30% in poly resistance is observed for both N+ and P+ unsalicided 0.11µ poly serpentine for the thinnest STI. In reasonable STI variation between 2800Å and 3300Å, the resistance increase remains below 5%.

Advanced processes for gate patterning currently use end point detection systems. These systems are dependent on the sub-layers, i.e. the STI for the poly etch. This is a hypothesis to explain why the STI thickness is an important parameter inducing variation of poly CD as it is shown on the figure 10.

Moreover, a barc/resist thickness variation occurs because of the STI topography. Swing curves are then locally modified, inducing a local CD variation.

### 3.4 Reverse narrow channel effect

It is well known that the main concern about STI planarity and uniformity deals with the off-state current leakage (Ioff) because of the RNCE effect. RNCE is directly related to the local edge oxide recess of the STI next to the active area before poly deposition. This local edge recess is stronger when the STI is thinner. This remains verified for our advanced processes, the figure 11 shows that the Ioff of a thin oxide device increases of roughly half a decade when STI is too thin. It is worth noting than the difference between the data obtained with the 0sec and the 15sec overpolish are pretty close.

### 3.5 Junction leakage related to contact etch

In the case of ULSI, design rules are such aggressive that active/poly and active/contact overlay is becoming a major concern. In very aggressive structures like SRAMs, it is likely that a non-negligible ratio of contacts is partially land on STI. Dedicated test structures containing misaligned contacts are presented in the cross sections of figure 2 and 3. These structures are able to monitor the W-plug / junction distance as a function of the STI overpolish time and the contact etch selectivity between the borderless nitride and the oxide of the STI.
The figure 12 illustrates the fact that if the etching is not enough selective, the contact plug creates a deep and leaky junction in the SD. When the etching is more selective, the leakage is almost not sensitive to the STI thickness. The slight increase observed for the thickest STI may be related to a shadowing effect of the STI during the junction implantation.

### 3.6 Gate oxide Reliability

The figure 13 quickly shows that no major concern appear about gate oxide reliability with the different CMP overpolish time. STI thickness does not appear to be a key parameter on the reliability.

![Figure 13. Weibull Qbd plot for a P+ poly / Nwell capacitance with a 65Å thick oxide.](image)

### 3.7 SRAM yield

SRAM functionality depends on the global leakage of the memory cell. Channel off-state current leakage and junction leakage are major contributors to the total consumption of the SRAM and consequently to the final yield. All data were obtained here with a selective contact etch. Active widths are going down to 0.13µ in this SRAM cell and OPC were used.

The figure 14 clearly shows the strong increase of the consumption of the 1Mbit SRAM memory when the STI is too thin. This is very well related to the prime yield observed. A first degradation and a strong dispersion is observed if overpolishing is pushed to 15sec. Up to 30sec, results become very bad.

![Figure 14. Static consumption of a 1 Mbit SRAM.](image)

![Figure 15. Prime yield of a 1 Mbit SRAM.](image)

### 4. Conclusion

This paper shows the expected importance of the STI thickness on RNCE. It has been related to the Yield results on a 1Mbit SRAM. But its consequence on the stress in the active area, isolation and poly CD should not be neglected. The absolute need of a selective contact etch is demonstrated. Only reliability does not exhibit a strong dependence.

### 5. References


