Abstract

A model for MOS capacitors in accumulation is presented, which is able to predict the nonlinear distortion accurately. The key idea of this work is to include the polysilicon gate depletion effect in that model.

Several test structures based on MOS capacitors in accumulation have been implemented with the object of validating the model and to explore the potential applications to high performance analog circuits fabricated in pure digital CMOS technologies. The model shows good agreement with experimental results.

1. Introduction

Nowadays, the prevailing technology is the digital one. In VLSI CMOS technologies intended mainly for digital circuits, the only available device is often the MOS transistor. Pure digital CMOS technologies rarely allow the use of polysilicon resistors (with silicide block) or double-pol y linear capacitors. Metal to metal capacitors are often used to implement linear capacitors; but these structures have the disadvantage of having very low specific capacitance and high mismatching errors, unless they are made using very esoteric techniques: Multiple metal level sandwiches or fractal capacitors [1].

In lack of special capacitor structures in standard digital technologies, the use of MOS capacitances has many advantages. Their major benefit, of course, is complete compatibility with all MOS technologies. It also provides a large specific capacitance per unit area, more precision in absolute value and are expected to have better matching properties [2]. Furthermore, as the absolute value of interlayer capacitances is poorly controlled in digital technologies, this kind of capacitors exhibits process variations as high as 20%. By contrast, the gate oxide capacitance is typically controlled with less than 5% error.

However, these capacitors have some drawbacks: they are nonlinear, have strong voltage dependence and their N+-silicon- to substrate parasitic capacitances limit their utility to RF applications. The voltage dependence originates from the variation of both the dielectric constant and the thickness depletion region within each plate. However, in spite of being a nonlinear element, capacitors presenting weak nonlinearities can be realized if this structure is properly biased.

To obtain capacitors as linear as possible, we focus on the use of MOS structures available in digital CMOS processes in place of metal-metal structures. The regions of interest of the C-V characteristic are the “flat” parts where the two terminal MOS structure operates either in accumulation or in inversion. It can be shown that for a certain gate-body bias and typical process parameters, accumulation capacitors tend to be more linear than inversion capacitors [3]. The distortion generated by a capacitor operating in inversion is higher than that generated by one operating in accumulation and, is a reason for considering accumulation capacitors.

An alternative to implement linear capacitors with high specific capacitance instead of the low-capacitance density metal-metal capacitors thus avoiding the need for additional processes, is to use the gate-to-channel capacitance of MOSFET devices as capacitors where gate oxide thickness is a variable which is well controlled in the process. This is typically used in pure digital CMOS technologies.
involves majority carriers with rates of generation greater
than minority ones mixed up in inversion mechanisms. In
consequence, inversion based capacitors present lower
specific capacitances than accumulation based
counterparts (up to 1:5 ratios) in non-quasistatic
operation mode (above 10 Hz).

Before integrating, a design simulation must be
carried out in order to check whether everything works
correctly. There is one problem regarding capacitors; as
accumulation is a region which lacks importance for
transistor operation, SPICE MOS transistor models in
this particular region are not accurate. Therefore, the
interest emerges on presenting a model for MOS
capacitors in accumulation, which will be able to predict
distortion accurately.

The nonlinearity in semiconductor capacitors can be
expressed as a capacitance voltage dependence. However,
since the actual expressions for this
defpendence can be quite complex, it is common practice
to model the nonlinearity in a polynomial way, i.e., by
using a Taylor expansion. This approximated model, not
always provided, is insufficient for accurate simulations
required in high performance analog circuits.

In mixed-signal integrated circuits; antialiasing filters,
smoothing filters and converters must offer at least the
same accuracy as the associated digital signal processor.
However, this requirement is not easy to achieve by
using capacitors from pure digital technologies. For
example, dynamic range and linearity better than 60 dB
are necessary for a modest 10-bit processor.

The physical-based model proposed in this work will
permit the computing distortion levels in continuous-time
filters and integral nonlinearity due to capacitive
nonlinearity in digital-to-analog converters in a more
accurate way, at the same time that it permits one to
advance in the study of mismatching reduction and
layout optimization.

The model can also be used for other structures, not
exclusively capacitive, such as poly resistors. For
example, many digital-to-analog converter architectures
are based on high-precision resistor-ladder structures,
which use poly resistances in standard CMOS
technologies. The poly depletion effect limits the
absolute precision and matching of this type of resistive
element.

A structure operating in accumulation mode suitable
for an N-well CMOS technology has been chosen. It is
desirable to ensure that the structure operates in
accumulation even with small bias values. Submicron
CMOS technologies present increasingly low supply
voltages, and therefore are closer to the flatband voltage.
In order to guarantee a low bias voltage value, an N+
polysilicon gate should be chosen in an attempt to make
the flatband voltage as small as possible [5].

The key idea of this work is to include the polysilicon
gate depletion effect in a model of this kind of
capacitor. The basis of the operation can be briefly
explained as follows: when a positive voltage (higher
than the flatband voltage) is applied to the gate,
negative charges are attracted to the oxide-
semiconductor interface and this phenomenon leads to
an accumulation of electrons at the surface forming a
channel (accumulation layer).

Note that a depletion layer appears in the gate due
to the finite doping density of the N+ polysilicon whose
thickness depends on the concentration of donors in the
N-well. The cross section of an N-poly, N-well
capacitor illustrating this effect is shown in Fig.1.

Figure 1. Cross section of an N-polysilicon,
N-well capacitor

2. Model Equations and Implementation

We present now the relations used in our study to
model the accumulation MOS capacitor. Nevertheless, to
obtain a more detailed explanation of the background of
these equations the reader is referred to [4].

In the analysis, the magnitudes are the potential drop
across the oxide ($\psi_{ox}$), the surface potential ($\psi_s$) and
the potential corresponding to the work function difference
of the bulk and gate materials ($\phi_{MS}$). Potential balance
equation by Kirchhoff’s voltage law (1), charge balance
(2) and the expression used to define the flatband voltage
of the two terminal structure (3) are:

$V_{GB} = \phi_{MS} + \psi_{dep} + \psi_{ox} + \psi_s$ (1)

$Q_G' + Q_x' + Q_o' = 0$ (2)

$V_{FB} = \phi_{MS} - \frac{Q_o'}{C_{ox}}$ (3)

We define the body effect coefficients for well ($\gamma$)
and poly ($\gamma_p$), as:

$\gamma = \sqrt{2q\epsilon_i N_D/C_{ox}}$ (4)

$\gamma_p = \sqrt{2q\epsilon_i N_{POLY}/C_{ox}}$ (5)

From basic electrostatics we obtain the potential drop
across the oxide and the charge per unit area on the gate:

$\psi_{ox} = \frac{Q_G}{C_{ox}}$ (6)

$Q_G' = \sqrt{2q\epsilon_i N_{POLY} \psi_{dep}}$ (7)
Using these expressions in equation (1) leads to:

\[ V_{GB} = V_{FB} + \psi_s + \psi_{dep} + \gamma \frac{\phi_t}{\phi_s} \exp \left( \frac{\psi_s - \phi_t}{\phi_s} \right) - \frac{\phi_t}{\phi_s} \psi_s - \phi_t \]  

(8)

With (1) and (6) we obtain:

\[ Q_G = C_{ox} (V_{GB} - \phi_{MS} - \psi_s - \psi_{dep}) \]  

(9)

Then, operating with (7) and (9), and defining (5), we obtain an expression for the potential drop across the gate depletion layer \( \psi_{dep} \):

\[ \psi_{dep} + \gamma_p V_{dep} - (V_{GB} - \phi_{MS} - \psi_s) = 0 \]  

(10)

If we solve this equation and make the approximation \( \gamma_p^2 / 4 \gg V_{GB} \), which is reasonable for practical values of process parameters and bias voltages, the solution can be simplified to give:

\[ \psi_{dep} = \left( V_{GB} - \phi_{MS} - \psi_s \right)^2 / \gamma_p^2 \]  

(11)

With this simple analytic expression and knowing the surface potential \( \psi_s \), we can obtain \( \psi_{dep} \).

We have made an approximation, which must be verified in our model. If this assumption is accurate, \( \psi_{dep} \) is a small fraction of \( V_{GB} \) and equation (8) can be changed into:

\[ V_{GB} = V_{FB} + \psi_s + \gamma \frac{\phi_t}{\phi_s} \exp \left( \frac{\psi_s - \phi_t}{\phi_s} \right) - \frac{\phi_t}{\phi_s} \psi_s - \phi_t \]  

(12)

With these expressions, we can solve (12) numerically for \( \psi_s \) and \( V_{GB} \) given. On the other hand, an explicit expression for the surface potential could be obtained for typical values of temperature and \( \gamma \)[5].

\[ \psi_s = 2 \phi_s \left( \frac{V_{GB} - V_{FB} + 3 \phi_t}{V_{GB} - V_{FB} + 6 \phi_t} \right) \log \left( 1 + \frac{V_{GB} - V_{FB}}{\gamma \phi_t} \right) \]  

(13)

Now, supposing a variation in the voltage across the two terminal structure we define:

\[ C'_{gb} = \frac{1}{C'_{ax}} + \frac{1}{C'_{c}} + \frac{1}{C'_{dep}} \]  

(14)

where \( C'_{ax} \) is the oxide capacitance per unit area, \( C'_{c} \) is the capacitance of the accumulation layer per unit area:

\[ C'_{c} = \frac{dQ'_c}{d\psi_s} = \gamma_c c'_{ax} \frac{\exp \left( \frac{\psi_s}{\phi_s} \right) - 1}{2 \phi_t \exp \left( \frac{\psi_s}{\phi_s} \right) - \psi_s - \phi_t} \]  

(15)

and \( C'_{dep} \) is the capacitance of the gate depletion region per unit area:

\[ C'_{dep} = \frac{dQ'_c}{d\psi_{dep}} = \frac{\gamma_p^2 c'_{ax}}{2(V_{GB} - \phi_{MS} - \psi_s)} \]  

(16)

In the proposed model, for a given \( V_{GB} \), the capacitance of the two terminal MOS structure can be obtained using these steps:

a) Calculate \( \psi_s \) with the approximate MOS structure.

b) Use this value to calculate \( C'_{c} \) in (15) and \( C'_{dep} \) in (16).

c) Obtain \( C'_{gb} \) using (14).

In order to obtain the charge per unit area on gate \( Q'_G \), we use (9) as recommended in [5].

The model calculates \( Q_G, \psi_s \) and \( C_{gb} \) when temperature, \( V_{GB} \) and dimensions of the MOS structure are introduced.

In a two terminal MOS structure, there is a reverse biased junction between the N-well and the substrate. The depletion region can be modelled as a capacitance between the two zones. This parasitic component must be included in the final model of the capacitor.

It has been implemented in MATLAB and it can be coded as a ‘C’ routine to be included in a general purpose circuit simulator. It also calculates distortion, which is highly dependent on derivatives of the C-V characteristic, and consequently it allows checking the accuracy of the model.

The proposed model is also valid for poly-diffusion capacitive structures implemented with technologies which permit it (BiCMOS, for instance). It can also be used to make precise calculations in double-poly structures because it models a nonlinearity not previously considered in the design kits which are known by the authors.

3. Measurement Results and Discussion

Several designs of MOS capacitors have been characterized measuring curves C-V in accumulation using a standard CMOS process. The gate oxide thickness for them is 45 Å.

Fig. 2 compares measurement results with our model whether considering the poly depletion effect or not, showing the best fit if this effect is introduced.
depletion effect is considered and donor density varied in the N-well; and we find that the C-V curve is flatter at bias values closer to the flatband voltage. Furthermore, the slope of the curve is smaller considering the great values of N-well density. These results must be considered when it comes to the design of capacitors.

4. Conclusions

Several test structures have been implemented with the object of validating the proposed model. They are based on MOS structures in accumulation and mean to improve basic characteristics such as a larger capacitance. We have taken special care in reducing the substrate resistance using a moderate poly area and rings with multiple contacts around that area being used as the contacts of the bottom plate of the MOS capacitor. Several possible layouts are currently under consideration. We are also thinking about an interdigitized structure, which is very appropriate for forming capacitor arrays, and a waffle-shaped capacitor. These are just some examples of layout styles which are, among others, under consideration. We are presently waiting for the integration of other test structures, nevertheless, the authors have committed themselves to present experimental results at the symposium.

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6. References