Si/SiGe Cross-hatching: a Good Indicator of Strained Si MOSFET Performance?

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Abstract

The impact of MOS processing on strained Si/SiGe device structures grown by CVD and MBE having different as-grown surface roughness has been examined. The Si/SiGe morphology was found to change dramatically with processing. Certain processes caused reactions common to both material types whereas others yielded dissimilar responses, suggesting that as-grown Si/SiGe surface roughness, commonly used as an indicator for material quality, is not justified. High thermal budget processing was found to degrade the surface roughness while low temperature processing did not. Thus a key performance limiting mechanism of Si/SiGe FET devices fabricated with a high thermal budget, i.e. MOSFETs but not MODFETs, has been identified, in agreement with experimental data.

Filtering AFM roughness data of specific wavelengths enabled the effects of processing on large-scale surface roughness and smaller scale microroughness to be investigated. Methods to reduce the surface roughness are discussed.

1. Introduction

The increased electron mobility in strained Si can be used in n-channel heterojunction MOSFETs (HNMOSFETs) to extend the lifetime and performance of CMOS technology [1]. Strained Si can be obtained by epitaxially growing Si on a relaxed SiGe ‘virtual substrate’ (VS). However, such growth leads to periodic surface roughness known as ‘cross-hatching’ [2]. Considerable work has been carried out to minimise the cross-hatching, which often exhibits peak to peak roughness of tens of nanometers. One method used is chemical-mechanical polishing (CMP). Electron mobility enhancements of 120% have recently been demonstrated in strained Si surface channel HNMOSFETs fabricated on a VS smoothed by CMP [3]. In addition a sample from the CVD wafer was given a low thermal budget oxidation. The dependence of surface morphology on ambient was studied by subjecting CVD samples to rapid thermal annealing (RTA) at high, medium and low thermal budgets (Table 2). Finally, samples of both SiGe wafers were subjected to two sequential RCA cleans, representing active area exposure prior to gate oxidation. Two RCA procedures were also carried out on all samples prior to thermal processing. Si control samples were processed simultaneously.

2. Experimental details

Two types of strained Si/SiGe material with differing as-grown roughness were generated on which to perform the experiments. A conventional MBE method was used to provide VS material with severe cross-hatching (Fig. 1(a)), while modifications to the equipment enabled ultra-low pressure CVD growth resulting in significantly smoothed material (Fig. 1(b)) [4]. SIMS and XRD confirmed the Ge concentration in the VS (~30%) and the relaxation in the VS (~99%) for both wafers. TEM verified that the strained thickness was below the critical thickness [5].

The effects of processing on surface roughness of MOS architectures was investigated using AFM, since electrical data was not available from the part processed samples. Samples from both SiGe wafers were given high and medium thermal budget oxidations (Table 1). In addition a sample from the CVD wafer was given a low thermal budget oxidation. The dependence of surface morphology on ambient was studied by subjecting CVD samples to rapid thermal annealing (RTA) at high, medium and low thermal budgets (Table 2). Finally, samples of both SiGe wafers were subjected to two sequential RCA cleans, representing active area exposure prior to gate oxidation. Two RCA procedures were also carried out on all samples prior to thermal processing. Si control samples were processed simultaneously.

3. Results and discussion

Roughness at all correlation lengths probed by AFM was found to be greater for the MBE material than for CVD material, as shown in the spatial frequency spectrum in Fig. 2, obtained by fast Fourier filtering roughness data. The data shown are the mean rms roughness values from numerous 25 µm x 25 µm scans around the wafers. The peak in the relative roughness in the second lowest frequency band highlights the largest difference between the roughness of the two material types, and confirms that the dominant wavelength of the
RCA cleaning on strained Si microroughness was hatch morphology dominated the rms roughness where microroughness must first be evaluated. Since the cross-

Therefore, the effect of RCA cleaning on strained Si to reductions in performance of conventional devices [6].

including those used in the present study, which has led concentrations of chemicals used in RCA cleaning,

HNMOSFET performance. However, surface roughness and potentially improving the uniformity of cross-hatching.

The overall rms roughness was found to be below the resolution of the AFM both before and after RCA cleaning. This suggests that the microroughness of strained Si was above that of unstrained Si before and after RCA cleaning. The improvement of strained Si microroughness following RCA cleaning contrasts Czochralski Si.

The impact of oxidation on MBE material is shown in Fig. 3. The roughness was found to reduce following the O₂-medium oxidation and increase with thermal budget (O₂-high), compared with RCA-cleaned samples. Unstrained Si is known to initially roughen before smoothing during oxidation [7]. The AFM images revealed the presence of sub-micron roughening on all areas measured on the MBE sample subjected to the O₂-high oxidation, while only one location investigated following the O₂-medium oxidation displayed such morphology. Fig. 5(a) shows representative 25 µm x 25 µm 3D AFM images of the MBE material prior to processing and following the O₂-medium and O₂-high oxidations. The increase in roughness on the O₂-high sample is evident while the as-grown and O₂-medium samples appear similar. The AFM images of the O₂-high sample were filtered, allowing roughness only at certain frequency bands to be observed, and confirmed that the enhanced microroughness was randomly orientated.

The microroughness of CVD material also increased following oxidation, as shown in Fig. 5(b). The roughness at shorter wavelengths was more prominent than observed for MBE material. Further, all oxidations on CVD material, including O₂-low, caused severe

Table 1. Oxidation conditions

<table>
<thead>
<tr>
<th>Oxidation Process</th>
<th>Temperature (ºC)</th>
<th>Time (min)</th>
<th>Ambient</th>
</tr>
</thead>
<tbody>
<tr>
<td>O₂-high</td>
<td>800</td>
<td>120</td>
<td>O₂</td>
</tr>
<tr>
<td>O₂-medium</td>
<td>800</td>
<td>60</td>
<td>O₂</td>
</tr>
<tr>
<td>O₂-low</td>
<td>750</td>
<td>60</td>
<td>O₂</td>
</tr>
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</table>

Table 2. RTA conditions

<table>
<thead>
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<th>RTA process</th>
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<th>Time (sec)</th>
<th>Ambient</th>
</tr>
</thead>
<tbody>
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<td>N₂-high</td>
<td>1050</td>
<td>20</td>
<td>N₂</td>
</tr>
<tr>
<td>N₂-medium</td>
<td>950</td>
<td>20</td>
<td>N₂</td>
</tr>
<tr>
<td>N₂-low</td>
<td>850</td>
<td>20</td>
<td>N₂</td>
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</tbody>
</table>

Table 3. Single RCA clean procedure

<table>
<thead>
<tr>
<th>Process step</th>
<th>Chemicals</th>
<th>Mixing ratios</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (RCA1)</td>
<td>H₂O,NH₄OH:H₂O₂</td>
<td>5.3:1.4:1.0</td>
</tr>
<tr>
<td>2</td>
<td>DI H₂O</td>
<td>-</td>
</tr>
<tr>
<td>3 (RCA2)</td>
<td>H₂O,HCl:H₂O₂</td>
<td>6.6:1.0:1.0</td>
</tr>
<tr>
<td>4</td>
<td>DI H₂O</td>
<td>-</td>
</tr>
</tbody>
</table>

Figure 1. AFM images and linescans of as-grown Si/SiGe material: (a) MBE, (b) CVD. The dissimilar scales highlight the growth-dependent morphology.

MBE material is shorter than that of CVD material. The dominant cross-hatching wavelength on the MBE material is approximately 2.0-2.5 µm whereas the main wavelength of the CVD material is approximately 6 µm (Fig. 1).

The impact of processing on surface roughness of MBE material is shown in the spatial frequency spectra in Fig. 3. The data is collected from several 40 µm x 40 µm scan areas around the wafer. The electrical noise of the AFM was less than 0.9 nm. Fig. 3 shows that the main energy within the distribution arises from the lowest frequency band. The overall rms roughness measured by the AFM is therefore dominated by cross-hatching.

At each frequency band resolved there was a significant reduction in roughness following RCA cleaning. The average rms roughness was found to decrease by 30% following cleaning and the variation in roughness decreased by over 50% in terms of the standard deviation of the mean value compared with roughness measurements on as-grown material. A similar trend was observed for RCA-cleaned CVD material. The overall roughness was reduced by 20% following RCA cleaning and the variation in roughness was reduced by approximately 60%.

Fig. 3 suggests that the use of RCA cleaning may provide a useful route to reducing the cross-hatch roughness and potentially improving the uniformity of HNMOSFET performance. However, surface microroughness of Czochralski Si is increased by certain concentrations of chemicals used in RCA cleaning, including those used in the present study, which has led to reductions in performance of conventional devices [6]. Therefore, the effect of RCA cleaning on strained Si microroughness must first be evaluated. Since the cross-hatch morphology dominated the rms roughness where more than one cross-hatch period is enclosed, the effect of RCA cleaning on strained Si microroughness was
roughening with little dependence on oxidation thermal budget. Thus, despite the improved as-grown morphology of Si/SiGe CVD material, the material appears to be more susceptible to roughening during oxidation than MBE material. These results are important because although the reduced cross-hatch severity of CVD material was maintained in terms of its amplitude following oxidation, the increase in roughness occurred at higher frequencies which may degrade carrier mobility. Therefore enhanced electrical performance of strained Si/SiGe surface channel devices is not necessarily due to the cross-hatching roughness. The observed increase in roughness at shorter wavelengths could not be quantified from spectral analyses due to accuracy limitations in filtering roughness wavelengths.

Annealing in N$_2$ was also found to degrade the morphology of the CVD material. The increase in microroughness at wavelengths below the dominant cross-hatching roughness was even more notable than that following oxidation. However, unlike the oxidised samples, roughness correlation lengths appeared to decrease with increasing thermal budget. These results suggest that the surface roughness of strained Si at wavelengths more likely to influence carrier mobility than cross-hatching roughness is affected by thermal budget opposed to ambient. Further, the results show that it is inappropriate to use as-grown surface roughness as an indicator for device performance, rather roughness following processing should be considered.

Strain relaxation should not occur with the resulting epilayer thicknesses. However, both types of material used were grown at relatively low temperatures (550-600 ºC). The roughening of the strained Si/SiGe material during high temperature processing may be a consequence of the ability of ions to move towards a minimum surface energy configuration at temperatures not experienced by material grown at such low growth temperatures. This agrees with the best HNMOSFET performance to date arising from material grown at high temperature [8].

The oxidation and annealing induced surface roughening on strained Si will additionally cause issues in the quality of silicides formed on the source and drain regions. In order to achieve extrinsic as well as intrinsic performance gains in strained Si/SiGe HNMOSFET devices, higher temperature material growth or a reduction in the VS alloy composition may be necessary. Since surface channel HNMOSFET device structures require only enough strain to split the conduction bands, it is anticipated that reducing the alloy composition to approximately 15% will yield improved device performance arising from enhanced material properties without the technological issues presented above. Reduced thermal budget processing commensurate with device scaling should also assist in minimising the interface roughness of strained Si/SiGe structures.

Reduced thermal budget processing commensurate with device scaling does not require either the high temperature gate oxide process or the source and drain implant activation stage, the morphological distortion following fabrication is likely to be considerably reduced.
compared with MOSFET processing. This may explain the high performance demonstrated by strained Si/SiGe n-channel MODFETs [9] while the performance of strained Si HNMOSFET devices to date remains below theoretical predictions.

4. Conclusions

The impact of processing Si/SiGe material has been investigated. CVD material displaying vastly improved as-grown cross-hatch morphology compared with MBE material was found to be more susceptible to increased surface microroughness from high thermal budget processing than MBE material. This demonstrates that it is unsuitable to use unprocessed Si/SiGe material quality in terms of cross-hatching roughness as an indicator for strained Si/SiGe MOSFET device performance.

High thermal budget processing in both O₂ and N₂ ambients caused an increase in high frequency roughness on both types of strained Si/SiGe material. Conversely low temperature RCA cleaning reduced both the cross-hatching roughness and the microroughness of strained Si material. The closer agreement between experimental data for strained Si/SiGe n-channel MODFETs and theory compared with strained Si/SiGe n-channel MOSFETs is considered to be due to the differences in the fabrication process; MODFETs do not require high temperature processing and therefore avoid increased surface roughness. Reducing the alloy composition, lower thermal budget MOS processing and increasing the material growth temperature may promote robustness of strained Si/SiGe material during fabrication, yielding greater performance advantages of surface channel HNMOSFET devices.

5. Acknowledgements

The work is supported by EPSRC. The authors wish to thank Southampton University Microelectronics Centre for the use of the clean room facilities, David Norris for TEM measurements and Evans Europa Ltd. for SIMS.

6. References