Abstract

The surface component of reverse current is a serious limitation for the operation of high voltage/current devices at high junction temperature. This component may induce reverse current-voltage instability of a PN junction followed by device failure during high temperature operation. Experimental results are presented for silicon rectifier diodes revealing the influence of the junction surface leakage current on the reverse I-V characteristics. Known results for silicon carbide PIN diodes are considered for comparison. Available PN junction passivation methods at this time are not effective enough in controlling the junction surface leakage current.

Improved surface passivation techniques are required to achieve reliable device operation, especially above 200 °C.

2. Experimental results. Discussion

Typical results that reveal the influence of junction surface effects on the reverse I-V characteristics are shown in Fig.1. This data relates to a mesa type silicon P'NN' structure of about 16mm² area and passivated with organic dielectric (silicone rubber). The used passivation method has the advantage that for the same structure, the passivation dielectric layer can be removed and the passivation process repeated.

Planar oxide and glass passivated junctions of about the same area and breakdown reverse voltage as those considered in Fig.1 have also been investigated. For some of them the passivating oxide was removed and a re-passivation by using organic dielectric was performed. It has been found that the state of the silicon junction surface in direct contact with the dielectric layer is of great significance for I-V reverse characteristic stability at Tj higher than 200 °C whilst the nature of the dielectric passivation material (organic or inorganic) is of less importance. The results in Fig.1 show a significant reduction in the value of reverse current, IR, takes place after heat treatment at 300 °C and that since the same behavior is repeated with the second passivation and anneal cycle, then this must be attributed to a reduction in surface related current. Fig.1 also show that a low level of IR near room temperature does not necessarily provide a low IR at high Tj. By heat treatment of the diode structure, changes in the state of the double electric charge layer (surface states) from the silicon-silicone rubber interface may occur. The properties of the dielectric material are not the same before and after heat treatment. Further experiments taking into account a correlation of the IR level with the junction area and its perimeter have indicated that the I-V characteristics in...
Figure 1. Current–voltage characteristics for a silicon controlled-avalanche diode structure with organic dielectric passivation near room temperature and above 200°C junction temperature. Fig.1 after heat treatment at 300 °C are still influenced by the surface component.

Investigated glass or oxide passivated junctions of available commercial devices with a silicon die of about the same dimensions, breakdown voltage and charge carriers lifetime as that used in Fig. 1, exhibited $I_{R}$ values above 200 °C not less than the lowest level shown in this figure. Consequently, the $I_{R}$ level of junctions passivated with inorganic dielectric is not lower than those passivated with organic dielectric and may be also controlled by surface phenomena.

Other examples that demonstrate the influence of the surface component on the level of $I_{R}$ are shown in Fig.2. This time a mesa P⁺N⁺N⁻ rectifier silicon structure of 16 mm² area but with an expected bulk breakdown voltage higher than 1500 V has been used and the graphs have been drawn with logarithmic voltage scales. The different I-V reverse characteristics shown correspond to three different re-passivations of the same silicon structure. The characteristics plotted after the 1st passivation relate to the situation when some contamination from the surrounding manufacturing ambience was permitted after the cleaning of the junction surface. Reverse characteristics for the 2nd and the 3rd re-passivations relate to a passivation process that was completed without allowing any influence from the surrounding manufacturing ambience. Nonetheless, some acid traces remained after the junction surface cleaning during the passivation process, more for the 2nd and less for the the 3rd re-passivation.

Fig. 2 shows that the surface component of $I_{R}$ has a significant influence not only on its level at room and higher junction temperature but also on the obtained breakdown voltage value. This time, significant voltage dependence of $I_{R}$ (soft surface breakdown characteristic) is manifested at room temperature well below the expected value of the bulk breakdown. At higher junction temperature the curvature of the characteristic towards 1000 V is significantly attenuated. As in the case of Fig.1 less voltage dependence of $I_{R}$ at room temperature observed in Fig.2 which may be favorable in reaching the bulk breakdown value determined at low current, does not provide low $I_{R}$ values at high $T_{J}$. In practice it is known that for higher reverse working voltages, above 1000 V, it is more difficult to reach the bulk breakdown voltage. Silicon controlled-avalanche diodes of breakdown voltage above 2000 – 3000 V are not easy to be realized.

While the level of reverse current at high junction temperature for the 1st passivation in Fig.2 is comparable with the corresponding one for similar commercial silicon diodes available on the market, for the other two passivation situations the level of leakage current is significant lower. It has also been found the blocking I-V characteristic of the drain junction of some investigated high voltage commercial power MOS devices of about the same area as for the diode structure used in Fig.2, does not exhibit lower $I_{R}$ values at high $T_{J}$ than it is shown in this figure. A saturation tendency of $I_{R}$ at lower $V_{R}$ and high $T_{J}$ observed in Fig.2 for the 1st and 3rd passivations cannot be considered evidence for the bulk diffusion component dominance because even lower $I_{R}$ values are obtained for the 2nd passivation case where visible voltage dependence is manifested. Consequently, in spite of significant reduced $I_{R}$ values at high $T_{J}$ obtained in Fig.2 its level continues to be under the influence of the surface component as in the Fig.1 case. Nonetheless, excessive high surface leakage current is prevented for the 2nd and 3rd passivation case.

High temperature reverse bias (HTRB) tests at 250 °C and 300 V for 250 hours have indicated good stability of the devices passivated in the same conditions as for the 2nd or the 3rd re-passivation cycle but no device from the first passivation cycle survived. These devices exhibited a relatively high initial $I_{R}$ level at 250 °C and
Figure 2. Electrical characteristics of a silicon high voltage rectifier diode passivated with organic dielectric; 1st passivation: permitted exposure of the junction peripheral surface to the surrounding manufacturing ambience; 2nd and 3rd passivations: without exposure to the ambient but with acid traces, more for the second and less for the third.

As a consequence, reliable operation of silicon high voltage diodes at junction temperature above 200 °C is only possible when the surface component of the reverse current is kept at a low level by suitable junction passivation process. Suitable chosen organic dielectrics for junction passivation may be more efficient at high temperatures than the presently used inorganic dielectrics.

The experimental results presented in this work were taken on high carrier lifetime PN junctions i.e. the density of bulk generation –recombination centers is low. However, for silicon fast recovery PN junctions the bulk component of $I_R$ may become the primary component at $T_J$ higher than 125 – 150 °C. [4]. Nevertheless even in this case, the surface component can still be a cause for reverse I-V characteristic degradation at elevated temperature.

To our knowledge PIN diodes based on SiC and with an area larger than 10 mm² are still not available even as demonstrating devices. However, a significantly lower level of $I_R$ for SiC based devices is expected because the carrier intrinsic concentration for this material is orders of magnitude lower than for silicon. Nevertheless it has already been observed in the literature that the experimental values for $I_R$ are orders of magnitude higher than predicted. Furthermore, published experimental reverse voltage characteristics for 4H-SiC or 6H-SiC diodes have been limited to less than 250 °C and voltages significantly lower than those given for the room temperature, [1,2]. For example in [1] experimental I-V reverse characteristics are shown up to 225 °C and 500 V for a 6H-SiC PIN diode with a diameter of 0.1 mm. At 225 °C and 500 V for the $I_R$ level a value of about $10^{-5}$ A/cm² is specified. The lowest $I_R$ level at 225 °C and 500 V resulted from experiments for Fig.2 is around of $10^{-4}$ A but for a silicon PIN diode of 16 mm² area. A current density (per cm²) correlation would not be correct for the silicon diode because of the significant influence of surface current.

Evidently, high temperature surface passivation is an issue that will need to be addressed to successfully realize the full potential not only of silicon, but of SiC as well.

3. PN junction physical model

The experimental results presented in Figs.1-2 can be understood by taking into account surface electrical phenomena of the types shown in Fig.3. Either a surface inversion, depletion or accumulation layer may cause surface leakage current at reverse bias voltage. The surface current component is dependent on the carrier intrinsic concentration. Consequently, for silicon based junctions a significant higher level of $I_R$ is expected than for semiconductors with higher band gap energy. Besides the bulk component of $I_R$ uniformly distributed over the junction area, the surface component may be non-uniformly distributed over the junction perimeter so that reverse current crowding may be favored in some
local regions. Ideally, the junction passivation process would prevent a surface space charge layer forming to assure device ability for operation at $T_j$ higher than 200°C. In practice a surface depletion or inversion layer as it is the case in Fig. 1 before annealing or in Fig. 2 ($1^{st}$ passivation) may be responsible for excessive high $I_R$ at high $T_j$. A charge accumulation layer as it is the case in Fig. 1 after annealing or in Fig. 2 after the $2^{nd}$ and $3^{rd}$ passivation can reduce the surface leakage current. With a decrease in the doping concentration of the starting silicon material necessary to obtain high working voltages, the formation of a surface space charge layer at the semiconductor surface is more difficult to be controlled. More influence on the level of $I_R$ at high $T_j$ or on the obtained breakdown voltage value is expected. A weak accumulation layer obtained by suitable junction passivation could be acceptable for high junction temperature operation providing low level of $I_R$ from low to high reverse voltage. Annealing process and silicon surface treatment with acid traces so that to avoid a contamination from the surrounding ambient are thought to be instrumental in creating these conditions.

4. Conclusion

The results presented indicate that high temperature operation of silicon power devices may be still affected by a significant surface leakage current component. Presently available junction passivation based on the Si-SiO$_2$ interface does not appear to provide an adequate control of leakage current needed to fully realize the potential of silicon at temperatures above 200°C. This is an issue that will be particularly relevant to the successful introduction of SiC devices.

5. References