Physically-Based Matching Model for Deep-submicron MOS Transistors

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Abstract

This paper presents a new physically-based deep-submicron MOS transistors matching model that eliminates the large discrepancy between measured matching parameters and the values computed with the existing matching models. Previously neglected effects specific to the deep-submicron MOSFETs with highly doped channel and ultra-thin gate such as channel and gate random dopant fluctuation, gate depletion and quantum mechanical effects in the inversion layer are considered. Analytical expressions that relate the threshold voltage and current factor mismatch coefficients to the process parameters were developed. The proposed matching model was validated through experimental measurements performed on several consecutive deep-submicron technologies: 0.35, 0.25, 0.18, 0.15 , 0.13 and 0.1µm.

1. Introduction

Predicting the impact of device mismatch on the performance of analog circuits requires a high accuracy matching model. The recent advancements in the deep-submicron CMOS technology that pushed the minimum gate size to below 100nm and the oxide thickness to less than 3nm, made invalid most of the assumptions under which the existing matching models were developed. If in the micron and moderate submicron devices with low doped channel (10^{15} - $10^{17}cm^{-3}$) the threshold voltage mismatch was contributed by the physical oxide thickness and to a lower extend by the depletion charge fluctuation, in the actual deep-submicron devices with channel doping higher than $10^{18}cm^{-3}$ it is dominated by the random channel dopant fluctuation and the increase of the effective oxide thickness due to the gate depletion and the quantum mechanical effects in the inversion layer. The mobility matching of micron devices was dominated by the interface charge scattering, whereas in state of the art deep-submicron devices with highly doped channels ($>10^{18}cm^{-3}$) it is given by Coulomb scattering with channel dopants in weak inversion and by surface-roughness scattering in strong inversion regime.

Pelgrom [1] has introduced the area mismatch law: for a parameter P, $\sigma(P)=A_P/\sqrt{(2W\cdot L)}$, where A_P is the area mismatch coefficient. This law holds also for the deep-submicron devices if the effective gate area is considered ($W_{eff}*L_{eff}$), instead of the geometric one (W*L) [2]. Lakshmikumar [3] has proposed a physically-based model in which the threshold voltage mismatch is dependent on the oxide thickness and the depletion charge and the mobility mismatch is dominated by the interface charge. Bastos [4] has added short and narrow channel effects corrections to the threshold voltage mismatch. However these corrections are not necessary for the actual CMOS processes in which the source and drain halo implant depress the short and narrow channel effects. Stolk [5] and Asenov [6] have developed physically-based matching models for the threshold voltage considering the impact of random channel dopants fluctuation. When the oxide thickness is reduced below 3nm, the gate depletion becomes a major contributor to the threshold voltage fluctuation [6]. When the effective transversal electric field increases above 1MV/cm and the inversion layer centroid becomes comparable with the depletion layer width, the quantum mechanical effects significantly impact the threshold voltage mismatch [7].

The measured threshold voltage (A_{VTO}) and current factor (A_β) matching coefficients of sub-0.25µ MOSFETs show large discrepancies in comparison to the values computed with existing matching models. The aim of this paper is to develop a physically-based matching model portable to all major circuit level simulators, that allows a correct evaluation of the deep-submicron devices matching coefficients as a function of their process parameters.

2. Threshold voltage matching model

Actual ultra-thin gate devices use a non-degenerate gate doping to avoid impurity penetration through the gate oxide. The reduced doping level in the polysilicon gate leads to the appearance of a depletion layer near the polysilicon-oxide interface when the device is biased in strong inversion. This effect called polysilicon depletion increases the total equivalent oxide thickness, reducing the inversion layer charge and enhancing the threshold voltage fluctuation [6]. The impact on A_{VTO} is more pronounced in devices with sub-3nm gate oxide. Equating the depletion layer charge in the channel with the depletion layer charge in the gate, the surface potential of the poly-Si gate (Ψ_g) can be computed, leading to a corresponding gate depletion width (W_g):

$$\Psi_g = 2\cdot\Phi_F\cdot N_{ch}/N_g \rightarrow W_g = \sqrt{4\varepsilon_{si}\Phi_F\cdot N_{ch}/qN_g{}^2} \quad \mathbf{(1)}$$

where Φ_F is the Fermi level in the channel N_g is t he

polysilicon gate doping and N_{ch} is the average channel doping. Considering the difference in permitivity coefficients from the poly-Si gate to the SiO_2 the equivalent increase of the effective gate oxide thickness is obtained ($\Delta t_{ox}=w_g \cdot \varepsilon_{ox}/\varepsilon_{si}$). The n-MOSFETs use highly doped n+ polysilicon gates that results in low polysilicon depletion effect, while the p-MOSFETs need a more lightly doped p+ polysilicon gate due to a higher acceptor dopants diffusivity. The PMOS devices tend to have a higher threshold voltage mismatch due to both higher channel doping and higher gate depletion.

The increase of the channel doping to above $10^{18}cm^{-3}$ and the reduction of the oxide thickness to below 3nm results in a very large transversal electric field that leads to a strong quantization of the carrier motion in the inversion layer. The carrier density does not have the maximum at the interface (as assumed by the classical theory), but at a given depth named inversion layer centroid, while the density vanishes at the interface. The dependence of the centroid (z) on the effective inversion layer transverse electric field (E_{eff}) is given by [7]:

$$z = z_0 \cdot (E_{eff} / [1MV/cm])^{-n} \quad \textbf{(2)}$$

$$z_0 = 1.783 - 0.107 \cdot \ln(N_{ch}[cm^{-3}]/10^{16})\ [nm]$$

$$n = 0.459 - 0.033 \cdot \ln(N_{ch}[cm^{-3}]/10^{16})$$

In deep-submicron devices with high channel doping, when the depletion region width (w_d) approaches the centroid of the inversion layer, the effective transversal electric filed (E_{eff}) is given by:

$$E_{eff} = \frac{1}{\varepsilon_{si}} \cdot \left(\frac{Q_I}{2} + (1 - \frac{z}{w_d}) \cdot Q_D \right) \quad \textbf{(3)}$$

The impact of the centroid on the surface potential is took into account by introducing a depletion layer surface potential at threshold ($\Psi_d = 2 \cdot \Phi_F - z \cdot Q_I/\varepsilon_{si}$). The resulting depletion charge (Q_D) is equal to:

$$Q_D = \sqrt{2 \cdot \varepsilon_{si} \cdot q \cdot N_{ch} \cdot (\Psi_d - kT/q)} \quad \textbf{(4)}$$

where the kT/q correction term accounts for the majority carriers tail in the depletion layer edge.

The inversion layer charge density (Q_I) accounts both for the gate voltage loss due to polysilicon gate depletion (Ψ_g) and the centroid impact on the surface potential (Ψ_d):

$$Q_I = \frac{\varepsilon_{ox}}{T_{ox_eff}} (V_G - V_{FB} - \Psi_d - \Psi_g - Q_D \cdot \frac{T_{ox}}{\varepsilon_{ox}}) \quad \textbf{(5)}$$

where V_G is the gate voltage and V_{FB} is the flat-band voltage. The effective oxide thickness (T_{ox_eff}) that cumulates the geometric thickness (T_{ox}) with the gate depletion (w_g) and inversion layer centroid contribution is:

$$T_{ox_eff} = T_{ox} + (w_g + z + L_D/2) \cdot \varepsilon_{ox} / \varepsilon_{si} \quad \textbf{(6)}$$

The $L_D/2$ term accounts for the fact that carriers within a Debye length (L_D) behind the depletion layer contribute to the screening of random dopant charge in the channel [6]

The threshold voltage of deep-submicron MOSFET's at zero substrate bias (V_{TO}) that includes the gate depletion (Ψ_g) and quantum mechanical effects (Ψ_d) is given by:

$$V_{TO} = V_{FB} + \Psi_g + \Psi_d + Q_D \cdot T_{ox_eff} / \varepsilon_{ox} \quad \textbf{(7)}$$

The flat-band voltage has a negligible contribution to the V_{TO} mismatch due to the negligible interface charge and the weak logarithmic dependence of the work function difference on channel and gate doping levels.

Actual deep-submicron devices use non-uniform channel doping profiles to optimize the device characteristics. A good agreement with the experimental results was obtained by integrating the 1D depth distribution of the depletion charge and introducing an average channel doping concentration (N_{ch}). The resulting threshold voltage area mismatch coefficient (A_{VTO}) that considers both the random channel dopant fluctuation, and the gate oxide thickness increase due to polysilicon depletion and inversion layer centroid (T_{ox_eff}) is:given by:

$$A_{VTO} = \frac{\sqrt[4]{4 \cdot q^3 \cdot \varepsilon_{si} \cdot \Phi_F}}{\sqrt{3}} \cdot \frac{T_{ox_eff}}{\varepsilon_{ox}} \cdot \sqrt[4]{N_{ch}} \quad \textbf{(8)}$$

3. Current factor matching model

The current factor (β) mismatch is contributed by both the variation of device geometric dimensions (channel width (W) and length (L), and oxide thickness (Tox)) and the channel carrier mobility (μ). The variance of the current factor is obtained as the quadratic sum of the variances of the constituent elements:

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_W{}^2}{W^2 \cdot L} + \frac{A_L{}^2}{W \cdot L^2} + \frac{A_{Tox}{}^2}{W \cdot L} + \frac{A_\mu{}^2}{W \cdot L} \quad \textbf{(9)}$$

where A_W, A_L, A_{Tox} and A_μ are the area mismatch coefficients of respectively W, L, T_{ox} and μ. In the deep-submicron CMOS processes the width of the channel is defined by optical lithography, whereas the length is defined by deposition and etchback. Therefore for minimum L and W devices the dominant factor in channel area fluctuation is the width ($A_W >> A_L$).

The channel carrier mobility is limited by the scattering with the acoustic phonons (μ_P), and the surface-roughness (μ_{sr}), the Coulomb scattering with the ionized dopants from both the channel region and the oxide interface (μ_C), and the carrier-carrier scattering (μ_{CC}). The overall channel carrier mobility is obtained by combining the four scattering limited mobilities through the Mathiensen law:

$$\mu_{eff}{}^{-1} = \mu_p{}^{-1} + \mu_{sr}{}^{-1} + \mu_c{}^{-1} + \mu_{cc}{}^{-1} \quad \textbf{(10)}$$

The carrier-carrier scattering becomes non-negligible at channel carrier concentration (N_I) higher than $5 \cdot 10^{18}cm^{-3}$). However the surface-roughness scattering becomes dominant before the carrier-carrier one start to increase, Therefore μ_{CC} will be neglected in the present model. Most of the existing MOSFET matching models are based on the Sun-Plumer model [8] that considers the mobility fluctuation dominated by the N_f fixed oxide charge ($A_\mu\ \alpha 1/\sqrt{N_f}$) and independent of the channel doping. This model is valid only for the micron and moderate submicron devices that have low channel doping levels (10^{15} - $10^{17}cm^{-3}$), when the Coulomb

scattering with the channel ionized dopants is negligible.

The inversion layer mobility (μ_{eff}) plotted as a function of the effective transverse electric field (E_{eff}) follows an universal curve, independent of the substrate bias and doping and of the gate oxide thickness. Recent measurements showed a severe roll-off of the mobility from the universal characteristic at low electric field, that was attributed to the Coulomb scattering with the channel ionized dopants [9].

In the micron and moderate submicron CMOS processes with low effective electric field the channel carrier mobility is dominated by the Coulomb scattering with oxide interface charge. As the quality of the oxide was similar for several consecutive scaled-down processes, a constant current factor mismatch coefficient was observed [2]. This assumption is no longer valid, a significant decrease of the current factor mismatch coefficient being reported in the deep-submicron processes

In the actual deep-submicron MOSFETs the transverse electric field reaches values higher than 1MV/cm, leading to a strong quantization of the channel carriers energy levels even at room temperature. In the electrical quantum limit condition when most of the channel carriers lie in the lowest quantization subband the phonon scattering limited mobility can be expressed as: $\mu_P=K_p/(E_{eff}^{\ 1/3} \cdot T)$ [9], where T is the absolute temperature and K_p is a constant dependent on the phonon-limited bulk mobility. The T^{-1} temperature dependence is given by the scattering with intravalley acoustic phonons.

When the channel doping exceeds $10^{18}cm^{-3}$ the Coulomb scattering of the carriers with the ionized channel dopants dominates in weak and moderate inversion. Carriers in quantized states scatters mostly with charged centers located within a thermal length (L_{th}) away from the Si/SiO_2 interface. In actual CMOS processes the density of interface charge is lower than 10^{10} cm^{-2} which makes the Coulomb scattering with interface charge negligible in comparison with the Coulomb scattering with the channel dopants. For devices operating in weak or moderate inversion the mobility mismatch coefficient (A_μ) results inverse proportional to the square root of channel doping:

$$\mu_c = \frac{\mu_0}{L_{th} \cdot N_{ch}} \rightarrow A_\mu \propto \frac{1}{\sqrt{N_{ch}}} \qquad \textbf{(11)}$$

where μo is the unscreened mobility per scattering center per unit area. For channel doping above $10^{18}cm^{-3}$ the mobility mismatch coefficient in weak inversion becomes negligible ($A_\mu << A_L$, A_W) and the current factor mismatch is given solely by the channel edge roughness (L and W mismatches) and the T_{ox} fluctuation.

The Si/SiO_2 interface is not flat, but has irregularities of one or two atomic layers. At high effective electric field, when the channel carriers are heavily pushed towards the interface the mobility is significantly degraded due to scattering with surface asperities. The resulting surface-roughness scattering limited mobility (μ_{sr}) is independent of the channel doping and features a linear temperature dependence due to the temperature dependence of the carrier screening and of the Fermi level [9]:

$$\mu_{sr} = K_{sr} \cdot E_{eff}^{\ -n} \quad ; \quad K_{sr} \propto 1/(\Delta \cdot \Lambda)^2 \qquad \textbf{(12)}$$

with n=2 for electrons and n=1 for holes, where Δ is the rms value of the interface asperities and Λ is the correlation length. At room temperature the surface-roughness scattering becomes dominant at effective electric fields higher than 0.5MV/cm. For the actual deep-submicron devices the effective transverse field exceeds 1MV/cm even at few KT/q above the threshold voltage. Therefore the mobility of today's MOS devices operating in strong inversion is always surface-roughness limited.

With the scaling of MOS devices down to sub-100nm the non-local effects are becoming more and more important. For moderate submicron devices (>0.25µm) the carriers still drift in equilibrium with the semiconductor lattice and their velocity is limited by the saturation velocity. For deep-submicron devices (<0.15µm) as the longitudinal electric field increases, the carriers gas starts to be in disequilibrium with the lattice due to the insufficient number of phonon scattering events experienced by the carrier during the flight. As a result the carrier can be accelerated to velocities higher than the saturation velocity, approaching ballistic transport conditions. This velocity overshoot leads to an enhancement of the mobility mismatch.

In conclusion, in weak and moderate inversion the current factor mismatch is given by the device geometric dimensions variation ($A_\beta = f(A_L, A_W, A_{Tox})$), while in strong inversion the mismatch increases due to the enhancement of the surface-roughness limited mobility mismatch ($A_\beta = f(A_L, A_W, A_{Tox}, A_{\mu sr})$).

4. Model Implementation and Experimental Results

Fig.1 presents the dependencies between the matching coefficients and the process parameters that were used in the implementation of the proposed matching model. The threshold voltage mismatch is generated by introducing a global parameter with a Gaussian distribution ($\sigma = A_{VTO}/\sqrt{2}$), that is added to V_{TO} through an additive model parameter (e.g. DELVTO). The current factor mismatch is given by a second global parameter with Gaussian distribution ($\sigma = A_\beta/\sqrt{2}$) that changes the value of the device multiplication factor (M).

The proposed physically-based MOSFET matching model can be implemented in any circuit level simulator that supports an additive V_{TO} correction parameter and a device multiplication factor (SPICE, Spectre, Saber, etc).

Matching measurements were performed over several years using special matching test-chips with devices of various W and L sizes, on subsequent scaled-down deep-submicron CMOS technologies (0.35, 0.25, 0.18, 0.15, 0.13 and 0.1µm). Fig.2 shows the measured (solid line) and computed (symbols) threshold voltage matching coefficient for the NMOS and respectively PMOS transistors, along with the linear dependence on T_{ox}

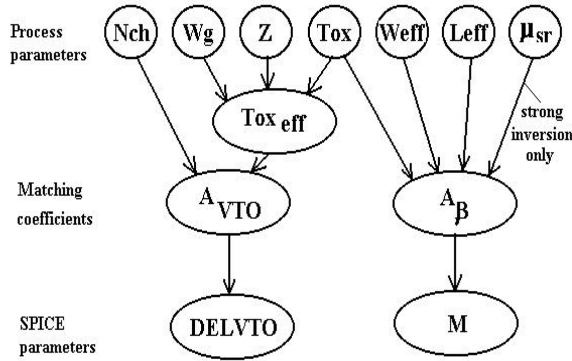

Fig.1 SPICE implementation of matching model

predicted by the existing matching models (A_{VTO} α $T_{ox}\cdot N_{ch}^{-1/4}$). It can be observed that for sub-0.25μ devices A_{VTO} looses its linear dependence on T_{ox}. This is due to the increase of the effective oxide thickness caused by gate depletion and inversion layer centroid. However, reploting A_{VTO} /$N_{ch}^{-1/4}$ as a function of T_{ox_eff}, it regains a linear dependence. The analytical model predicts within only few percent the experimental measured V_{TO} matching coefficient. The A_{VTO} degradation constitutes a major barrier for the usage of sub-0.1μ MOS devices in precision analog circuits. Also as expected, the PFETs have a higher V_{TO} mismatch due to a more pronounced gate depletion and also a higher channel doping. Furthermore the low-VT NFETs tend to have a better V_{TO} matching in comparison with the regular NFETs due to their lower channel doping (no threshold adjustment implant). Fig.3 gives the comparison of the experimental and computed strong inversion current factor matching coefficient (A_{β}) for the same CMOS processes. For moderate submicron processes the current factor matching coefficient decreases significantly due to the reduction of the oxide and interface charge, but going towards sub-100nm its value saturates due to the enhancement of surface roughness and limitations in the optical lithography.

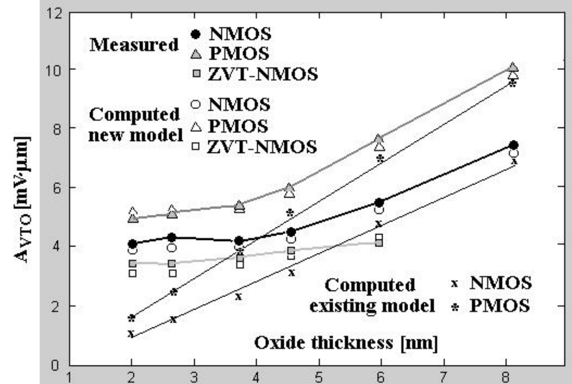

Fig.2 NMOS & PMOS devices A_{VTO} over process

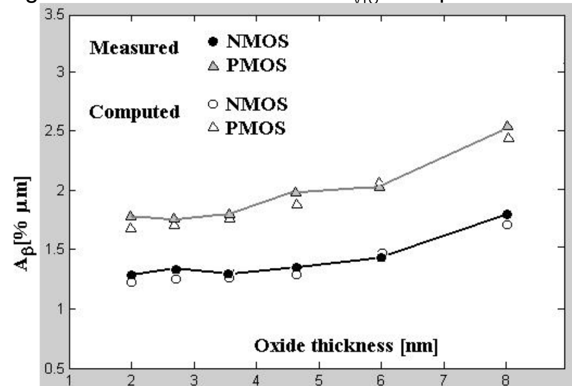

Fig.3 NMOS and PMOS devices A_{β} over process

5. Conclusions

A high accuracy physically-based MOSFET matching model was proposed, that considers the phenomena specific to the deep-submicron devices: channel random dopant fluctuation, gate depletion and quantum mechanical effects. Analytical expressions are provided for both the threshold voltage and current factor mismatch coefficients. Present model can be easily implemented in most existing circuit level simulators, independent of the level used to model the MOSFET. The proposed matching model was validated through measurements on several consecutive deep-submicron CMOS processes.

6. References

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