Substrate Bias Effect on Cycling Induced Performance Degradation of Flash EEPROMs

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Abstract

Cycling induced performance degradation of flash EEPROMs has been reported for $V_B=0$ and $V_B<0$ programming operation. Compared to $V_B=0$, $V_B<0$ programming shows lower interface degradation for identical cumulative charge fluence (for program) during repetitive program/erase cycling. Reduction in programming gate current has been found to be lower for $V_B<0$ operation under identical interface damage as the $V_B=0$ case. As a consequence, programming under $V_B<0$ condition has been found to cause lower degradation of programming time and programmed V_T due to cycling.

1. Introduction

Hot-carrier injection under negative substrate bias ($V_B<0$) is a more efficient programming scheme for flash EEPROMs (faster speed, lower power) compared to programming under $V_B=0$ condition. This scheme, also known as CHannel Initiated Secondary ELectron (CHISEL) mechanism (see Figure 1) has shown good endurance for device parameters up to 10^5 program/ erase cycles, leading to reliable operation of single cells and arrays [1-7]. However, it was recently shown by measurements on FET devices that $V_B<0$ operation causes enhanced device degradation when compared to the $V_B=0$ case [8]. Though it throws up some concern regarding the reliability of CHISEL programming operation, results from measurements on actual flash cells are still missing.

In this work, we perform a comparative study to explore the effect of $V_B=0$ (CHE) and $V_B<0$ (CHISEL) programming operation on cycling induced degradation of actual flash cells. We show by measurements on fully scaled $L_{FG}=0.22\mu m$ flash cells that apart from enhancement in programming speed, programming under $V_B<0$ causes (i) lower interface degradation for identical cumulative charge fluence (for program) during repetitive program/erase cycling and (ii) lower gate current reduction for identical interface degradation when compared to the $V_B=0$ case. This can be attributed to the higher energy of injecting electrons at $V_B<0$ due to impact ionization feedback. This also ensures reduced degradation in programming time and programmed V_T due to cycling when $V_B<0$ is used to program flash cells.

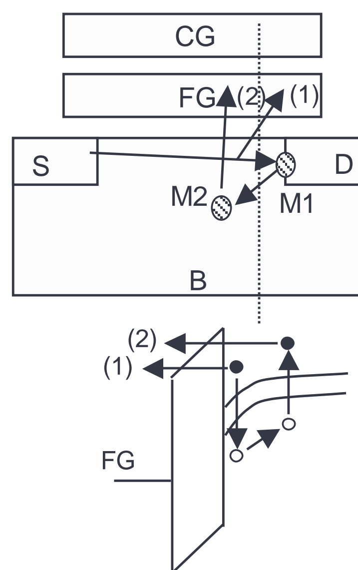

Figure 1. Hot-carrier injection under $V_B=0$ and $V_B<0$. Channel electrons heated by lateral field undergo impact ionization M1. Holes generated from M1 flow to the substrate and undergo further impact ionization M2, which is enhanced under high transverse field (negative V_B). The secondary electrons (CHISEL) generated from M2 traverse towards the interface and get injected into the oxide (2) with greater energies than the lateral field heated channel electrons (1).

2. Device fabrication

$W_{FG}=0.25\mu m$, $L_{FG}=0.22\mu m$ fully scaled flash cells were fabricated using a state-of-the art $0.18\mu m$ process involving STI and self-aligned source/drain contacts. The cells have area of $\sim 0.45\mu m^2$ with tunnel and inter poly oxide thickness of 12nm and 20nm respectively and a gate coupling of ~0.6.

3. Program/erase performance degradation

Figure 2 shows the programming transients measured under different program V_B values. The measured program times are 23µs, 9.8µs and 5.1µs respectively at $V_B=0$, –1 and –2V. Note that program speed increases by ~4X w.r.t $V_B=0$ when programming is done at $V_B=-2V$. This increase in programming speed has been attributed

to the increase in energy of electrons that get injected into FG as a result of impact ionization feedback mechanism at $V_B<0$ [1-7].

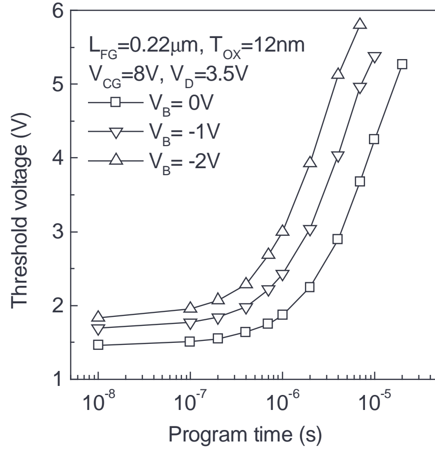

Figure 2. Programming transients as a function of V_B measured on a L_{FG}=0.22µm cell. Secondary electrons at $V_B<0$ cause enhanced I_G leading to faster programming for a given drain bias (V_D).

Figure 3 shows the degradation in program and erase transients measured before and after 10^5 program/erase cycles for programming at V_B=0 and V_B=–2V. It can be clearly seen that programming under $V_B<0$ causes much lower degradation in programming transients while the degradation in erase transient is slightly higher when compared to V_B=0 case.

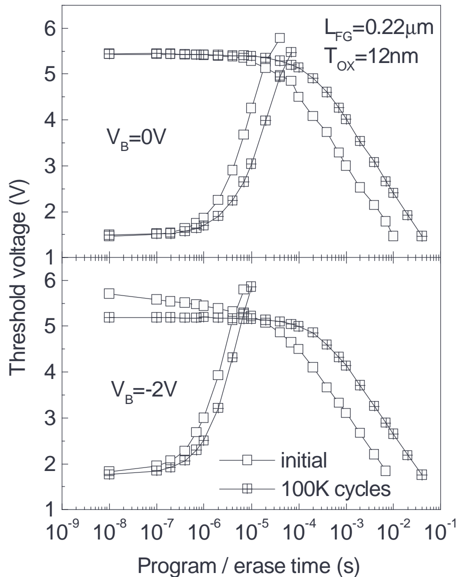

Figure 3. Program and erase transients of a L_{FG}= 0.22µm cell before and after 10^5 program/erase cycles measured under V_B=0 and $V_B<0$ programming condition. Program V_{CG}/V_D=8/3.5V, erase V_{CG} = –22V. Degradation in program transient is lower while that in erase transients is marginally higher when programming is done at $V_B<0$.

Figure 4 shows the programmed and erased V_T as a function of program/erase cycles. Programming at V_B=0 and –2V were performed using 23µs and 5.1µs pulses respectively, while channel erase was performed using a 6.6ms pulse. Programmed V_T remains almost constant up to 10^5 cycles for programming at $V_B<0$, while it starts degrading after 10^2 cycles and drops by ~1V for the V_B=0 case. Erased V_T for the V_B=0 case decreases near 10^2-10^3 cycles indicating hole trapping – which accounts for the slightly higher erased V_T degradation observed for the $V_B<0$ case. Figures 3 and 4 show consistent results, i.e. lower programming time and programmed V_T degradation with slightly higher erase time and erased V_T degradation for programming under $V_B<0$ condition. The program/erase time and programmed/ erase V_T degradation correlates well for all V_B values as shown in Figure 5.

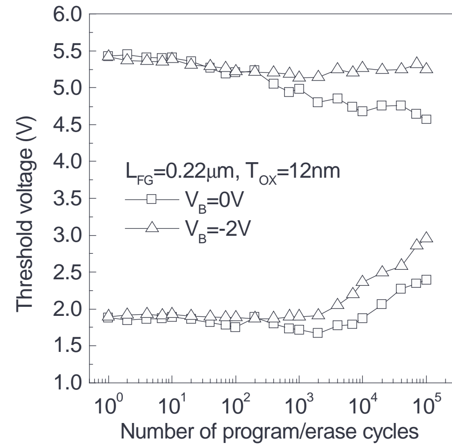

Figure 4. Program/erase V_T window closure due to cycling, measured on a L_{FG}=0.22µm cell under V_B=0 and $V_B<0$ programming condition. Program V_{CG}/V_D=8/3.5V, erase V_{CG}= –22V. Degradation in programmed V_T is lower while that in erased V_T is marginally higher when programming is done at $V_B<0$. Note hole trapping around 10^3 cycles from erased V_T for programming under V_B=0 condition.

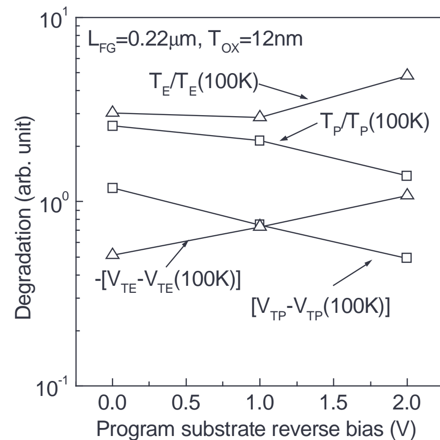

Figure 5. Correlation of program/erase time degradation with that of V_T degradation in programmed and erased state measured on a L_{FG}=0.22µm cell for programming under different V_B values. Program V_{CG}/V_D=8/3.5V, erase V_{CG}= –22V.

4. Interface degradation

Figures 6a to 6c show normalized transconductance degradation ($\Delta g_m/g_{m0}$) for programming under V_B=0 and V_B<0 conditions, measured as a function of (a) program/ erase cycles, (b) cumulative programming time and (c) cumulative electron fluence from substrate to FG during programming. Compared to V_B=0, g_m degradation for V_B<0 programming is lower for identical number of program/erase cycles (Figure 6a), though it is higher for identical cumulative programming time (Figure 6b). Note that the high energy electrons coming from M2 (see Figure 1) under V_B<0 condition cause enhancement in gate current (I_G) [1-7] but also cause more g_m degradation [8]. Therefore when compared for a fixed time, V_B<0 condition shows more g_m degradation. However, since I_G enhancement leading to faster program time is more dominant than the increase in g_m degradation, V_B<0 programming shows lower interface degradation when compared under identical number of program/erase cycles. Therefore, V_B<0 offers a more efficient hot-electron injection mechanism in terms of degradation to injection ratio. This is evident from Figure 6c, which shows lower g_m degradation under V_B<0 condition for identical cumulative electron fluence (as V_B=0) from substrate to FG during programming.

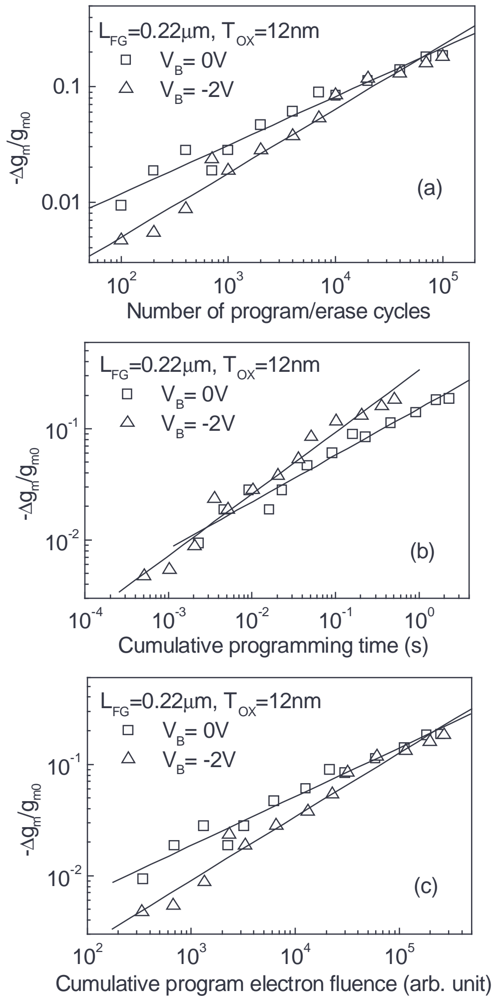

Figure 6. Transconductance degradation as a function of (a) number of program/erase cycles, (b) cumulative programming time and (c) cumulative electron fluence during programming. Measurements were done on a L_{FG}=0.22μm cell under V_B=0 and V_B<0 programming condition. Program V_{CG}/V_D=8/3.5V, erase V_{CG}= –22V.

5. Gate current degradation

Charges associated with interface defects act as a barrier to further charge injection and reduce I_G during programming, which cause degradation in programming performance. Figures 7a and 7b show gate current degradation for programming under V_B=0 and V_B<0 conditions, measured as a function of (a) program/ erase cycles and (b) cumulative g_m degradation with increase in repetitive program/erase cycling. The average gate current was measured from changes in V_T during programming.

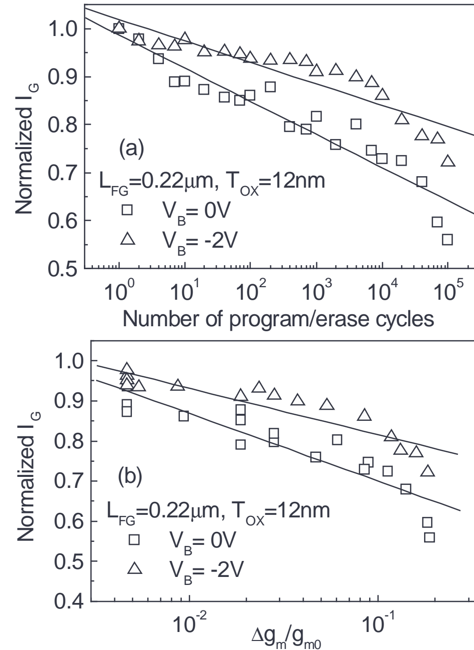

Figure 7. Normalized gate current degradation as a function of (a) number of program/erase cycles and (b) normalized transconductance degradation. Measurements were done on a L_{FG}=0.22μm cell under V_B=0 and V_B<0 programming condition. Program V_{CG}/V_D=8/3.5V, erase V_{CG}= –22V.

Compared to V_B=0, programming under V_B<0 shows reduced I_G degradation for identical number of program/ erase cycles (Figure 7a). This can be attributed to lower g_m degradation for V_B<0 programming (Figure 6a), and also to lower I_G degradation for a given g_m degradation as shown in Figure 7b. Compared to V_B=0, the lower I_G degradation due to cycling for V_B<0 is consistent with

lower degradation in programming transient and programmed V_T as shown in Figures 3 to 5.

The lower I_G degradation for a given g_m degradation for $V_B<0$ programming (Figure 7b) is explained as follows. Figure 8 shows the simulated Electron Energy Distribution (EED) at the interface and at the point of maximum electron injection of a L_{FG}=0.22μm device under V_B=0V (CHE) and –2V(CHISEL) operation. The EEDs were obtained using monte-carlo simulations on devices having structure and doping identical to the experimental flash cells.

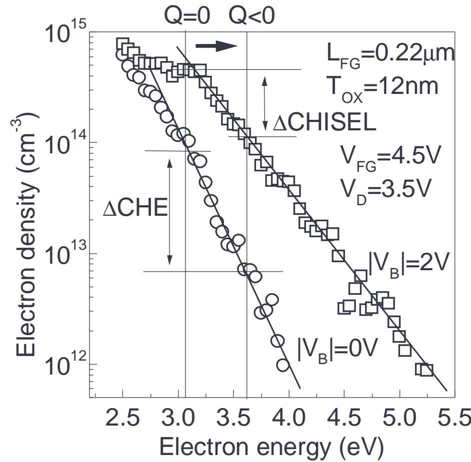

Figure 8. Simulated electron energy distribution in the channel of a L_{FG}=0.22μm device. The distribution was recorded at the interface and at the point of maximum electron injection into the gate. The barrier over which electrons are injected to the gate are approximately shown by vertical lines, before (Q=0) and after (Q<0) interface charge buildup due to cycling.

It can be seen that secondary impact ionization M2 (see Figure 1) populates the high-energy tail of EED under $V_B<0$ operation. The increase in potential barrier due to interface charge buildup (shown by vertical lines in the plot) reduces the electron density over the barrier by an amount Δ as shown. Since the energy distribution decays faster at high energies for V_B=0 as compared to $V_B<0$, ΔCHISEL < ΔCHE, and the degradation in I_G and hence programming time and programmed V_T are larger for V_B=0 as compared to $V_B<0$ programming operation.

6. Conclusions

To summarize, we have studied the effect of V_B=0 (CHE) and $V_B<0$ (CHISEL) programming operation on cycling induced performance degradation of flash cells. Using detailed measurements on fully scaled L_{FG}= 0.22μm flash cells we show that programming under $V_B<0$ causes lower interface degradation for identical cumulative charge fluence (for program) during repetitive program/erase cycling. Furthermore, due to the higher energy of injecting electrons coming from secondary impact ionization at $V_B<0$, gate current reduction with cycling is lower for identical interface degradation when compared to the V_B=0 case. This ensures reduced degradation in programming time and programmed V_T due to cycling (in addition to higher program speed) when $V_B<0$ is used to program flash cells.

References

[1] J. D. Bude, "Gate current by impact ionization feedback in sub-micron MOSFET technologies", in *Proc. Symp. VLSI Technology*, p.101, 1995.

[2] J. D. Bude, A. Frommer, M. R. Pinto and G. R. Weber, "EEPROM/flash sub-3.0V drain-source bias hot carrier writing", in IEDM Tech. Dig., p.989, 1995

[3] J. D. Bude et. al., "Secondary electron flash – A high performance low power flash technology for 0.35μm and below", in IEDM Tech. Dig., p.279, 1997

[4] J. D. Bude, M. R. Pinto and R. K. Smith, "Monte Carlo simulation of CHISEL flash memory cell", *IEEE Trans. Electron Devices*, vol.47, p.1873, Oct.2000.

[5] M. Mastrapasqua, "Low voltage flash memory by use of a substrate bias", Microelectron. Eng., vol.48, p.389, 1999.

[6] D. Esseni and L. Selmi, "A better understanding of substrate enhanced gate current in MOSFETs and flash cells – Part I: Phenomenological aspects", *IEEE Trans. Electron Devices*, vol.46, p.369, Feb.1999.

[7] L. Selmi and D. Esseni, "A better understanding of substrate enhanced gate current in MOSFETs and flash cells – Part II: Physical analysis", *IEEE Trans. Electron Devices*, vol.46, p.376, Feb.1999.

[8] F. Driussi, D. Esseni, L. Selmi and F. Piazza, "Substrate enhanced degradation of CMOS devices", in *IEDM Tech. Dig*., p.323, 2000.