Characteristics of Sub-100nm High-k Gate Dielectrics MOSFETs With Different Source/Drain Structure

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Abstract

The characteristics of a typical 70nm high K gate dielectrics MOSFET with different source/drain structure including S/D lift-up structure are simulated by two dimensional device simulator. The impact of FIBL effect the gate dielectric permikttivity increasing to the characteristics of MOSFET is investigated. The simulation results shows that the degradation of MOSFET characteristics can be suppress by change the structure of source/drain such as gate offset and S/D lift-up.

I. Introduction

The continuity scaling MOSFETs down to sub-100nm will face the challenges when SiO_2 is used as gate dielectric. The thickness of gate oxide in sub-100nm MOSFETs is below 1.5nm. The electrons can tunnel through the gate oxide easily, which cause the unacceptable standby power. An alternative solution is use high k dielectric materials [1]. However, the use of high K dielectric on MOSFET does not just simply increase the thickness of high K dielectric layer. The characteristics of MOSFETs with high K gate dielectrics need to study in details. Several simulations have been done to study the impact of high K gate dielectrics on deep sub-100nm MOSFETs. [2-4,6]. The 'fringing-induced barrier lowing' (FIBL) is used to describe the performance degradation of sub-100nm MOSFET with high K gate dielectric material [4]. However, most of them are focused on the influence of fringing electric field on the channel. The systematic study on the impacts of high K gate dielectrics on the whole MOSFET and comparison of the different MOSFET source/drain structure is rare. In this work, extensive simulations are carried out to study impact of high K gate dielectrics on the characteristics of a typical 70nm MOSFET with different source/drain structure including S/D lift-up structure. The key factors affecting the device characteristics are investigated.

II. Device structure and simulation method

The simulations are carried out with a two-dimensional device simulator ISE. The simulated structures are based on the typical 70 nm gate length nMOSFET with 1.5nm effective gate oxide proposed by ITRS [5]. The dielectric constant of the gate dielectric varies from 3.9 (SiO_2) to 200 ($BaSrTiO_3$). In order to keep the gate oxide capacitance C_{ox} as constant with the dielectric permittivity varying from 3.9 to 200, the thickness of high K gate dielectric is calculated by

$T_K = \frac{K \times T_{SiO_2}}{3.9}$. Where K is the permittivity of high K dielectric and T_{SiO2} is the equivalent thickness of SiO_2 that is fixed to 1.5nm during the simulations. The steep retrograde channel profile with a surface doping concentration of $3x10^{17}cm^{-3}$ and a peak concentration of $5x10^{18}cm^{-3}$ at a depth of 25nm is used. The source/drain extension and deep source/drain junction depths are 25nm and 80m respectively. The length of source/drain extension is 25nm. D_{sd} is the distance of gate and S/D extension overlap. D_{sd} is zero when there is no overlap, and D_{sd} is positive for the structure with gate overlap and is negative for gate and S/D offset. The structure of high K MOSFET is plotted in Fig.1. In the figure, Structure A is bulk MOSFET and Structure B is recess channel MOSFET with S/D region lift-up 80nm. SiO_2 sidewalls are used for both of the structures. During the simulation, the gate and S/D extension overlap D_{sd} changed from +15nm to –10nm.

III. Simulation Results and Discussion

The MOSFETs of Structure A with different D_{sd} are simulated and compared. Fig.2 and 3 show the impact of bulk high K gate dielectric MOSFETs with D_{sd} changed from 15nm to –10nm on current. From Fig.2 it can be seen that with K increasing the leakage current I_{off} becomes larger and this trend becomes more obvious for the MOSFET with gate and S/D overlap (D_{sd} positive). However, the turn on currents I_{on} change slightly with K increasing. From the figures, it also can be seen that leakage currents of MOSFETs are very sensitive to the structure of different S/D structure. The leakage current increases about two orders when D_{sd} changed from –10nm to 15nm but I_{on} just increases about triple.

Fig.4 plots the ratios of I_{on}/I_{off} for several of D_{sd} with different gate dielectric constant. With D_{sd} changing from negative to positive, the effective channel length decreases. Then both I_{on} and I_{off} increase, and I_{off} increases rapidly due to short channel effect. Thus the ratios of I_{on}/I_{off} decreases for D_{sd} changing from –10nm to 15nm. The ratio of I_{on}/I_{off} also decreases due to the fringing-induced barrier lowering (FIBL) effect [4] for MOSFETs with high k gate dielectric materials. From the figures it also can be seen that the FIBL effect has less influence for the structure of gate and S/D offset (D_{sd} negative) but becomes seriously for the structure of gate and S/D overlap (D_{sd} positive). Fig.5 plots the potential distribution along the channel of 70nm MOSFET with different gate dielectric constant (3.9 and 100) both for structure A with D_{sd}=-10nm and 10nm respectively. It reveals that the reason of the degradation in sub-micron MOSFET with high K gate dielectric can be described as fringing-induced barrier lowering (FIBL). From the figure, it can be seen that with K increasing the potential distribution in the channel decreases and the potential barriers of source and drain junction become lower while the potential distribution in the S/D extension region increases due to the fringing electric field. However, the details of the S/D structure can influence the distribution of potential and the effect of fringing electric field. From Fig.5 it can be seen that, for the structures with gate and S/D offset, there exists a potential discontinuity along the channel between the gate and S/D. This discontinuity can suppress the fringing electric field thus the potential distribution in the channel decreases slightly with K increasing. For the structure with gate and S/D overlap, FIBL effect becomes more serious due to the gate and S/D coupling. Then the characteristics of MOSFET with gate and S/D overlap are degraded more seriously with K increasing. This also can be seen in Fig 6 and 7, where the threshold and subthreshold swing of structure A with different D_{sd} are plotted.

Recess channel MOSFET with S/D region lift-up is a structure can solve the problem of ultra-shallow junction. Fig.8 show the threshold and subthreshold swing of structure B. The FIBL effect also can be suppressed by corner effect.

IV. Conclusion

The high K gate dielectric MOSFETs with different S/D structure including the structure with S/D lift-up are simulated by two-dimensional device simulator.

Due to the FIBL effect when the gate dielectric permikttivity increases the threshold voltage decrease while the leakage current and the subthreshold swing increase. However simulation results shows that the degradation can be suppress by change the structure of source/drain such as gate offset and S/D lift-up.

Reference

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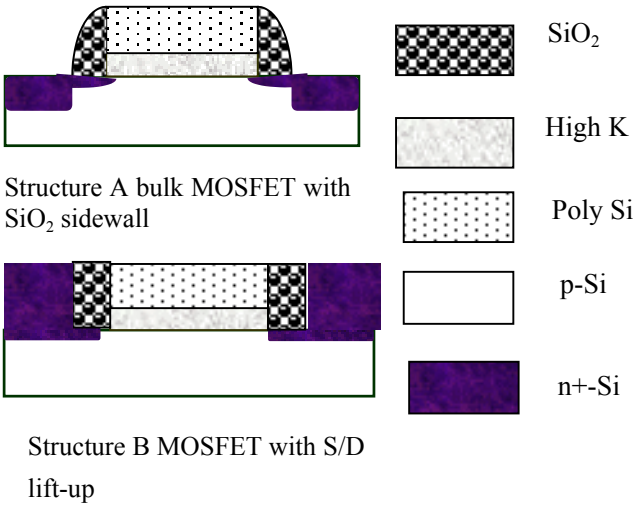

Fig.1 The structure of high K MOSFETs

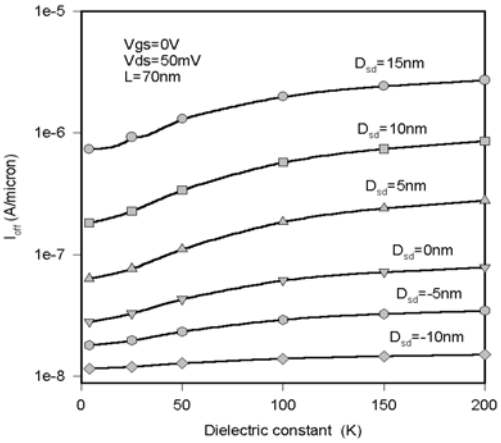

Fig.2 leakage current for MOSFETs with D_{sd} changed from 15nm to –10nm.

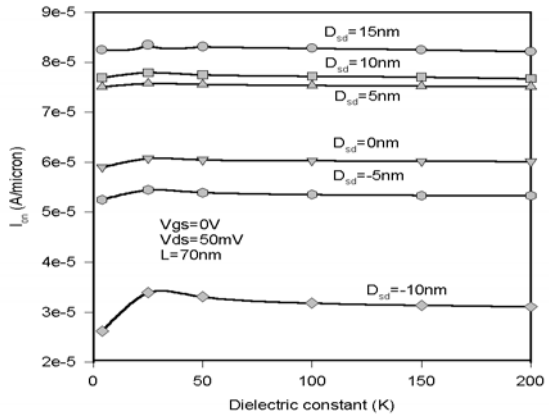

Fig. 3 I_{on} for high K gate dielectric MOSFETs with D_{sd} changed from 15nm to –10nm.

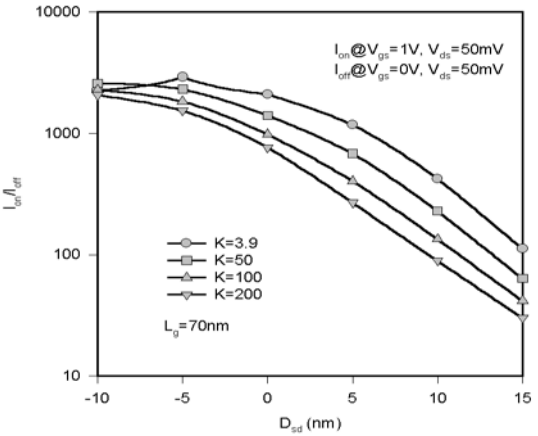

Fig.4 the ratios of I_{on}/I_{off} for several of D_{sd} with different gate dielectric constant.

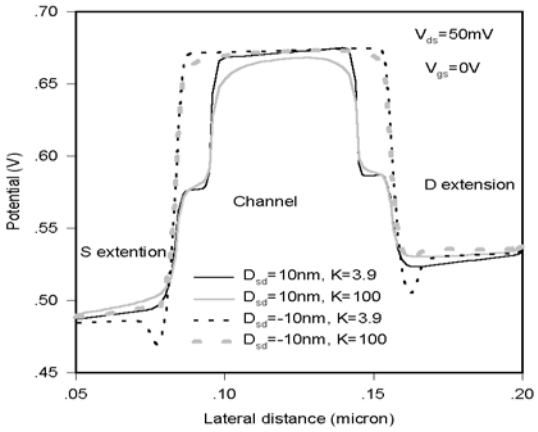

Fig.5 The potential distribution along the channel of structure A with D_{sd}=±10nm.

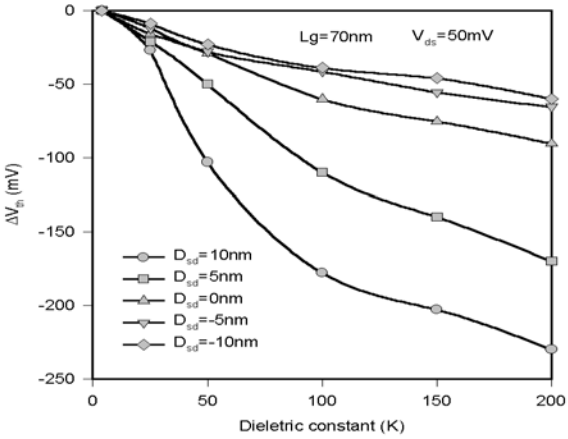

Fig 6 the threshold of structure A with different D_{sd}

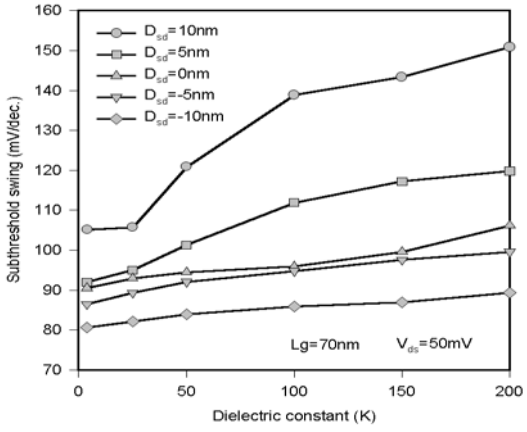

Fig7. the subthreshold swing of structure A with different D_{sd}

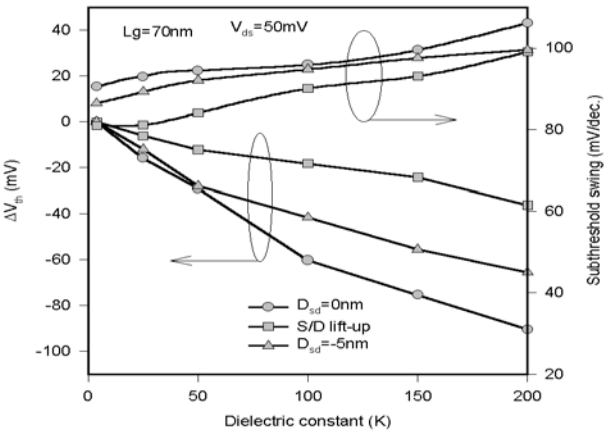

Fig.8 the threshold and subthreshold swing of structure B.