Improved Isolated RESURF Technology for a Multi Power BCD Process

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Abstract

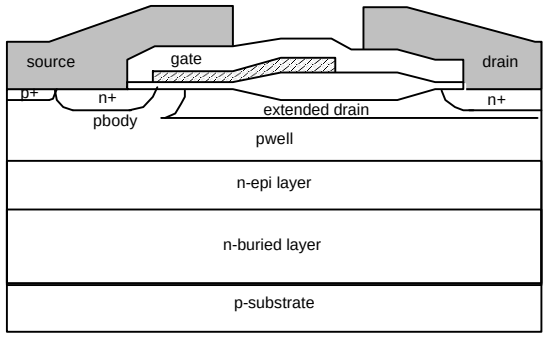
In order to reduce on state resistance of LDMOS transistor, it is necessary to use RESURF structure. However, conventional isolated RESURF structures cannot be used in a multi power BCD process because of the breakdown voltage dependence on epi thickness. Accordingly, we had to use non RESURF LDMOS transistor that has higher on state resistance than RESURF LDMOS transistor in a multi power BCD process. In this paper, we suggested a new isolated RESURF LDMOS structure whose breakdown voltage is independent of epi thickness, and applied this structure to the multi power BCD process that provides 5V CMOS, 20V vertical NPN transistor and 40V / 60V LDMOS transistors. Consequently, we could lower 34 ~ 49% on state resistance of the LDMOS transistors. This newly designed isolated RESURF LDMOS structure will be very useful for many multi power BCD processes

1. Introduction

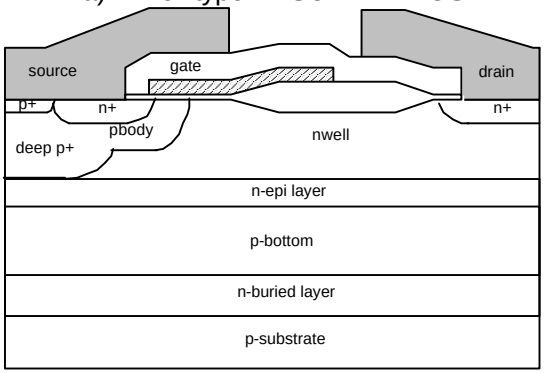
In the field of power integrated circuits much work has been done in the development of power transistors. Advancements were made enabling LDMOS power transistor to exhibit low on state resistance and high breakdown capability concurrently through a reduced surface field (RESURF) technology [1]. RESURF LDMOS transistors are utilized in high side driver applications and other applications that mandated electrical isolation between source and substrate by using isolated RESURF technology. However, this isolated RESURF technology cannot be used in a multi power BCD process providing CMOS, high performance vertical NPN transistor and multi power LDMOS transistors at the same time. This is because vertical NPN transistor and isolated RESURF LDMOS transistors require different epi thickness according to their breakdown voltage. Hence, we had to use non-RESURF LDMOS transistors whose on state resistance is higher than RESURF LDMOS in a multi power BCD process. In this paper, we suggest a new isolated RESURF structure whose breakdown voltage is independent of epi thickness, and apply this structure to the multi power BCD process that provides 5V CMOS, 20V vertical NPN transistor and 40V / 60V LDMOS transistors simultaneously. As a result, we could lower the on state resistance of the LDMOS transistors in the multi power BCD process.

2. Device Structures

In the beginning, we will examine the cross section of conventional isolated RESURF LDMOS transistors.



a) P-well type RESURF LDMOS



b) P-bottom type RESURF LDMOS

Figure 1. Conventional Isolated RESURF LDMOS Transistors

In case of p-well type LDMOS (fig 1a), avalanche breakdown is occurred under the drain n+ region. Therefore, it is necessary to optimise epi thickness, extended drain / pwell doping concentration and pwell junction depth according to the target breakdown

voltage. P-bottom type LDMOS (fig. 1b) case, breakdown is occurred at the surface if the epi thickness is not optimised. This is because surface electric field of the LDMOS transistor can be reduced only in the optimised epi thickness and nwell / pbottom doping concentration. After all, epi thickness of the conventional isolated RESURF LDMOS transistors should be different according to their breakdown voltage. In addition to these LDMOS transistors, vertical NPN transistor also requires optimised epi thickness according to the breakdown voltage. However, a multi power BCD process provides vertical NPN transistor and LDMOS transistors having different breakdown voltage at the same time. Hence, conventional isolated LDMOS transistors cannot be used in a multi power BCD process.

Now, we will examine the cross section of the proposed isolated RESURF LDMOS transistor (fig. 2). Since the electric field concentration under the drain n+ region is eliminated by using nwell below drain region, we could control the breakdown voltage of the LDMOS only with extended drain / pwell doping concentration and pwell length. Accordingly, this proposed isolated RESURF LDMOS transistor can be used in the multi power BCD process.

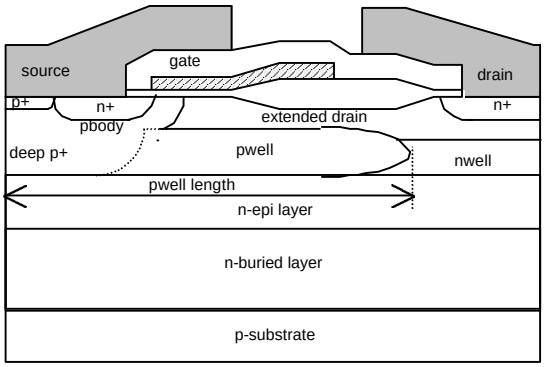
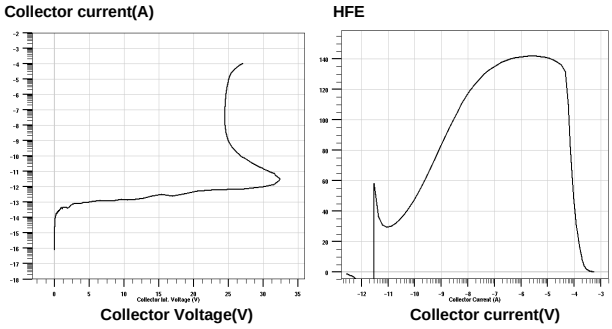


Figure 2. Proposed Isolated RESURF LDMOS Transistors

3. Device Simulations

3.1. Vertical NPN transistor

In order to develop the multi power BCD process that provides 5V CMOS, 20V vertical NPN transistor and 40V / 60V LDMOS transistors by using proposed isolated RESURF technology, vertical NPN transistor should be optimised in the first place. This is because vertical NPN transistor determines the epi thickness. Figure 3 and table 1 show the electrical characteristics of the optimised 20V vertical NPN transistor. In order to obtain these characteristics, it is necessary to use 6.2um epi thickness. Thus, we must use this epi thickness to provide 20V vertical NPN transistor.



a) BVceo Curve b) HFE Curve

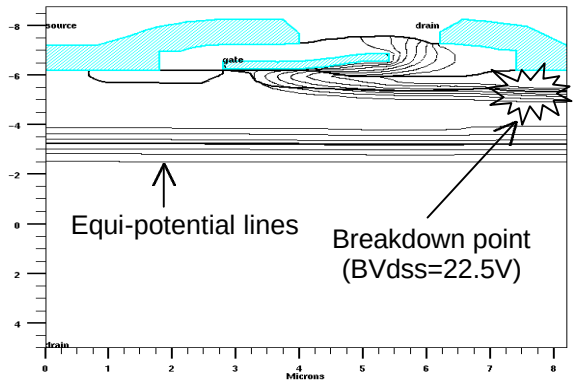
Figure 3. BVceo & HFE Curve of vertical NPN tr.

Table 1. Electrical Characteristics of NPN tr.

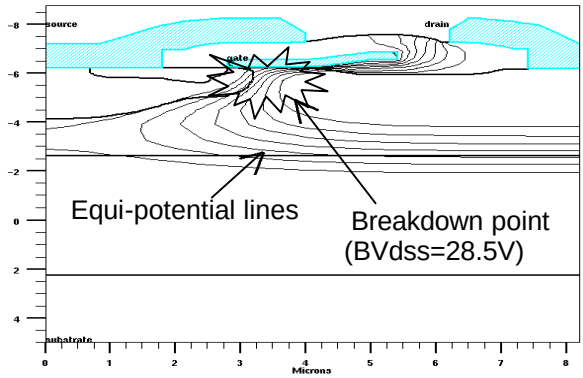
Parameter	BVceo	HFE
Value	25V	140

3.2. Low On Resistance LDMOS transistors

It is necessary to use 6.2um epi thickness to provide the 20V vertical NPN transistor. However, we cannot use conventional isolated RESURF structures as we mentioned previously. Figure 4 shows the equi-potential line and breakdown voltage of conventional isolated RESURF LDMOS transistors in that epi thickness.



a) Pwell type isolated RESURF LDMOS



b) Pbottom type isolated RESURF LDMOS

Figure 4. Equi-potential line and breakdown voltage

As can be seen in the figures, we cannot obtain 40V and 60V breakdown voltage with conventional isolated RESURF structures in 6.2um epi thickness. Pwell type needs higher epi thickness and p-bottom type needs lower epi thickness than 6.2um to get higher breakdown voltage.

Now, we will examine the proposed isolated RESURF LDMOS structure. The breakdown voltage of the RESURF LDMOS transistor is different according to pwell length. As shown in figure 5, its breakdown voltage is increased in the longer pwell length. Thus, we could make 40V and 60V RESURF LDMOS with different pwell length.

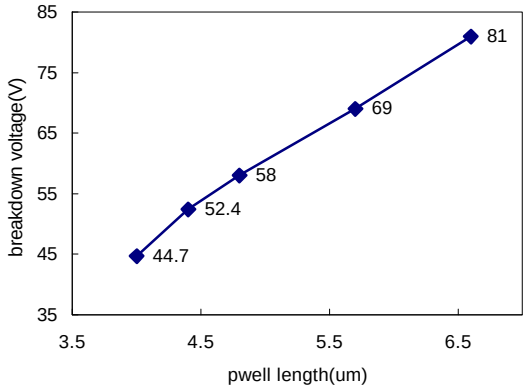
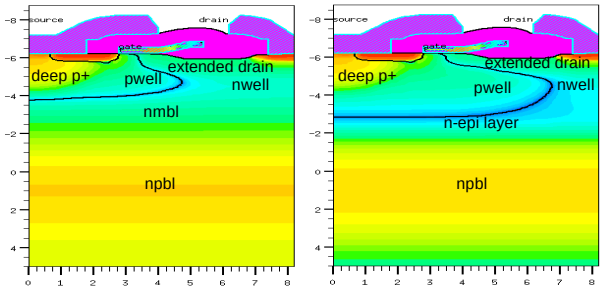


Figure 5. Breakdown voltage VS. Pwell length

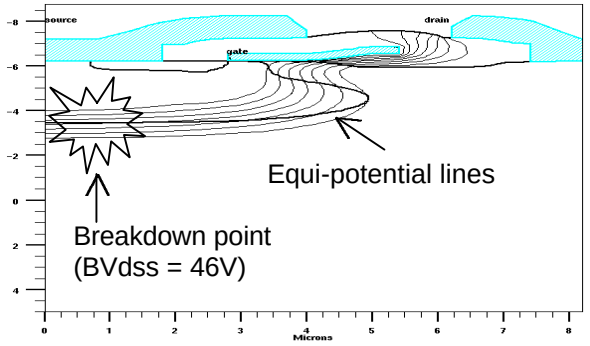
Figure 6 shows the cross section of the 40V and 60V RESURF LDMOS transistors. In addition to npbl, nmbl is used in the 40V LDMOS in order to prevent surface breakdown.



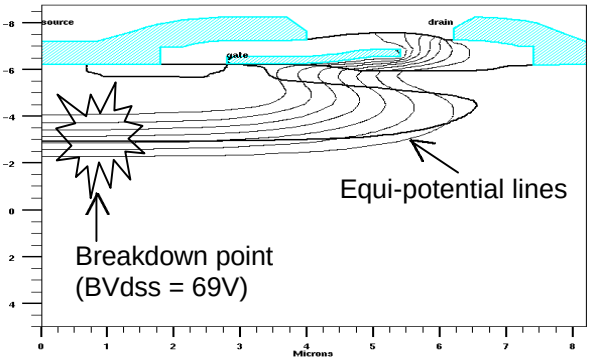
a) 40V LDMOS b) 60V LDMOS

Figure 6. Cross section of 40V & 60V LDMOS

Figure 7 shows the equi-potential line and breakdown voltage and figure 8 shows the breakdown current flow line of the proposed 40V / 60V isolated RESURF LDMOS transistors in 6.2um epi thickness. As can be seen in the figures, their surface electric field is well reduced and breakdown occurs vertically.

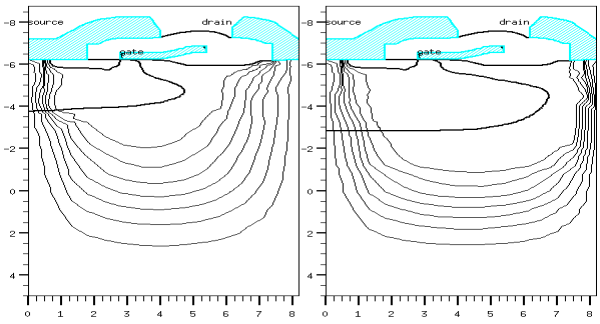


a) 40V RESURF LDMOS



b) 60V RESURF LDMOS

Figure 7. Equi-potential line and breakdown voltage of 40V & 60V LDMOS.



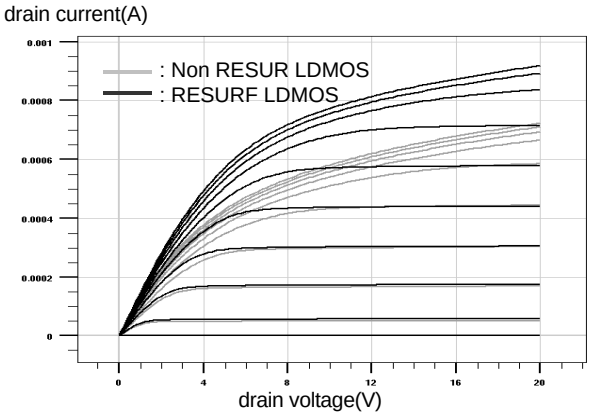
a) 40V LDMOS b) 60V LDMOS

Figure 8. Breakdown current flow line

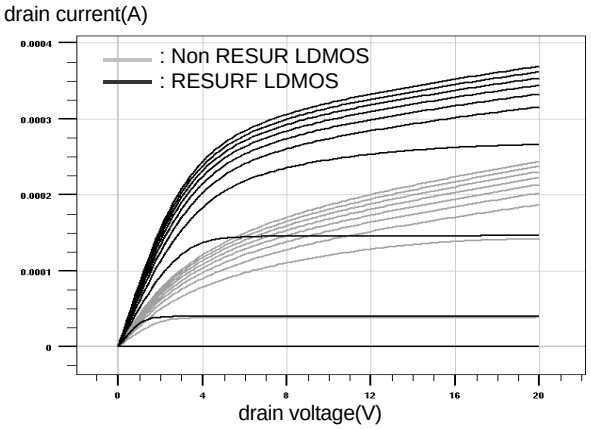
4. Comparison of non-RESURF LDMOS and proposed RESURF LDMOS

Figure 9 shows the drain current versus drain voltage curve for 40V / 60V non-RESURF and proposed RESURF LDMOS transistors, and table 2 shows the electrical characteristics. As shown in the figure and table, 40V RESURF LDMOS has 34% lower on state resistance and 60V RESURF LDMOS has 49% lower on state resistance than non RESURF LDMOS. Since the influence of drain resistance upon the on state resistance is increased in the higher voltage LDMOS,

on state resistance difference between RESURF and non-RESURF LDMOS is increased in 60V LDMOS.



a) 40V LDMOS transistor



b) 60V LDMOS transistor

Figure 9. Drain current versus drain voltage curve

Table 2. Electrical Characteristics of non-RESURF and proposed RESURF LDMOS

Parameter	Non-RESURF LDMOS		Proposed RESURF LDMOS	
	40V	60V	40V	60V
Threshold Voltage(V)	1.7		1.7	
On State Resistance (mohm/cm^2)	0.82	2.41	0.58	1.21
Breakdown Voltage(V)	49	72	46	69

5. Conclusion

Since the surface electric field of the conventional isolated RESURF LDMOS transistors can be reduced only in the optimised epi thickness, we could not use RESURF structure in a multi power BCD process that provides CMOS, high performance vertical NPN transistor and LDMOS transistors having different breakdown voltage. In this paper, we suggested new isolated RESURF LDMOS structure whose breakdown voltage is independent of epi thickness, and applied this structure to the multi power BCD process that provides 5V CMOS, high performance 20V vertical NPN transistor and 40V / 60V LDMOS transistors. Consequently, we could reduce 34 ~ 49% on state resistance of the LDMOS transistors.

Generally, we used non RESURF LDMOS structure in a multi power BCD process because of the dependence of LDMOS's breakdown voltage upon the epi thickness. However, we can use RESURF LDMOS structure that has lower on state resistance than non RESURF LDMOS structure now by using the newly designed isolated RESURF technology. This new technology will be very useful for many multi power BCD processes.

6. References

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