**A New Latch-Up Free Complementary Bipolar Process Using PBSOI Technique**


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**Abstract**

In this paper, for the first time, we suggest a novel high voltage, high speed and latch-up free NPN transistor and PNP transistor fabrication technology using PBSOI (Patterned and Bonded Silicon On Insulator) and STI (Shallow Trench Isolation) technology. Using this technique, we can easily control the breakdown voltage ($BV_{CEO}$) without the problem of P+B/L out-diffusion. In this PBSOI process, after long-time diffusion of well (collector), the Buried Layer is diffused on the well.

In addition, unlike the prior technology that devices are fabricated in epitaxial layer, the proposed devices are formed in active wafer itself, therefore we can get defect-free devices promising excellent characteristics. The peak $fT$s for NPN and PNP transistor are 10GHz and 9GHz, the values of $BV_{CEO}$ for the NPN and PNP devices are 15V and 17V, respectively. Finally, these values were found to be excellent results as shown in the maximum value of Johnson-limit for the $fT$-$BV_{CEO}$ product.

**Introduction**

Complementary silicon bipolar process has been extensively used in high performance applications, and high voltage complementary bipolar process is used for a lot of high speed amplifier applications in current market trend. Especially, in these amplifier applications, PNP device must be satisfied with characteristics such as high operating voltage for output stage driver and high $fT$ for fast AC signal path. Since $BV_{CEO}$ and $fT$ have a trade-off relationship, the higher the $BV_{CEO}$, the higher $fT$ is more difficult to get.

Furthermore, it is more difficult to get higher $fT$ in PNP transistor than in NPN transistor, due to lower hole mobility in silicon. Generally, the biggest weak point in complementary bipolar process is latch-up due to parasitic transistor action generated from vertical PNP transistor, therefore SOI substrate isolation is very useful for preventing the latch-up.

Nevertheless, in conventional SOI structure [1,2], it is difficult to secure effective p-collector area for high breakdown voltage unlike NPN transistor. In case of PNP transistor, boron source is used for the P+B/L (Buried Layer) and in case of NPN transistor, arsenic source is used for N+B/L which play a role in collector current path. Owing to the diffusivity difference between arsenic and boron source, we can’t control effective collector (flat well region).

In order to solve all described problems, we have optimized this process using PBSOI (Patterned and Bonded Silicon On Insulator), STI (Shallow Trench Isolation) and Trench Isolation technique.

**Proposed Structure and Process Procedure**

In terms of vertical PNP transistor, a novel process to fabricate high speed and voltage complementary bipolar process is described. Figure1 (a) to (e) show how to make PBSOI wafer. As shown in figure1 (a), the low concentrated active wafer is used to make easily p-well and n-well simultaneously. There are no problems whether the active wafer is p-type or n-type. First of all, after the P-well is implanted and diffused for a long time, the P+B/L is implanted and diffused on the P-well for a short time. And after trench etching for the device isolation and thermal oxidation, the poly-silicon is fully deposited to fill trenched region. In figure1 (b), poly-silicon CMP process (chemical and mechanical polishing) is performed to be able to bond to handle wafer. In this step, it is important to get a flat poly surface profile for easy bonding throughout the whole wafer area (Top, Center, Bottom, Left, Right). If not so, after bonding is processed, the voids are generated in BPSG interface between poly-silicon and handle wafer.

Figure3 shows measured poly thickness after poly CMP process. Figure4 presents SEM image of bonded wafer showing the void and BPSG bubble at bonded interface in figure3 case. The voids were disappeared after controlling CMP parameters. Fig.5 indicates the measured poly-silicon thickness after optimizing poly-silicon CMP parameters. In figure3 and figure5, it can be recognized that the thickness uniformity of poly-silicon is different between two case of CMP profiles.
After the CMP process, BPSG layer is deposited on polished poly and reflowed at nitrogen ambient 1000°C. It is very important to control boron and phosphorus concentration for BPSG layer. As shown in figure4, we can see the bubble due to thermal precipitation after the bonding. But the critical boron or phosphorus concentration not to make bubble due to precipitation is dependent on annealing temperature and time. And then, the handling wafer to operate next steps is bonded on the re-flowed BPSG layer.

Figure 1(c) Back-Side Grinding and Selective CMP using oxide Polishing Etch Stopper

Figure 2. Final schematic cross-section of a PNP transistor using PBSOI

Figure 3. Measured poly-silicon thickness after poly CMP process

Figure 4. SEM image of bonded wafer showing the void at bonded interface due to the poor polysilicon CMP process

Figure 5. Measured poly-silicon thickness after optimizing poly-silicon CMP parameters.

Figure 6. SEM image of bonded wafer showing no void at bonded interface due to the good poly-silicon CMP process

Figure 7. SEM image of completed active wafer using PBSOI technique (for vertical PNP transistor’s P-well region)
Figure 6 represents the SEM image of void free bonded wafer at bonded interface in realized process. And as shown in figure 1(c), we have to up side down the completed bonding wafer. And then the active wafer is fabricated after roughly backside grinding and selective CMP processes. In this step, the oxide of trenched region is used for the stopper of selective etch and photo-auto align key for the next process step. The obtained active wafer is used as the epitaxy region to operate actual devices in conventional SOI process. The SEM image of completed active wafer using PBSOI technique in case of vertical PNP transistor’s P-well region is shown in figure 7. The consecutive processes are the same as conventional complementary bipolar process. To implant with the reverse type is the only different point. Fig. 2 shows final schematic cross-section of vertical PNP transistor with double poly structure. And the NPN transistor was also fabricated with the same sequences for vertical PNP transistor as explained.

The details of the PBSOI (Patterned and Bonded Silicon On Insulator) were found in [3].

Simulation Results and Experimental Results
The realized active wafer, where complementary bipolar devices will be transplanted, using PBSOI technique is shown in figure 7.

Figure 9. \( f_T (GHz) \) vs. \( I_c (A) \) of VPNP transistor (\( A_e=1.0 \times 4.0 \))
(a) simulation result (b) experimental result

Figure 10. \( Bv_{CEO}(V) \) vs. \( I_c (A) \) of VPNP transistor (\( A_e=1.0 \times 4.0 \))
(a) simulation result (b) experimental result
As using this technique (PBSOI), we can more easily control breakdown voltage than the normal epitaxy process. Because the remained active thickness can be controlled (depend on) by trench depth for device isolation and the effective well (collector) region can be secured without out-diffusion of Buried Layer. In advance, preliminary test for outlook of device’s characteristics using normal epitaxial growth was performed before we realize the devices using this prepared wafer. The simulation and experimental results are shown in figure8 through figure11 and table1. The schematic one and two-dimensional doping profiles are shown in Figure11 for extracting electrical parameter by simulation. The simulation and experimental results are represented in figure8, 9, and figure10, respectively. The (a) and the (b) of each figures represent simulation and experimental results, respectively.

Table1 shows electrical characteristics of valid devices in real experimental test. As shown in the figures and table, the current gain of NPN and PNP transistors were 120 and 70, respectively yielding beta-Early voltage products of 7200 and 2100, respectively. The collector-emitter breakdown voltages are 15V and 17V for the NPN and PNP devices, respectively.

The peak $f_T$ for the NPN is about 10GHz (see table1) while the peak $f_T$ for the PNP is about 9GHz as shown in Figure6 at a current density of about 100μA/μm$^2$. These are excellent results which show the maximum value in Johnson-limit for the $f_T$-$B_{vceo}$ product [4]. The other significant parameters for valid devices are summarized in Table1.

The whole process combined the prepared active wafer with devices realized in preliminary test is processing now. The experimental results will be presented at the conference.

**Summary**

This process using PBSOI technique will be created to serve the next generation of high frequency analog markets (Band Width : more than 500MHz) and is an advanced, complementary, dielectrically isolated bipolar technology. It has an advantage that the breakdown voltage ($B_{vceo}$) can be easily controlled by well designed trench depth as well as no out-diffusion of Buried Layers (B/L).

**References**


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Table1. Electrical Characteristics of Valid Devices (experiment values)

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<td>V</td>
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<td>V</td>
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<td>9</td>
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Figure11. One and Two-dimensional doping profiles and structure of a VPNP transistor by Silvaco simulator