# The characteristics of leakage current mechanisms and SILC effects of $Al_2O_3$ gate dielectric

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ABSTRACT

**Electrical properties, current transport mechanism, and stress induced leakage current (SILC) effect of $Al_2O_3$ gate dielectric thin films deposited by reactive dc magnetron sputtering were studied. The results show that annealing in $O_2$ ambient can effectively reduce the oxygen vacancy in $Al_2O_3$ films but may not result in additional interfacial layer form at $Al_2O_3$/Si interface. In the fresh devices there exist few interfacial traps at $Al_2O_3$/Si interface. However, negative gate bias stress can cause the generation of new interfacial traps at $Al_2O_3$/Si interface.**

## I. INTRODUCTION

When CMOS technology scales into 100nm node, below 1.5nm $SiO_2$ is required to maintain high device performances. However, such an ultra thin $SiO_2$ will cause the unacceptable gate leakage currents and reliability due to significant direct tunneling effect and high electrical field effect. High K gate dielectrics such as $Al_2O_3$ [1-3], $HfO_2$ [4], $ZrO_2$ [5], $La_2O_3$ [3], and $TiO_2$ [6] have been extensively studied to replace $SiO_2$. Among of them, $Al_2O_3$ is a promising candidate due to its high thermal stability, large band gap and large band-offset with Si. Ultra-thin $Al_2O_3$ gate dielectric films and MOSFET with $Al_2O_3$ gate dielectric have been demonstrated [1,2]. However, there are few studies on the transport mechanisms of $Al_2O_3$ gate leakage current up to now. Understanding the leakage current transport mechanisms of gate dielectrics is very important since we can extract the information such as material properties and reliability characteristics from it. In this paper, the electrical properties, the leakage current characteristics of $Al_2O_3$ gate dielectric films and the impacts of process and voltage stress were studied. By comparing the electric field dependence behaviors of gate leakage currents with different carrier transport mechanisms, the characteristics of interfacial traps at $Al_2O_3$/Si interface were obtained.

## II. EXPERIMENTAL

$Al_2O_3$ gate dielectric thin films were deposited on Si substrates by reactive dc magnetron sputtering at room temperature in $Ar+O_2$ ambient. The Si substrates were pre-treated by a HF-last cleaning process then were loaded immediately in the deposition chamber. During sputtering $Ar/O_2$ rate was 2:1, total pressure of $Ar+O_2$ mixture gas was $8.5\times10^{-7}$ Torr, power was 200W, and sputtering time was 2 minutes. The $Al_2O_3$ films of the samples were deposited simultaneously. The samples were then furnace annealed in different conditions, where S1, S2 and S3 were annealed in $N_2$ ambient for 2 minutes at 400ºC, 600ºC and 800ºC, respectively, and S4 was annealed firstly at 500ºC in $O_2$ ambient for 10 minutes then annealed at 850ºC in $N_2$ ambient for 2 minutes. Keithley 590 CV analyzer and HP4156B parameter analyzer were used to

measure capacitance-voltage (C-V) and current-voltage (I-V) curves.

## III. RESULTS AND DISCUSSION

High frequency C-V curves of the samples were firstly measured at 1MHz as shown in Fig. 1. We can find that the accumulation capacitance increases with increasing annealed temperature and the largest accumulation capacitance is in sample S4 where an annealing step in $O_2$ ambient was introduced. Such results suggest that the dielectric constants of $Al_2O_3$ gate dielectric films increase with increasing annealing temperature, and the annealing step in $O_2$ ambient will not cause the formation of an additional interfacial layer at $Al_2O_3$/Si interface due to the thermodynamic stability of $Al_2O_3$ on silicon.

Figure 2 shows I-V curves of the capacitor samples. Gate bias was swept from –3V to +3V for fresh devices. Ionic conduction behaviors (leakage current hysteresis effect)[7] were observed in the samples S1, S2 and S3 but the ionic conduction behavior disappeared in S4. Meanwhile, leakage current of S4 drops. So we can deduce reasonably the oxygen vacancy in $Al_2O_3$ films is responsible for the ionic conduction behaviors in samples S1, S2 and S3, and annealing in oxygen ambient can reduce the density of oxygen vacancy in $Al_2O_3$ films.

Various conduction mechanisms were proposed to account for the carrier transport behaviors in insulating dielectric thin films, which show different electric field and temperature dependences [7]. In this study, Fowler-Nordheim tunneling (FN), Schottky emission (SK), and Frenkel-Poole emission (FP) mechanisms were applied to characterize the leakage current behaviors of $Al_2O_3$ gate dielectric films. The results indicate that the FN mechanism could not characterize the leakage current behaviors whether for gate injection or substrate injection due to the negative slope in the curves of $ln(I/V^2)$ versus $V^{-1}$; the SK mechanism could fit the behaviors for both gate injection and substrate injection as shown in Figs.3 and 4; and the FP mechanism could characterize the behaviors for gate injection as shown in Fig. 5 but failed to characterize it for substrate injection where a negative slope of $ln(I/V)$ versus $V^{1/2}$ curves is observed as shown in Fig.6. As we know well, the FN mechanism is associated with tunneling effect, the SK mechanism is associated with the thermionic emission across the metal-insulator interface or the insulator-semiconductor interface, and FP is due to field-enhanced thermal excitation of trapped electrons into the conduction band [7]. Thus, above results indicate that the transport mechanism of tunneling effect is negligible and the thermionic emission mechanisms (including SK and FP) dominate the leakage current transport of $Al_2O_3$ gate dielectric films in the samples. Meanwhile, the interfacial traps are responsible for the FP mechanism, and there are few traps at the $Al_2O_3$/Si interface but a great deal of traps exist at the metal/insulator ($Al/Al_2O_3$) interface. The traps at $Al/Al_2O_3$ interface may be originated from the contamination of lift off process.

The stress-induced leakage current (SILC) effect of $Al_2O_3$ gate dielectric was studied. –10V gate injection voltage stress was applied. Significant SILC effects were observed in the samples (S1, S2, S3, and S4). Fig.7 shows the SILC effect of S4 for substrate injection. Generally, SILC effects are associated with the generation of new traps in dielectric films or at interface during the stress. Fig.8 shows the electric field dependent behaviors of S3 and S4 after negative gate voltage stress. FP mechanism can fit them. Compared with Fig.6, the result of Fig.8 suggests that significant increase of gate leakage current in substrate injection case is due to the generation of new traps at $Al_2O_3$/Si interface under the stress.

## IV. CONCLUSION

$Al_2O_3$ gate dielectric thin films were deposited by reactive dc magnetron sputtering and post-anneal process. The results indicate that annealing in oxygen ambient may not cause the formation of an additional interfacial oxide layer but can reduce the oxygen vacancy of $Al_2O_3$ films. The results also show that the interfacial traps at $Al/Al_2O_3$ interface and $Al_2O_3/Si$ interface are responsible for FP mechanism, and there are few interfacial traps formed at $Al_2O_3/Si$ interface during deposition but negative gate bias stress causes the generation of new interfacial traps at $Al_2O_3/Si$ interface.

## ACKNOWLEDGEMENTS

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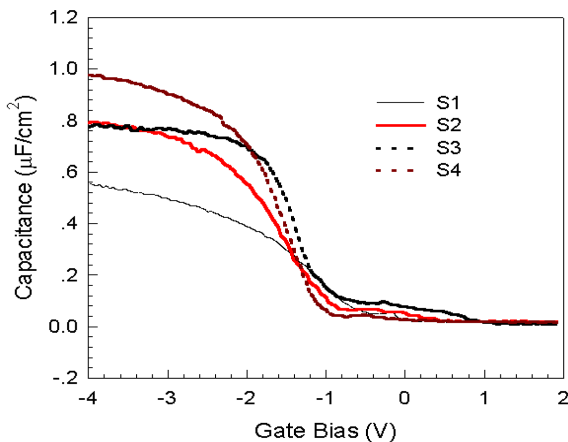



Fig. 1 High frequency C-V curves of the samples (S1, S2, S3, and S4) measured at 1MHz, where S1, S2, and S3 were annealed in $N_2$ ambient at 400°C, 600°C and 800°C.

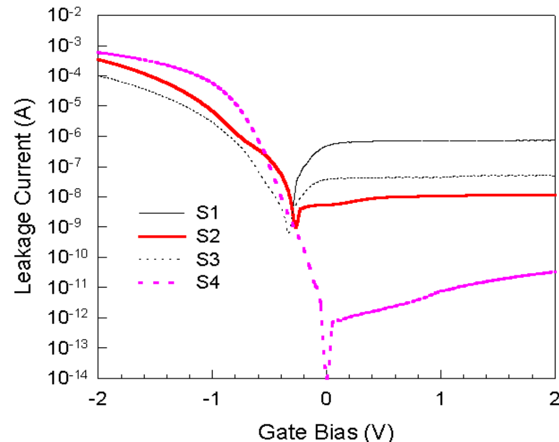
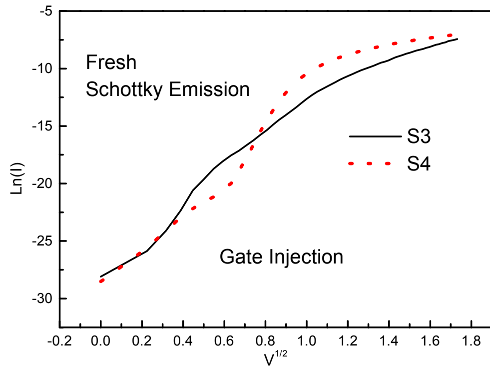



Figure 2 I-V curves of the samples (S1, S2, S3, and S4), where S4 was firstly annealed at 500°C in $O_2$ ambient then annealed at 850°C in $N_2$ ambient. Gate bias was swept from –3V to +3V.



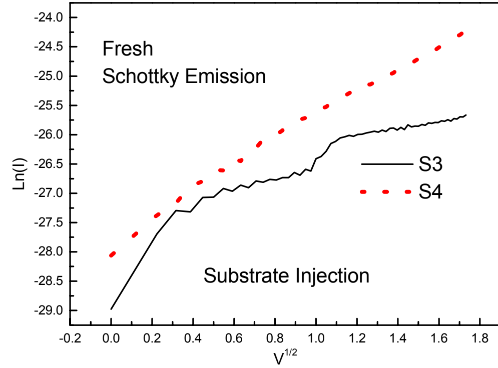
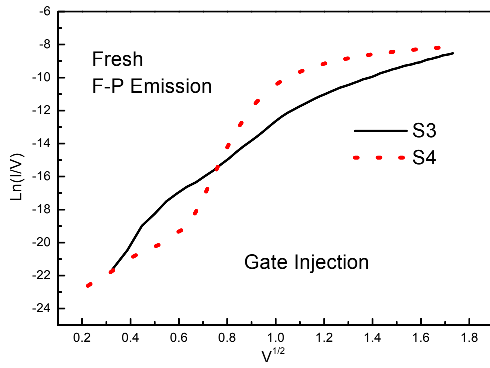




Fig.3 The electric field dependence of the leakage currents of S3 and S4 (fresh devices) based on SK mechanism for gate injection.

Fig.4 The electric field dependence of the leakage currents of S3 and S4 (fresh devices) based on SK mechanism for substrate injection.



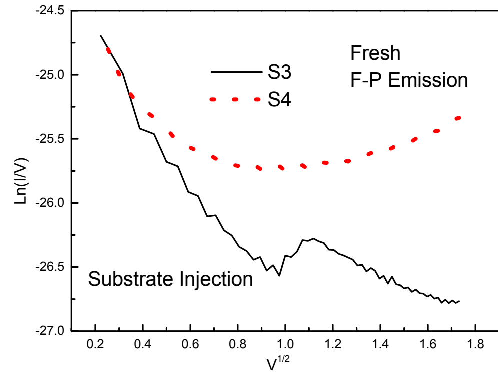
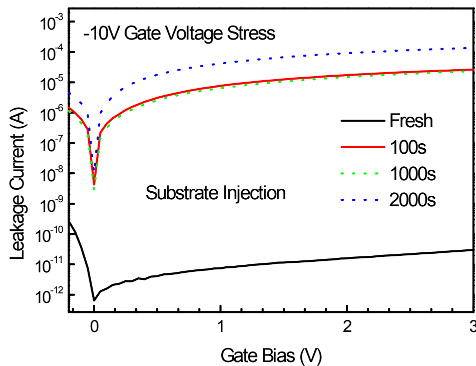




Fig.5 The electric field dependence of the leakage currents of S3 and S4 (fresh devices) based on FP mechanism for gate injection.

Fig.6 The electric field dependence of the leakage currents of S3 and S4 (fresh devices) based on FP mechanism for substrate injection.



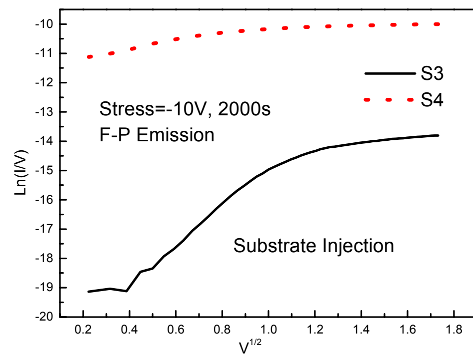




Fig.7 The electric field dependence of the leakage currents of S3 and S4 (fresh devices) based on FP mechanism for substrate injection.

Fig.8 The electric field dependence of the leakage currents of S3 and S4 (fresh devices) based on FP mechanism for substrate injection.