A Simple and Accurate HSPICE Compatible Gate Leakage Macro Model

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Abstract

A simple and accurate gate leakage macro model that is compatible with HSPICE circuit simulator is presented. This model accurately predicts gate leakage of capacitors in accumulation and inversion and corrects for the gate-leakage induced errors in transistors under different operating conditions. This model is based on a universal gate leakage curve from accumulation to inversion. Simulations of inverters, ring oscillators and current mirrors using this model are presented. It is shown that the tunneling leakage component of off-state current can lead to significant increase in power consumption and noticeable degradation in current mirror performance for typical ASIC applications. This indicates that circuit simulators with accurate gate leakage models are essential for 90 nm node designs.

1. Introduction

Leakage from ultra-thin gate oxides (< 16 Å) used in the 90 nm node constitutes a considerable fraction of the transistor off-state [1] leakage current. Modelling and accounting for this leakage current has attracted considerable attention in the recent years [2]-[7]. Recently, version 4 of the BSIM extraction model that includes gate leakage with explicit source and drain partitioning was introduced by [3]. This approach models gate leakage, based on [2], as an exponential function of the form \( A(1-e^{-Bv}) \), where \( A \) and \( B \) are extracted constants. The source and drain partitioning of gate current is further studied by [4], in which they pointed out that the exponential form of the gate leakage current listed in [2] and [3] is accurate only in the weak tunnelling regime. They presented a more rigorous physical model, requiring numerical solution, of gate leakage. They also showed that, for weak tunnelling regimes, their model reduced to the same exponential equation as listed by [2] and [3]. Another approach to modelling gate leakage was presented in [5] and expanded in [6]-[8], where the gate leakage currents were modelled as several current sources using the behavioural model option of SPICE.

In this paper, we present an empirical HSPICE compatible macro-model that accurately models capacitors (in accumulation and inversion) and transistor gate leakages, for 90 nm node devices, under all operating conditions. The leakage currents from the gate to each of the three other nodes are modelled as voltage controlled current sources (VCCS), dependent only on the difference in the potential between the gate and that node.

2. Capacitor Measurements

N and P channel capacitors (30 µm X 30 µm) were used to understand the different components of the gate leakage current. The relatively small sized capacitor was used to avoid any effect of parasitic resistances on the measurements. Gate, source/drain (S/D) and substrate currents were measured under different drain and substrate bias conditions. Fig. 1(a) shows gate currents for different drain biases. Fig. 1(b) shows the same data plotted against the gate to drain potential, \( V_{gd} \). For the gate bias ranging from accumulation to inversion, all curves simply sit on top of each other. This allows for the generation of a universal gate leakage curve vs. \( V_{gd} \) as shown in Fig. 1(b). Fig. 1(c) indicates that gate current is a very weak function of substrate bias. Indeed, when the individual drain and substrate current were analyzed, as shown in Fig. 2, the following was noticed: In accumulation, roughly equal amounts of gate current flows into the drain/source and substrate terminals. However, in inversion, almost all the gate current (ratio > 10^5) flows into the S/D nodes. Identical observations were made for P-type capacitors. Figures 1(a)-(c) show that the gate current, as pointed out by [4], is indeed not an exponential function of voltage and therefore, using an exponential fit to estimate gate current as suggested by [2] and [3] would lead to substantial errors in gate current estimation at high \( V_{gd} \) values.
3. Description of Macro Model

The observed behavior of capacitor's gate, S/D and substrate currents suggest that each of these currents can be modeled simply as voltage dependent current sources (VCCS), dependent only on the relative potential of that node to gate. A schematic of this macro-model is shown in Fig. 3, where each VCCS is modeled as a polynomial function of the potential difference over the entire range of operation. The S/D and substrate currents are modeled as polynomials and the results for the capacitor at $V_d=0$ and $V_{sub}=0$ are shown in Fig. 2. The total gate leakage is then reported as the sum of the currents flowing into the substrate and S/D nodes. This approach is similar to that proposed by [5]-[6], but differs from them in independently resolving gate current components to S/D and substrate. Therefore, this approach accurately models the gate current from accumulation to inversion. However, the proposed empirical model does not attempt to explicitly consider the interaction between source and drain components, instead treating them as independent of each other and only dependent on the gate to source/drain potentials respectively. This is a reasonably good assumption since in the region of most interest, i.e., $V_g=0$, $V_s=0$, $V_d=1V$ and $V_g=1V$, $V_s=0$, $V_d=1V$, the currents are indeed independent of each other. The third condition, any value of $V_g$ and $V_s = V_d$, is identical to the

Fig. 1 (a) Gate Leakage under different drain biases for a 30X30 μm², N Type 16 Å capacitor. (b) Same data plotted vs. $V_{sub} = V_g-V_s$, all plots lie on top of each other. A combined $I_g$ vs. $V_g$ plot is also shown, and (c) $I_g$ vs. $V_g$ for different substrate voltages, it is seen that gate leakage is a weak function of substrate bias.

![Fig. 1](image1.png)

![Fig. 2](image2.png)

![Fig. 3](image3.png)
capacitor case that was employed to create the model in the first place. These assumptions allow us to greatly simplify the macro-model to use just three current sources, in contrast to [8] which could result in > 40 voltage and current sources to accurately resolve all aspects of the equations presented in [5]-[6]. This approach puts minimal run-time overhead and is being used to analyze complex circuitry for the 90 nm node.

Excellent match between the model and measured gate current was observed, shown for \( V_{dd} = 1 \text{ V} \) and gate dielectric thickness is 16 A for both cases.

4. Studies of Simple Circuits

The macro-model presented in the previous section was used to study the DC and AC behavior of some common circuits and compared with results obtained from a standard BSIM3V3 model. The simulation results for a simple inverter \((W_p=2 \mu m, W_n=1 \mu m, L=0.1 \mu m)\) are
shown in Fig. 5a. The transfer characteristic was unchanged between the two cases, however, the current drawn from the power source increased for low input voltages and the estimated gate leakage current is shown in Fig. 5a. However, as the fan-out increases, degradation in voltage transfer characteristics was observed.

Next, a ring oscillator with varying number of inverter stages were simulated and the ring speed and dynamic power consumption was noted. While the predicted speed for single fan-out ring oscillator did not change significantly, there was a definite increase in the predicted power consumption with the gate leakage model. Fig. 5b shows the % difference between the two cases vs. the number of stages in the ring oscillator. The discrepancy between the two cases increases linearly with the number of stages in the ring. While a ring oscillator is an extreme case since it is always on, it should be noted that considerable error in power consumption estimation could arise if gate leakage is ignored.

Another interesting and potentially more serious effect of gate leakage is felt on the operation of current mirrors. The current mirror circuit in Fig. 6 will provide an output current \( N \) times the drain current of transistor \( M_0 \) i.e. \( I_{out} = N \times I_{in} \). Without gate leakage, \( I_{out} = N \times I_{in} \). However, with leakage the mirrored current \( I_{out} = N \times (I_{in} - I_{gleak}) \). The discrepancy that arises from not modeling the off state leakage accurately will be most enhanced in current-mode Digital to Analog Converters where several binary weighted current sources are switched on and off based on the digital input leading to a steady degradation of mirroring ability as seen in Fig. 6.

5. Conclusions

An accurate and simple HSPICE compatible macro-model of gate leakage is presented. A universal gate leakage curve is used to model gate leakage as a function of gate to S/D/Sub potential. This model accurately predicts both transistor and capacitor gate leakage and its drain/source and substrate components. Simulations of inverter, ring oscillators and current mirrors are presented. Results indicate that ignoring gate leakage can result in a substantial error in power consumption estimation and errors in current mirror operation.

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References

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