Investigation of HFO_2 dielectric stacks deposited by ALD with a mercury probe

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Abstract

In this paper, a mercury probe is used to characterize electrically HfO_2 dielectric stacks. Its effectiveness and limitations are first investigated through C-V measurements analysis. Particularly, an new analytic electrical model is proposed to explain the frequency-dependence of C-V characteristics not only due to classical series resistance effects. An application to the study of different HfO_2 films is finally presented. It reveals, on as-deposited high-k oxides, the presence of a moderated-k interfacial layer, which composition can change after post-deposition anneals. The stretch out of C-V curves due to polysilicon deposition and doping activation annealing is also reported .

1. Introduction

In order to replace SiO_2 as a gate dielectric in future sub-0.1µm devices, the high-K material HfO_2 is extensively investigated [1-2]. On the technological point of view, to achieve the integration of this new material, its main electrical properties must be rapidly known to enable an efficient optimization of process parameters related to the deposition operation or post-deposition annealing. To perform such electrical measurements at the front-end level, the use of a mercury probe [3-4] can be an attractive solution since the main oxide parameters can be directly characterized without any gate material patterning. Such an opportunity is particularly interesting for high-K materials where the elaboration and the etching of gate electrode also constitute additional critical issues [1].

After describing the experiment of this study, efficiency and limitations of this equipment are presented. Then the influence of several process parameters on the electrical behaviour of hafnium oxide is analyzed from measurements performed with a mercury probe.

2. Experiment

In this study, p-type wafers are processed without any lithography operation. A first cleaning treatment leads to the formation of a native oxide, on which hafnium oxide HfO_2 is deposited by atomic layer deposition ALD. Various post-deposition anneals, at 600°C and 800°C, can then be performed on different as-deposited samples in nitrogen ambient and a few ppm of O_2. To investigate the impact of polysilicon gate on HfO_2 dielectric stacks, in-situ n+-doped polysilicon has been deposited on some HfO_2 layers, annealed and finally removed by a wet etching operation. The different wafers are then characterized electrically by a mercury probe.

3. Efficiency and limitations of the mercury probe

As the gate of the studied capacitors is obtained directly by the contact of a mercury dot with the dielectric stack, the quality of this electrode must be well-controlled to perform reliable measurements. Figure 1 shows C-V characteristics dispersion obtained on 3.5 nm SiO_2 oxide (between each C-V measurement, the Hg/High-K contact is removed and formed again). Since the maximum deviation is limited to 2% in accumulation regime, the oxide thickness maximum error can be estimated to 0.7Å on a 3.5 nm oxide. The dispersion is larger in a depletion region due to small variations of the mercury work function. Nevertheless, the maximum error of 2.10^{11} cm^{-2} for the fixed charges remains acceptable.

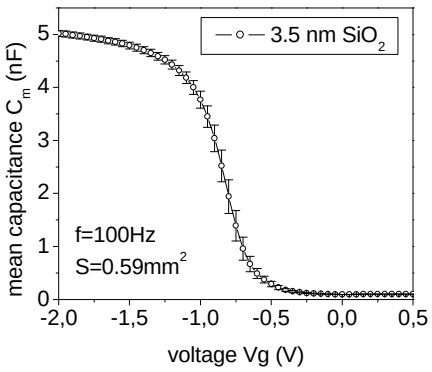

Figure 1. Mean capacitance C_m and standard deviation versus gate voltage obtained with nine C-V characteristics.

On figure 2, a C-V measurement has been performed on a 3.5 nm ALD HfO_2 oxide. The measured capacitance C_m in accumulation regime is strongly frequency-

dependent. Usually, this phenomenon is attributed to series resistance effects [5] but here, as illustrated in figure 3, such a classical electrical model cannot explain the frequency dependence of both capacitance and conductance. Consequently, a new model must be proposed where the interface between Hg and the dielectric is modelled as a leaky oxide with its own resistivity and thickness.

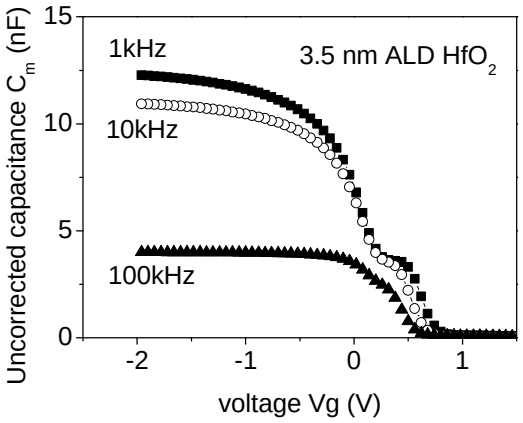

Figure 2. Frequency dependence of the measured C-V characteristics.

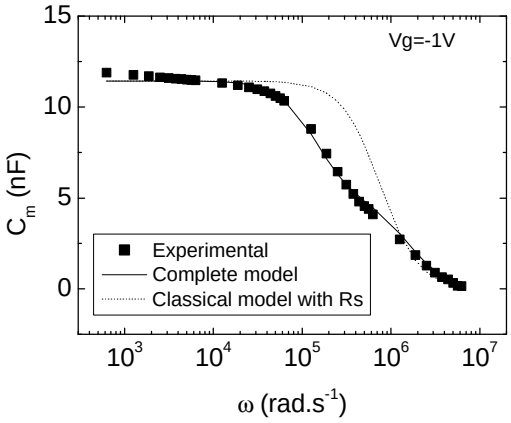

Figure 3. Measured capacitance C_m versus ω compared with classical and new complete models.

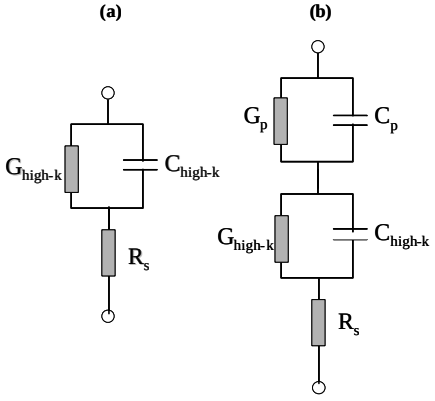

Figure 4. (a) Classical electrical scheme (b) Complete model with an interfacial layer

The classical electrical model for C-V frequency dependence, shown on figure 4 (a), which assumes a resistance Rs in series with the impedance of the dielectric stack (C_{High-K},G_{High-K}) is not sufficient here . An impedance (Gp,Cp) must be added to model the interfacial layer leading to the scheme of the figure 4 (b). Assuming an equivalent SiO_2 oxide thickness for this parasitic film of 1.6nm and a conductance Gp=3.8mS , the dependence can be correctly simulated as shown on figure 3. A methodology to easily extract Rs, Cp, Gp is given in [3]. The raw data of figure 2, obtained on a 3.5 nm HfO_2 deposited on a 0.7 nm native oxide, can then be corrected leading to the C-V characteristics of figure 5. C-V curves are all superposed at the different frequencies in the accumulation region illustrating the effectiveness of such a model. The EOT (ie Equivalent silicon Oxide Thickness) extracted with a C-V quantum simulator is here 1.3 nm.

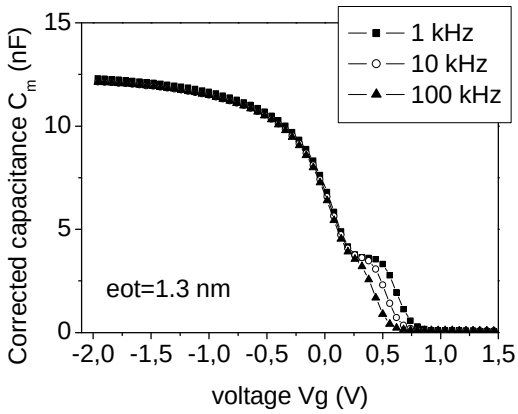

Figure 5. Corrected C-V characteristics obtained on an as-deposited 3.5 nm HfO_2 oxide.

The quality of the Silicon/HfO_2 interface can then be analyzed through the characterization of the interface states. Their energy profile over silicon bandgap can be extracted either by capacitance method [6] or by conductance method [7] (G(V)/ω characteristics are reported in the inset of figure 8). The two techniques leads to the same interface states density shown on figure 6. The density of interface traps Dit which is rather high on this as-deposited sample can be significantly reduced by further post-deposition anneals.

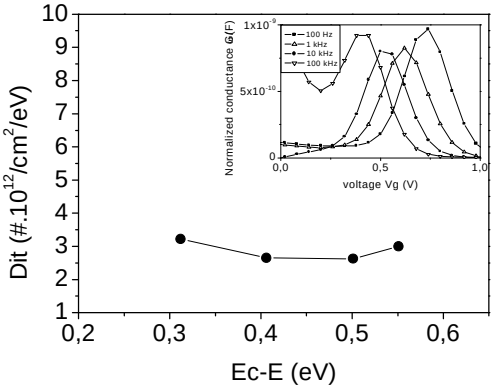

Figure 6. Energy profile of interface traps extracted from G(V) method. Inset: conductance peaks G(V)/ω.

4. Application to HfO_2 dielectric stacks study

4.1. Nature of the interfacial oxide

The nature and quality of native oxide can impact the main electrical properties of the dielectric stack in term of EOT, interface states and fixed charges. In figure 7, the EOT is plotted versus the physical HfO_2 deposition thickness. The linear dependence of the data obtained for three physical thicknesses allows an extraction of the dielectric constant as well as the interfacial layer thickness. The dielectric constant of this hafnium oxide can be estimated to 22.1 in the range of values already reported in the literature [2]. The interfacial oxide thickness $e_{interfacial}$, evaluated to 0.67 nm, seems to remain unchanged after the HfO_2 deposition (it was estimated by an ellipsometry measurement at 0.7 nm before the HfO_2 deposition). Actually, the physical thickness of this thin film is higher (≈1.2nm) as shown on figure 8 which represents a TEM cross-sectional image of the amorphous 5.0nm HfO_2 dielectric stack. Therefore, this result suggests that the ALD hafnium oxide deposition partially transforms pure SiO_x oxide into a interfacial layer with a dielectric constant of 7. This result well-agrees with similar studies performed on ZrO_2 films [8],[9].

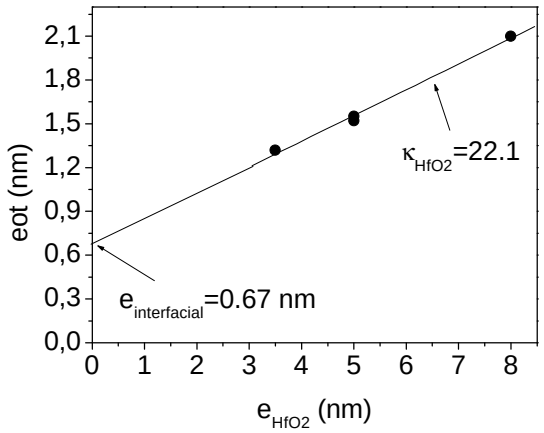

Figure 7. EOT versus HfO_2 physical thickness

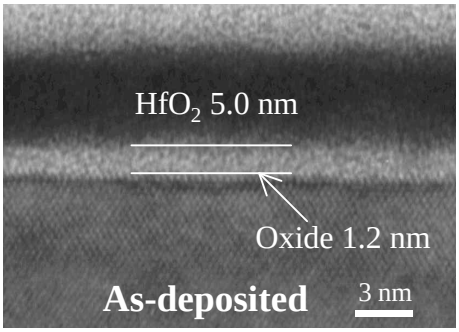

Figure 8. High-resolution cross-sectional TEM image of an as-deposited p-Si/SiO_x/HfO_2

4.2. Influence of post-deposition anneals

The effects of two different N_2 post-deposition anneals on electrical behavior of HfO_2 dielectric stacks has been investigated. Figure 9 shows that post-deposition anneals mainly favor a rising of the interfacial layer electrical thickness, from 0.67nm for as-deposited samples, respectively, to 0.91 nm and 1.43 nm for 600°C and 800°C annealed stacks. For the highest temperature annealing, we can also notice that the extracted electrical value is consistent with the physical thickness measured on the HRTEM picture of figure 10. This result suggests that the 800°C anneal enables the re-growth of a pure SiO_2 layer from the moderated-κ interfacial oxide of as-deposited films without significantly modifying its thickness. Furthermore these HfO_2 stacks stabilized by the 800°C annealing do not seem to be very sensitive, in term of EOT, to the polysilicon deposition and doping activation anneal since there is no significant difference in figure 9 between data obtained with the mercury probe and those obtained on patterned polysilicon gate capacitors with the same process.

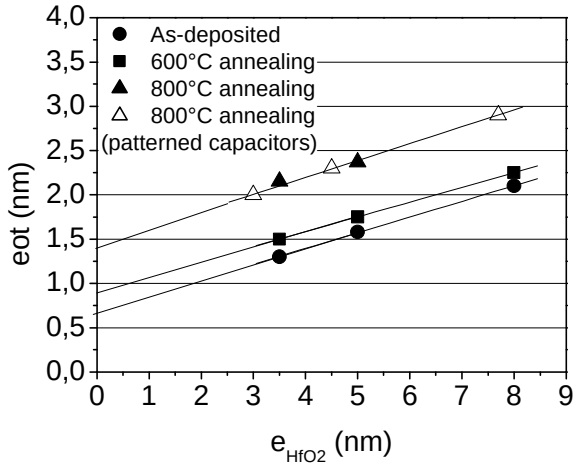

Figure 9. EOT versus physical thickness of HfO_2 e_{HfO2} for as-deposited and annealed high-k stacks.

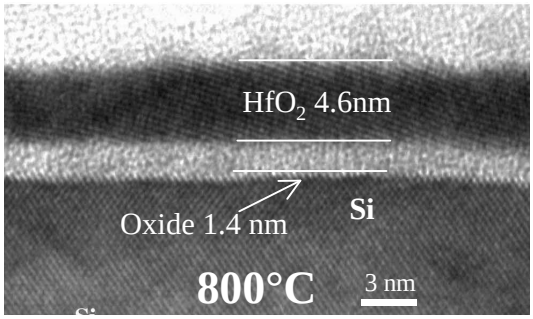

Figure 10. High-resolution cross-sectional TEM image of an 800°C annealed p-Si/SiO_x/HfO_2

4.3. Influence of Polysilicon deposition and activation annealing

The influence of the polysilicon deposition and doping activation annealing on the electrical characteristics of HfO_2 oxide has also been studied. On

an initial 0.7 nm native oxide with a 5.0 nm HfO_2 oxide without any deposition annealing, an in-situ n+-doped polysilicon material has been deposited and activated. After removing the polysilicon by wet etching, the wafer has been characterized by Hg probe. Figure 11 shows the results of this experiment through three C-V characteristics obtained on As-deposited and treated samples. For the doping activation, a 750°C and 950°C RTP anneals are compared. After the polySi deposition, the C-V curve seems to be stretched out. This phenomenon, which has already been reported by [10], cannot only be explained here by a large density of interface traps.

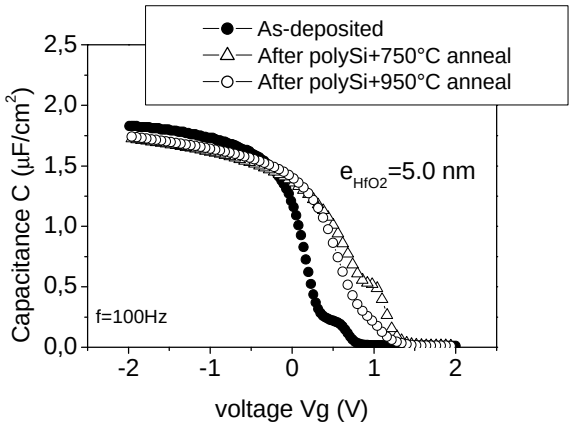

Figure 11. C-V characteristics before and after polySi deposition and doping activation annealing

The polysilicon deposition generates fixed negative charges in the oxide, as it can be seen in figure 11. The stretch out of the C-V curve may actually be due to the clustering of fixed charges [6], chapter 6. If the surface distribution of fixed charges is no longer gaussian over the capacitor area, a large dispersion of local flat band voltage Vfb may appear, leading to this stretching effect. Such an analysis is confirmed by a HRTEM observation on a similar dielectric stack on which the interfacial layer seems to be no longer homogenous. Especially, its thickness is reduced locally from 1.2 nm to 0.7 nm due to presence of non-uniformities. On patterned wafers, we have demonstrated that the stretch out effect is significantly reduced by post-deposition anneals.

5. Conclusion

In summary, the effectiveness of mercury probe to quickly evaluate the main electrical properties of high-k dielectrics has been demonstrated. Good accuracy has been obtained thanks to a good repeatability and a new efficient model for the impedance correction. With this model, a complete electrical characterization of high-κ films can be performed without any limitation down to at least 1.3 nm high-k EOT. With this mercury probe we demonstrate that an interfacial layer is formed between silicon and HfO_2 oxide. Its electrical thickness is increased by HfO_2 post-deposition anneals. Comparative TEM characterizations of this interface shows that the post-deposition annealing has not an significant influence on its physical thickness but modifies its nature: its dielectric constant intermediate between HfO_2 and SiO_2 material becomes similar to SiO_2 one. We have also notice that polysilicon process may induce a stretch out of C-V characteristics associated to a clustering of fixed charges.

6. Acknowledgments

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