A New Improved Model for LDMOS Transistors under Different Gate and Drain Bias Conditions

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Abstract

The behaviour of the capacitances of LDMOS devices as a function of gate and drain bias is analysed using TCAD simulations and S-parameter measurements. Both simulations and measurements revealed that instead of the smooth sigmoid shape usually seen in MOSTs, the capacitances of LDMOS devices show a distinct ridge at low values of $V_{ds}$. A full analysis of this phenomena is used to propose a significantly improved macro-model for the DMOS device.

1. Introduction

DMOS devices are being increasingly employed in dynamic applications such as switches in power systems and fine slope control in electrical motor drives. However, existing DMOS models are not sufficiently accurate and SPICE models are especially poor when modelling AC performance. It is known that the intrinsic gate-drain and gate-source capacitances, which to a large extent determine the turn-on and off characteristics of a switch, are not well modelled. To investigate the capacitance behaviour and develop an improved model, TCAD simulations and S-parameter measurements have been performed.

2. Device description

A cross-section of the device under investigation is presented in Figure 1. The Alcatel Microelectronics I2T-flow is based on a 0.7\textmu m CMOS process-flow to which some extra masks and implants have been added to provide the high voltage features. From figure 1 it can be observed that the LDMOS transistor is an asymmetric device, with the drift region on the drain-side located in a lightly doped N-tub.

Figure 1. Section through an LDMOS

The channel is self-aligned to the source and is created by the out-diffusion of the P-body under the gate. As a result the dopant distribution along the channel is non-uniform and decreases towards the drain end. Higher breakdown voltages are achieved due to the depletion region that extends from the P-body into the drain which provides a voltage drop between the drain contact and the channel-region. The gate oxide and the polysilicon extend beyond the channel of the device as illustrated in figure 1.

To develop the new model an LDMOS device is both measured and simulated for a number of bias conditions. The gate voltage is swept between –5 and 10V with the drain voltage stepped between 0 and 18V in 2V increments. S-parameters are measured on-wafer at frequencies up to 5GHz using a 37369B Anritsu-Wiltron vector network analyser and a simple open-de-embedding procedure is used.

TCAD simulations are performed using Silvaco software with the process input deck having been calibrated using SIMS and SRP profiles as well as SEM cross-sections. The device simulations are performed using the Lombardi model for the carrier mobility which takes into account high-field velocity saturation effects.
3. Intrinsic drain voltage ($V_K$) behaviour in relation to gate and drain voltage [1,2]

The intrinsic low-voltage MOS transistor is delimited by the source of the high voltage transistor and the end of intrinsic inversion channel (the boundary between the p-region and the extended drain n-region, as shown in figure 1). This location is called the K-point and its potential is denoted by $V_K$. TCAD has the great benefit that the simulations allow us to analyse the variation of $V_K$ in all regions of transistor operation with respect to the gate voltage and drain voltage. From figure 2(a) one can observe that $V_K$ remains at a low voltage (below 7V). It should be noted that self-heating was not enabled in the numerical simulations and, consequently its impact on device characteristics is not discussed.

![Image](a)

![Image](b)

![Image](c)

Figure 2. LDMOS channel voltage variation as a function of $V_{GS}$ and $V_{DS}$: (a) 3-D representation, (b) $V_K$ vs. $V_{DS}$ for different values of $V_{GS}$, (c) $V_K$ vs. $V_{GS}$ for different values of $V_{DS}$

The analysis of $V_K$ provides information on the operation regions (linear/saturation) of the intrinsic MOS device and the variation of the voltage drop over the drift region. Figure 2 illustrates in detail the behaviour of $V_K$ as a function of $V_{DS}$ for constant $V_{GS}$ (fig. 2(b)) and the behaviour of $V_K$ as a function of $V_{GS}$ for constant $V_{DS}$ (fig 2(c)). From fig 2(b) one can see that $V_K$ rises as a function of $V_{DS}$ which drives the intrinsic transistor from the linear region into saturation. Fig 2(c) indicates that at first there will be an increase in $V_K$ when $V_{GS}$ rises. This increase can be attributed to the raised surface potential. However, $V_K$ starts to decrease when $V_{GS}$ is increased further and the maximum of $V_K$ occurs at higher $V_{GS}$ value as $V_{DS}$ is increased.

The analysis of the simulated 2D structures shows that this maximum corresponds to the pinch-off effect resulting from the depletion regions in the drift region (the current is forced through a funnel created by two depletion zones), fig. 3(b). This pinch-off results in a rise in the drift region resistance and, as a consequence of this increase, the voltage drop over the drift region increases. It is this voltage increase that pushes the intrinsic transistor back into the linear regime and thus decreases the voltage at the intrinsic drain node (K-point).

![Image](a)

The region under the gate oxide in the drift region is depleted. No current flow is present

![Image](b)

The region under the gate oxide in the drift region is partially depleted and a funnel is formed through which the current flows.

![Image](c)

The region under the gate oxide in the drift region is now in accumulation. The current flows just under the oxide.

Figure 3. The electron concentration of an LDMOS transistor for different bias conditions (dark region = low concentration; light region = high concentration).

4. Capacitance behaviour of LDMOS transistors

Figure 4 compares simulated and measured capacitance characteristics. A good agreement is observed taking into account that for the measured device the body and the source are tied to ground, whilst in the TCAD characteristics, the body terminal is separated. The most interesting feature in figure 4 is the peak in $C_{gd}$ (the capacitance around the threshold voltage) which has been previously reported in [4]. Conventional MOSFETs do not show such a peak in $C_{gd}$ (see figure 2 of reference
and the behaviour of LDMOS capacitances has been explained in [5] and [6].

5. Proposed model topology

The non-standard behaviour of the LDMOS device cannot be rendered with the standard BSIM3v3.2 model. A dedicated sub-circuit model is required and figure 5 shows the chosen topology for the new model.

Figure 5. Sub-circuit model of LDMOS device

Key features of this proposed macro-model are: (1) the adapted JFET model, modelling the drift region and (2) the shorted PMOS, which models the drift region under the gate oxide. Special care is also required in modelling the K-point behaviour. The following section briefly describes the various components of the model.

5.1 MOS transistor M1 (channel region)

The channel region of the DMOS transistor model is based on the standard low-voltage BSIM3.3v2 model. It should be noted that the BSIM3.3v2 model is not capable of modelling a non-uniform doping profile along the channel but our results have demonstrated that this assumption can be made without introducing a significant error. The BSIM3.3v2 model contains a large set of parameters and, because of the topology of the model, only a small set of the BSIM3.3v2 parameters needs to be extracted.

5.2 JFET J1 (drift region)

The drift region is modelled using a modified FET model where the equations are based on the Schichman & Hodges JFET model. The behaviour of the LDMOS drift region (as explained in paragraph 3) requires an adaptation of the JFET model and this component is implemented using a Verilog-A module containing standard JFET equations where a variable $V_T$, which is controlled by the LDMOS gate, has been introduced.

Figure 6. JFET $V_T$ dependence as a function of $V_{gs}$

5.3 Shorted p-type MOS transistor M2 & M3

A shorted pmos device (for an n-type DMOS model) has been inserted in order to model the region in the n-tub overlapped by the gate oxide. This region changes from inversion to depletion to accumulation with increasing $V_{GS}$.

5.4 Diodes D1 & D2

The separation of the body-drain diode into two components located on each side of the drift-region JFET is important in order to correctly predict several pronounced peaks which are observed in the capacitance characteristics.

5.5 Diode D3

This diode is used to model the leakage current and capacitances that exist between the different layers from drain to substrate.

6. Results and discussion:

The parameters for this new model have been extracted from LDMOS devices capable of handling 40V on the drain and 13V on the gate. The extractions are performed on a set of devices with different widths ranging between 20µm and 250µm. The model has been verified for the complete bias range and good agreements between the model and measurements have been obtained as illustrated in figure 7. The temperature behaviour of the model has been validated for temperatures ranging between -50ºC and 180ºC.

6.1 DC-curves:

Figure 7 shows the DC-results for the proposed model. One can observe the good agreement between simulations and measurements. A difference between the
simulations and measurements at large $V_{GS}$ and $V_{DS}$ can be detected from figure 7(b) which is caused by self-heating which is not modelled.

Figure 7(c) shows the voltage over the intrinsic MOS and JFET regions. One can see that the voltage over the intrinsic MOS region is limited to a low voltage and the high voltage drop, present in the drift region, is handled by the JFET, which corresponds to the behaviour described in [2].

Figure 7, Comparison of DC characteristics. (a) Id-Vg and gm plot; (b) Id-Vd plot; (c) voltage over the channel MOS-transistor and the JFET

6.2 AC-curves:

Figure 8 shows the AC-results of the proposed model. The peak in $C_{GD}$ at low $V_{GS}$ can be observed with the resistive division between $C_{GD}$ and $C_{GS}$ at higher $V_{GS}$ being modelled. At $V_{GS} \leq 0\,\text{V}$ a mismatch in $C_{GS}$ and $C_{GD}$ can be seen. This spike is caused by the shorted PMOS as the transition between inversion and depletion simulated by the model does not exactly correspond to the behaviour observed in the measurements. However, precise modelling of this spike region is not particularly important as the LDMOS device is not typically used at this bias condition ($V_{GS} \leq 0\,\text{V}$).

Figure 8. Simulated and measured $C_{GD}$ curves as functions of $V_{GS}$ at $V_{DS}=0\,\text{V}$

7. Conclusion

An improved DMOS macro-model has been presented which, in contrast with other macro-models, is physically based and covers all bias-regions, including quasi-saturation and particular impact of drift region on DMOS capacitance behaviour. It performs well for both DC and AC regimes and, as standard elements or verilog-A blocks have been used, is simulator independent.

8. Acknowledgements

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9. References


