Impact of Post Metal Etch Resist Strip in Plasma on Plasma Charge-Induced Erosion of Tungsten-Plugs

Malik Fatkhoutdinov, Eddy De Backer, Pierre Bruneel
Alcatel Microelectronics, Westerring 15, B-9700 Oudenaarde, Belgium
malik.fatkhoutdinov@mie.alcatel.be

Abstract

Erosion of W-plugs in vias during the treatment in chemical solution after etching of aluminium-interconnects above the plugs was attributed to positive charging of the interconnects during the metal etch [1]. Quite a range of methods was proposed to tackle the problem. Those include specially designed solvents for BEOL operations, discharging of interconnects using electron beam [2], passivation of tungsten in a low pH dilute nitric acid solution prior to treatment in solvents [3] etc. It was also demonstrated [4] that the problem can be solved if an oxygen-based post metal etch plasma resist strip is replaced by ozone-ashing. It is shown here that the post metal etch resist strip operation plays the main role in either inducing or reducing the effect of W-erosion. The failures can be avoided simply by careful optimisation of the in-situ dry resist strip process as well as by introducing a proper extra ex-situ plasma treatment.

The results of the development work are implemented in an industrial 0.35 µm technology.

1. Introduction

Al-based metallisation and tungsten filled via plugs is a dominant interconnect architecture for the technologies from 0.6 µm down to 0.25 µm and even below. Though normally targeted, a robust overlapping of the vias by the metallisation above is almost never a case. And the tungsten in vias, at least partially, can be exposed to treatments related to a metal patterning, including the post metal etch polymers removal in chemical solution. It was noticed [1;4] that the erosion of tungsten normally occurs in poorly overlapped vias that connect metallisation structures electrically isolated from the substrate.

Identification of the failing vias in the circuit is not an easy task. But it is comparatively simple to find them on regular electrically floating vias chains. Here a passive voltage contrast technique can be applied to identify the location of electrically open vias and FIB and SEM imaging can help with the analysis. To control the defectivity of the vias we use so called via-yield monitor structures containing metal1-via-metal2 chains. Typical size of such a chain is 100,000 vias per chain. The results of the electrical measurements are expressed in the number of failing vias per chain of 1E8 vias, and this largely helps to quantify the effect of process changes. Apart from that the procedure can be formalised and quite a big number of wafers can be included into each split and a reliable statistic can be built up, because the electrical analysis is comparatively fast. We used normally 5-8 wafers per split, and the results of the experiments were reconfirmed several times.

Though metal1-via-metal2 interconnect structures are only discussed here below, similar results were demonstrated for the tungsten plugs contacting Poly-silicon gates and a substrate.

Analysis of the failures normally showed missing or empty vias. The missing vias are attributed to lithography problems (figure 1a). While there might be several causes for the empty vias. But the fact that the frequency of this kind of failures is very sensitive to the changes in the scheme of treatments after top metal etch indicates that in our case it was related to an erosion of W-plugs in post metal etch cleaning solution (figure 1b).

2. Experimental

In this study p-type <100> 6" Si-wafers with only above mentioned tests structures were processed according to 0.35 µm technology rules. The first Al-Cu metallisation with Ti/TiN barrier was created on top of a blank PECVD oxide layer. CMP planarised HDPCVD oxide was used as an inter-metal dielectric. Tungsten was used to fill 0.5µm in size vias, following the deposition of Ti/TiN barrier layer. There was no any deliberate
misalignment introduced between the vias and metal2 structures. The metal etch was done using either a MERIE chamber with an in-situ down-stream strip chamber or a HDP chamber with an in-situ DSQ strip module. In-situ plasma strip included a water-vapour step and an oxygen based step. Prior to a wet removal of polymers in basic solution some of the wafers received an extra plasma treatment.

3. Results and discussion

3.1. Extra ex-situ plasma treatment prior to cleaning in basic solution

Initially an extra ex-situ oxygen based 30sec long treatment was tried out in a down-stream plasma asher after the in-situ resist strip. This resulted in higher via loss than that of the standard split, which only received in-situ strip prior to solvent clean. Though the standard split had also quite high defectivity. The results correspond with the findings in [4]. Further on an oxygen based ex-situ plasma strip was replaced by the plasma treatment in Forming-gas (mixture of 4% H2 in N2) using the same system and all the same process settings except the gas composition. The latter process significantly reduced the via failure rate. And the duration of the treatment in Forming-gas did not have an impact (15sec vs 80sec long process).

In another test a comparison was done with the combined process where the 30sec long oxygen based strip step was followed by a 15sec long Forming-gas plasma step. This demonstrated that the negative impact of the oxygen plasma can be successfully wiped out by a short treatment in Forming-gas. The results are summarised on figure 2.

An attempt to use thermal oxide wafers and Plasma Damage Monitor (PDM) tool to detect the surface charges created by an ex-situ plasma treatments has failed because the noise level (wafer-to-wafer and within the wafer variation) of the PDM voltage was higher than the difference of averages for different groups, and the variation of the voltage was only within a range from -1 to +2 V.

Similar positive impact on via-integrity was demonstrated when the wafers were treated ex-situ in He-environment of down-stream isotropic etcher, Ar-environment of RIE etcher, fluorine and oxygen mixture of RIE etcher and Forming-gas with oxygen and nitrogen additives of down-stream asher.

Analysis of the failing vias showed missing holes on the wafers of the last three splits in graph 1, while the majority of failing vias of the first two splits were empty.

The post metal etch polymers removal in basic solution was done in a spray batch -tool. A standard process is run at 70°C for 20 min. It was noticed that after resist strip in oxygen plasma the duration of the treatment impacted the integrity of the vias, and they were failing starting from about 10 min long exposure to the solvent. But once an optimised extra plasma treatment is done the vias are no longer sensitive to the solvent.

Figure 3 illustrates the via integrity verses the time of wet cleaning. Here the first is a standard split as described above, the other three splits after the in-situ strip received extra treatment in a fluorine based plasma. Split 2 was only rinsed in DI-water with no exposure to a solution, split 3 received 6 min long exposure to a basic solution and the split 4 received 20 min long exposure.
3.2. In-situ resist strip process

The in-situ resist strip process is normally designed to prevent post etch corrosion of aluminium and to remove the remaining resist after metal etch. Water vapour based process step is most efficient for the corrosion prevention while the oxygen based plasma step is mostly used for the bulk resist removal, though both steps still do the job for both purposes. Usually the process starts with a water based strip, which is followed by an oxygen plasma step. As it was demonstrated earlier, the negative impact of the oxygen plasma could be reduced by the following Forming-gas treatment. Here an impact of the water vapour plasma treatment was investigated. The standard process included 60sec long water strip step followed by 90sec long O2 plasma step. For the second group of wafers one more, only 10sec long, water based plasma step was added at the end of the in-situ strip process. All the wafers were directly transferred for processing in the basic solvent. Figure 4 illustrates the results of electrically measured via defectivity.

![Figure 4. Number of failing vias per 1E8 chain when different in-situ plasma resist strip processes were applied](image)

As one can see, just a small modification of the in-situ strip recipe can make things very different. In-situ strip in oxygen plasma with the water vapour additives also results in positive outcome.

Though the PDM tests demonstrated clear charging picture of the metal etch steps (with the PDM voltages above 10V and min/max range above 15V), the difference in PDM voltages of different strip steps was again below the noise level.

4. Conclusion

Post metal etch plasma resist ashing is the main contributor to a charge induced erosion of tungsten plugs during the wet cleaning in a basic solution. The failures can be avoided simply by optimisation of in-situ plasma strip processes as well as by introducing a proper ex-situ plasma treatment. For the in-situ resist strip a water vapour containing plasma process and/or just the last process step was found to be efficient. An ex-situ extra plasma treatment can be recommended, for instance, for reducing the in-situ strip time and improving the throughput of metal etchers, for removal of polymers in fluorine based plasma etc. Here a gamma of processes can be offered to suit virtually any requirements. Once an extra ex-situ treatment is introduced, the in-situ strip process no longer affects the final results. Despite the obvious impact on the via integrity the different post etch plasma treatments do not show noticeable differences in charging behaviour. That is why the judgement of the impact could only be done based on direct electrical measurements of via integrity. But it is still obvious that the plasma resist strip process overwrites the charging picture related to metal etch and only the very last step of the plasma treatment prior to exposure to a solution makes all the difference.

5. References