Impact of source/drain implants on threshold voltage matching in deep sub-micron CMOS technologies

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Abstract

A new mechanism causing deterioration of the threshold voltage matching performance of MOSFETs is described. We demonstrate that this effect depends on several fundamental CMOS device architecture aspects such as the source/drain implant energies, the gate layer thickness, a gate top oxide layer thickness and the polysilicon gate morphology. It is concluded that penetration of a small (fluctuating) fraction of the LDD and HDD source drain implants through the gate can be responsible for severe degeneration of the matching performance of deep sub-micron CMOS technologies.

1. Introduction

For analogue circuits, such as digital-to-analogue converters, current mirrors, band-gap references, differential amplifiers, but also for digital applications, like large SRAMs, the transistor matching performance of a process is an important device architecture performance indicator [1].

Matching describes the fluctuation of the differences between transistor parameters for closely located identical transistor pairs. One of the most important CMOS matching performance indicators is $\Delta V_T$, which relates the $V_T$ mismatch fluctuation standard deviation to the inverse of the square-root of the effective device area [2]. Threshold voltage matching is affected by the gate oxide thickness and the microscopic fluctuations of the channel dopant (see for example [3]).

The experiments described in this paper were initiated by the alarming observation that (in a development version of our 0.25 µm CMOS process) the NMOST $\Delta V_T$ was anomalously high, compared to the $V_T$ matching scaling theory. This is depicted in figure 1 where the standard deviation of the threshold voltage mismatch of NMOS devices with the minimum gate area is plotted versus the process generation. The ‘17 mV’ dashed line in figure 1 indicates a target benchmark, roughly based on a ‘1 mVµm per nm gate-oxide’ rule of thumb [2]. Note that a 1 sigma $\Delta V_T$ fluctuation of 35 mV becomes unacceptably large compared to the total allowed process spread window for advanced CMOS technologies.

This paper describes a set of experiments that helped to identify and solve this problem.

![Figure 1. The spread in the threshold voltage difference between two closely separated identical NMOS devices with a minimum gate area (minimum width and length) as a function of process generation. The line indicates a target benchmark value based on the gate area and gate oxide thickness.](image)

2. Experiments

The experiments were performed during the yield and reliability fine-tuning phase of a 0.25 µm CMOS process. The base-line process uses shallow trench isolation (STI)
and nitride spacers with a width of 80 nm. The gate oxide thickness is 5 nm and the gate layer is deposited as a 200 nm thick amorphous Si layer, which crystallises into a poly silicon layer during subsequent anneal steps. The NMOS devices (which are the topic of this study) receive Arsenic LDD and HDD source/drain implants and an Indium \( V_t \) adjust implant. Typical implant doses for the LDD and HDD implants are \( 2 \times 10^{14} \) cm\(^{-2} \) and \( 3 \times 10^{15} \) cm\(^{2} \) respectively. These implants are done at an angle of 7°, the LDD implant is done in QUAD mode.

The gate poly layer is (over)doped in the desired flavour using the LDD and HDD implants. In this process, the gate poly is pre-doped with phosphorus to reduce gate depletion, thus increasing the drive current \( (I_{on}) \) of the NMOS devices.

In the experiments described in this paper the following process settings were varied:
- LDD as well as HDD implant energies
- Gate poly layer thickness
- Gate morphology
- Poly re-oxidation

Threshold voltage matching is determined by measuring the threshold voltage fluctuation of closely spaced transistor pairs of varying dimensions using the three point method (described in more detail in [5]). The used transistor dimensions are \( W/L=80/80, 40/40, 20/20, 12.8/12.8, 6.4/6.4, 3.2/3.2, 1.6/1.6, 0.8/0.8, 0.35/0.25 \). The extent and relevance of the experiments are depicted in figure 2, showing the mismatch standard deviation observations for a devastating 13 mV\( \mu \)m example, compared to a quite acceptable 6.7mV\( \mu \)m result.

$$\sigma(\Delta V_t) = A_{Vt} (WL)^{-1/2}$$

**Figure 2.** Examples of the threshold voltage mismatch fluctuation standard deviations as a function of gate area. The slopes of the lines represent \( A_{Vt} \).

### 3. Experimental Results

Figure 3 shows the \( A_{Vt} \) of the NMOS transistors as a function of LDD implant energy for two different HDD implant energies. From this figure it is clear that both a reduction of the LDD energy and of the HDD energy, result in a better matching performance. The optimal \( A_{Vt} \) is obtained by reducing both the LDD and HDD implant energies.

**Figure 3.** NMOS \( A_{Vt} \) as a function of LDD implant energy. Circles are for low energy and squares for high energy HDD source/drain implants.

Figure 4 shows the NMOS matching as a function of deposited gate poly thickness. The matching performance improves significantly with increasing poly gate thickness.

**Figure 4.** NMOS \( A_{Vt} \) versus poly thickness. The different symbols are for two different batches.

The influence of the implant energies on the threshold voltage matching as seen in figure 3, triggered some additional experiments on scatter oxide thickness. In the default processing after the poly etch, a 5 nm re-oxidation of the poly is done. This oxide serves as a
scatter oxide for the subsequent LDD implant. Figure 5 shows the threshold voltage matching as a function of this oxide thickness. A particularly severe degradation of the matching with decreasing oxide thickness is observed.

![Figure 5. AVt versus poly re-oxidation thickness.](image)

Lastly, effects of the poly grain size on the matching behaviour have been investigated. The following two ways of forming the poly silicon gate layer are studied:

- An amorphous silicon layer is deposited at a temperature of 560 °C. A side-wall oxidation after the gate etch subsequently transforms the amorphous layer into poly silicon. The poly silicon that is formed in this way consists of crystallographic randomly oriented relatively large silicon grains (typical grain size 200 nm, hence locally in the range of the gate layer thickness).
- Alternatively, fine grained poly silicon is deposited at a temperature of 620 °C. This layer consists of relatively small randomly oriented silicon grains at the oxide interface (typical grain size of the order of 50 nm) while a clear (110 oriented) columnar structure develops as the layer grows thicker (see Figure 6).

The implant energies for this particular experiment have been chosen relatively high (LDD 50 keV and HDD 60 keV), being typical conditions where we expect from results above that implantation tails of these implants can penetrate locally through the gate layer.

The resulting AVt’s are summarised in table 1. It can be clearly seen that the final gate morphology plays an important role.

<table>
<thead>
<tr>
<th></th>
<th>α-Si</th>
<th>Poly-Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVt (mVµm)</td>
<td>10.3</td>
<td>6.7</td>
</tr>
</tbody>
</table>

![Table 1. AVt of NMOS devices for two different poly morphologies.](image)

4. Discussion

The root cause of the enhanced threshold voltage mismatch fluctuation compared to previous CMOS process generations was pinpointed to a new phenomenon: local (random) penetration of the LDD and HDD implantation through the gate.

The implantation energies of HDD and LDD source/drain implants of CMOS processes are commonly optimised for sheet resistance, short-channel effects and hot-carrier degradation performance. In principle, the projected ranges and straggles of these implants are chosen such that the HDD and LDD implants will not reach the channel region (through the gate layer and its dielectric). This is usually verified by monitoring the threshold voltage of large transistors or C-V measurements. For the process under discussion, the impact of the source/drain implants on the Vt was considered to be negligible.

The basic explanation for the observed impact of LDD and HDD implants on threshold voltage matching is that part of the implanted species penetrates through the gate, depending on the local (random) crystal orientation of the poly-Si grains.

As is well known, the depth of an implantation in silicon depends on the crystal orientation of the material it is implanted in. This is why most ion implantations in (100) silicon are performed slightly off axis to avoid channeling tails. The new element of the current study is that we clearly demonstrate that when a source/drain implantation is implanted into a gate layer, the local orientation of the crystal grains in the poly layer serve as a random scattering mechanism: Some poly grains are oriented such that channelling will be inevitable, whereas (most) other grains will block the implant more effectively (figure 7A).
channeling

increased oxide layer to reduce channeling

Fine grained poly to reduce channeling

Reduction of the implant energy to reduce channeling

Figure 7. Schematic view of the matching problem described in this paper (A) and the three possible solutions examined in the experiments (B,C,D)

All experiments presented above support this explanation:
- Lower implantation energies result in a smaller fraction of the dopants reaching the substrate (figure 7B).
- A thicker gate layer similarly prevents more effectively the implantation from reaching the MOST channel region.
- A sufficiently thick (amorphous) scattering layer on top of the gate again increases the stack thickness and (more importantly) reduces the channelling susceptibility (figure 7C).
- Finally, the improvement due to fine grained poly (figure 7D) can also be attributed to a reduced susceptibility for ion implantation channelling: In the standard poly layer the grains are large and randomly oriented, hence some of these grains will inevitably be oriented 'favourable' for implant channelling. The poly layer deposited at a higher temperature lacks these channelling paths. Moreover, the standard 7° S/D implantation angle is off-axis with respect to the dominant (110) crystal orientation in the fine grained poly layer columns.

A similar observation of improved matching for finer grained poly silicon was reported in [5]. In that study the matching improvement was attributed to reduced gate depletion for fine grained poly. That this is not the case in the present work is demonstrated by figure 4: If gate depletion fluctuation would have been the main $V_t$ fluctuation cause, $V_t$ matching would deteriorate for thicker poly (more gate depletion), whereas we observe the opposite behaviour.

Finally, it should be noted that although the implant dose of the regular HDD implant is much higher than the dose of the LDD implant, the impact on the $V_t$ mismatch fluctuations of these two implants is apparently of the same order. This can be explained by assuming that only a fraction of the large implant dose can indeed channel. The amorphisation of the top region of the poly silicon by the relatively heavy As ions at these energies quickly forms an (amorphous) scattering top layer that prevents significant channelling beyond a certain 'threshold dose'.

5. Conclusions

A new mechanism responsible for degeneration of the threshold voltage matching performance of deep sub-micron CMOS technologies has been identified. Due to the reduction of the poly gate thickness for these technologies, (random) penetration of a small fraction of the LDD and HDD implants into the channel area may occur. This severely deteriorates matching behaviour. We demonstrate that the extent of this effect depends on the implant energies, gate thickness, poly re-oxidation layer and poly gate morphology.

With the reduction of the gate layer thickness and the introduction of even more elaborate device architectures for advanced deep sub-micron technologies (e.g. Halo's or pockets), careful evaluation and control of threshold voltage fluctuation enhancement effects like the phenomena discussed in this paper, form indispensable elements of CMOS device architecture optimisation.

References