Design and simulation of an a-Si:H/GaAs Heterojunction Bipolar Transistor

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Abstract

Results from a detailed simulation study are presented to help evaluating pros and cons of a wide gap hydrogenated amorphous silicon emitter (a-Si:H) introduced for improving the injection efficiency at the emitter-base junction of a GaAs bipolar transistor. For a set of devices withstanding the same maximum emitter-collector voltage, it is shown that, in spite of the poor carrier mobility in a-Si:H, the emitter thickness has a minor effect on the device current gain, which is instead strongly influenced by the base thickness. The base thickness also has a weak impact on the cut-off frequency, which however shows a clear dependence on electron mobility in the emitter.

The study predicts that the current thin film silicon technology would allow the fabrication of a transistor performing a DC current gain close to 3000 and a cut-off frequency close to 10 GHz. Due to the simplicity of fabrication, such a device could represent an effective way to add a bipolar stage to a GaAs MESFET IC without recurring to AlGaAs/GaAs heterostructures.

1. Introduction

The npn AlGaAs/GaAs heterojunction bipolar transistors (HBT) are widely used in analog and digital appliances for wireless communication, optoelectronics and high speed computing. In fact the insertion of a wide-gap AlGaAs emitter permits to fabricate devices with a very high current gain, which is in turn traded for larger bandwidths [1]. Presently, the fabrication of these devices is based on either the molecular beam epitaxy (MBE) or the metal organic chemical vapour deposition (MOCVD), two outstanding epitaxial technologies which however require expensive and hazardous equipments.

In the last years the increasing interest for the exploitation of hydrogenated amorphous silicon (a-Si:H) and silicon carbide (a-SiC:H) as wide gap semiconductors compared to other important crystalline semiconductors, has led to the proposal of several amorphous/crystalline HBT’s [2-3]. In fact, with an energy gap exceeding 1.7 eV, a-Si:H promises to allow the fabrication of high-gain HBT, while requiring a technology which is far simpler than those based on the classical heteroepitaxy.

As a contribution to the study of possible applications of a-Si:H as a wide gap semiconductor, in this work DC and high frequency characteristics of a new HBT technology are investigated by means of numerical simulations. The proposed device in particular performs a hydrogenated amorphous silicon emitter, while the base and collector regions are made of GaAs. A commercial finite element simulator of semiconductor devices, which takes into account the distributed density of states typical of amorphous materials, was utilised throughout the work. For a careful tuning of the electronic properties of the amorphous layer, the results of a previous study, which involved the fabrication and characterisation of ad hoc devices [4], were considered.

2. Characteristics of an a-Si:H/GaAs heterojunction

The preferred deposition technique for thin film a-Si:H is the plasma enhanced chemical vapour deposition (PECVD) in a SiH₄ ambient, at temperatures between 200 and 280 °C. In fact, this technique ensure a high degree of hydrogenation which allows a control of the number of defects and the width of the energy gap [5]. Generally, depending on the deposition technique and parameters, a-Si:H can show an energy gap \( E_g \) in the range 1.6-1.9 eV. Due to the low deposition temperature, the technology of a-Si:H is compatible with that of many other semiconductors, and in particular with GaAs. The potential advantages of the association of these two semiconductors come from the band offsets establishing at the heterojunction. The two materials have in fact almost the same electron affinity, being \( \chi_{a-Si:H} = 3.93 \) eV [6] and \( \chi_{GaAs}=4.07 \) eV. The energy gap difference \( \Delta E_g \) is therefore mostly located at the valence band side, with a valence band offset \( \Delta E_V \) up to 0.36 eV. Such a configuration for an emitter-base junction of a npn HBT would in theory result in a current gain increase by a factor \( \exp(\Delta E_V/kT) \approx 10^6 \) [1], at room temperature. In addition, due to the lack of a crystal lattice in a-Si:H, no strain exists at the interface whatever the energy gap difference, a clear advantage in comparison with AlGaAs/GaAs heterostructures.

Unfortunately experimental works have shown that the density of states at the amorphous/crystalline interface has a negative impact on the base current of a HBT [7]. Moreover, the electron and hole mobilities in
a-Si:H is very low and the resulting poor conductivity can be compensated only in part by a higher doping because the doping efficiency is always low in a-Si:H [5].

In an effort of gaining more insight into such kind of structures, and identifying the critical aspects determining their electrical behaviour, a-Si:H/GaAs heterojunctions have been studied recently [4]. In particular the characteristics of an experimental heterojunction pin diode were compared to those calculated by means of the finite element device simulator ATLAS [8], showing that limiting the number of defects located at the interface below a critical level would dramatically improve the minority carrier injection ratio at the heterojunction. Such level, moreover, is close to that technologically attainable today. Moving from those considerations, in this paper the design approach and the predicted DC and AC characteristics of a GaAs bipolar transistor with a wide gap a-Si:H emitter will be discussed.

3. HBT structure and simulation settings

A schematic representation of one half of the a-Si:H/GaAs HBT considered in this work for simulations is reported in Figure 1. The device is in particular designed for a low power GaAs technology ($V_{DD} \leq 5$ V).

![Fig. 1. Schematic representation of one half of the simulated a-Si:H/GaAs HBT](image)

The fundamental geometrical and electrical characteristics are summarised in Table 1 for the base and collector regions, and in Table 2 for the a-Si:H emitter region.

The parameters $N_{G,C}$ and $N_{G,V}$ are respectively the integrals over the whole energy spectrum of the two gaussians located in the gap representing the defects associated to the dangling bonds throughout the gap. However a detailed description of the way these defect distributions in a-Si:H were considered for our simulations is contained in Refs. 4 and 9.

![Tab. 1. Simulation parameters in the GaAs regions](image)

![Tab. 2. Simulation parameters in the a-Si:H emitter region. Other parameters were set as in Ref. 4](image)

The a-Si:H(n) emitter stripe is 0.5 µm wide, with an emitter-base distance of 0.25 µm. In order to determine the effect of the emitter thickness on the device performances, three sizes were considered for it, namely 5, 10 and 20 nm. To compensate for the low carrier mobility, the emitter region was assigned a doping level of $6 \times 10^{18}$ cm$^{-3}$, which is close to the technological limit for a-Si:H.

The base doping was changed between $10^{17}$ and $5 \times 10^{18}$ cm$^{-3}$. The base thickness ranged accordingly between 5 and 200 nm to guarantee a base punch-through voltage of 5 V.

4. Simulated DC characteristics

The devices considered in our simulations are listed in Table 3 with the relevant technological characteristics. The emitter and collector areas are 25 and 75 µm$^2$ respectively for all devices.

![Tab. 3. Parameters characterising the various simulated devices](image)

The parameters $W_E, W_B$ and $N_B$ are respectively the emitter thickness, the base thickness and the base doping. Devices A, B and C differ only in the emitter thickness, while devices A, D, E, F and G fundamentally differ each other in the base doping. However, in order to compare devices designed for the same application, the base width was scaled in each HBT in a way such that they had the same maximum base punch-through voltage, i.e. $V_{CE, max}=5$ V.

The corresponding DC current gain plots for $V_{CB}=0$ are shown in Figure 2 and Figure 3. The three devices with different emitter thickness but same base doping have in fact similar characteristics. This demonstrates the minor role played by the emitter size, which is justified by the very low hole diffusion length in the amorphous film. A useful aspect of this result is that one
can design devices with extremely thin emitters, with clear advantages on the high frequency performances and minor effects on the base current.

5. Simulated AC characteristics

The small signal analysis of the devices type A, E and F was performed to assess their high frequency behaviour. Proceeding from a DC solution at an assigned bias, the simulator applies a frequency swept AC generator to the base contact, with the device used as a common emitter amplification stage. We focused our attention on the small signal current gain $\beta_{AC}$, the transconductance and the scattering parameter $S_{21}$.

The short circuit AC current gain $\beta_{AC}$ was calculated with the devices biased in the active region, with $V_C=3\,\text{V}$, $V_E=0$ and $V_B$ ramping from 1.0 to 2.0 V. The quite large emitter-base polarisation is necessary to sustain a base current $I_B$ parallely ramping from $10^{-9}$ to $10^{-4}\,\text{A}$. As an example the simulation results for $V_B=1.6\,\text{V}$ are shown in Figure 4. The three plots are in fact coincident: for all of the devices the low frequency $\beta_{AC}$ is close to 50 dB, while the cut-off frequency $f_t$ is approximately 8 GHz. This is an unusual result for bipolar transistors if one considers the progressive base thinning from 50 to 14 nm, and demonstrates that the base transit time gives a minimal contribution to the overall emitter-collector transit time, being indeed the actual speed limiting factor the emitter junction transit time, and in particular the emitter resistance.

This explains the interest for extremely thin emitter devices in this technology. Our calculations indicate in fact that the emitter differential resistance $r_e$ is in excess of 60 $\Omega$, while common values in standard GaAs HBT’s are generally in the range of a few ohms. Moreover, by coupling this resistance to an estimated emitter junction capacitance of $2.8 \times 10^{-13}\,\text{F}$, we get an emitter junction transit time $\tau_e$ of $2 \times 10^{-11}\,\text{s}$, which returns a maximum cut-off frequency $f_t = (2 \pi \tau_e)^{-1} = 8\,\text{GHz}$ if one assumes a total emitter-collector transit time coincident with $\tau_e$.

The polar plot of the scattering parameter $S_{21}$, calculated for 50 $\mu\text{m}^2$ emitter area devices, is shown in Figure 5 for samples A, E and F ($V_C=3\,\text{V}$, $V_B=1.6\,\text{V}$.
This parameter represents the voltage gain for matched load, and at low frequencies it is higher than 4, or 12 dB, for all the devices. The parameter $S_{21}$ crosses the unity gain circle at approximately the frequencies of 9 GHz for device F, 8 GHz for device E, and 7 GHz for device A, which are therefore the devices maximum oscillation frequencies.

![Polar plot of the $S_{21}$ parameter](image)

Fig. 5. Polar plot of the $S_{21}$ parameter for three devices with different base doping and thickness

In the same frequency interval the device transconductance was also calculated as shown in Figure 6. It drops from 430 mS/mm, at low frequency, to 240, 195 and 165 mS/mm respectively for device F, E and A, at about 10 GHz.

![Calculated frequency dependence of the transconductance $g_m$](image)

Fig. 6. Calculated frequency dependence of the transconductance $g_m$ for devices with different base thickness and doping

Once again the maximum oscillation frequency of 9 GHz calculated for device F slightly differs from that of the 50 nm thick base device A.

The device high frequency characteristics are obviously affected by the quality of the amorphous layer. Table 4 in fact summarises the calculated cut-off frequencies $f_i$ for the device E for various electron/hole mobilities and for two gap states concentrations, namely $10^{18}$ and $3 \times 10^{18}$ cm$^{-3}$. The results demonstrate that the cut-off frequency is remarkably sensitive to the carrier mobility while showing a lower dependence from the defect concentration.

6. Conclusion

DC and AC characteristics of an a-Si:H/GaAs npn HBT have been computed through numerical simulations. The analysis demonstrated that the emitter thickness has a limited effect on the device DC characteristics. However the presence of a large emitter resistance severely affects the emitter junction charging time. The cut-off frequency is therefore strongly dependent on the amorphous layer electronic properties, and in particular on the carrier mobility. A cut-off frequency of 10 GHz can be predicted in a device with optimised base width and doping.

**References**