Gate dielectrics for high performance and low power CMOS SoC applications

F.N. Cubaynes*, C.J.J. Dachs, C. Detcheverry, A. Zegers¹, V.C. Venezia, J. Schmitz, P.A. Stolk, M. Jurczak², K. Henson³, R. Degraeve⁴, A. Rothschild³, T. Conard³, A. Petry³, M. Da Rold³, M. Schaekers², G. Badenes² L. Date³, D. Pique³, H.N. Al-Shareef⁴, R.W. Murto⁴

Philips Research Leuven, Leuven, Belgium; ¹Philips Research, Eindhoven, The Netherlands; ²IMEC, Leuven, Belgium; ³Applied Materials, Meylan, France; ⁴International Sematech, Austin, TX; *E-mail: Florence.Cubaynes@philips.com

Abstract

This paper investigates the use of plasma nitridation (PN) for fabricating 1.5 and 2 nm gate dielectrics for CMOS system-on-a-chip (SoC) applications. The separate optimisation of PN recipes for high performance (HP, 1.5 nm) and low power (LP, 2 nm) CMOS devices results in good device performance with excellent device lifetime and low 1/f noise. For triple-oxide SoC applications, the use of a common PN step for both HP and LP yields gate dielectrics with excellent breakdown characteristics and devices with the required off-state leakage control.

1. Introduction

Aggressive reduction of the gate dielectric thickness enables the continued down scaling of CMOS transistors. Devices for future portable applications need equivalent oxide thickness (EOT) in the 1.5-2 nm range to yield both HP ($I_{off}$=1-10 nA/µm) and LP ($I_{off}$=10-30 pA/µm) transistors [1]. In this work, we have optimised PN oxides independently for HP and LP applications and obtained good CMOS performances. We have further explored the effect of a common nitridation for multiple-oxide chip configurations.

2. Experimental details

CMOS transistors were fabricated on p-type (100) Si wafers. The gate dielectric was formed by performing PN on thin oxide films thermally grown using rapid thermal oxidation (RTO), or in-situ steam generation (ISSG) oxidation. PN dielectrics for HP and LP applications have been optimised separately. PN recipes were varied by changing such conditions as the He percentage in the plasma and processing time. Pure oxides and furnace nitrided oxides were used as a reference. For the fabrication of sub-100 nm gate length devices, special attention was paid to source/drain engineering using ultra-low energy implantation, optimised HALO’s in combination with spike annealing. Note that common implant conditions were used for both HP and LP devices, so as to avoid additional implant masks when merging HP and LP devices into a single chip.

3. Gate dielectric optimisation

1.5 and 2 nm EOT gate dielectrics were fabricated for HP and LP applications, respectively. The EOTs were extracted from C-V curves (Fig. 1) using the NCSU program [2].

![Figure 1. Capacitance-voltage characteristics measured at 1 MHz on 200 and 100 µm² capacitors for 2 and 1.5 nm EOT, respectively. The EOT was extracted using the NCSU model [2] accounting for quantum size effects and gate depletion.](image-url)

The linear threshold voltage ($V_{th}$) of PMOS transistors for various dopant activation anneals is summarised in Fig. 2. When increasing the thermal budget of the activation anneal, a large $V_{th}$ shift of more than 500 mV is observed for transistors with a furnace nitrided dielectric, indicating excessive B penetration. The very small $V_{th}$ shift observed for heavily nitrided oxides using...
PN shows the excellent resistance against B penetration for such dielectrics, which is in accordance with previous work [3].

Figure 2. Linear threshold voltage vs. anneal temperature for dopant activation with 1.5 nm base dielectrics followed by various nitridation treatment. PN treated samples are effective in blocking B penetration.

The introduction of a high amount of nitrogen in the oxide has also the advantage of reducing the gate leakage current for a given EOT. When using PN, the on-state gate leakage current density is reduced by a factor of 100 and 10 compared to pure oxide and furnace nitrided oxide dielectrics, respectively (Fig. 3). Different PN conditions have been applied for HP and LP applications in order to obtain the lowest gate leakage current for the different EOTs. For 1.5 and 2 nm, the gate leakage current density, measured on NMOS transistors, was 3 and 0.02 A/cm², respectively.

Figure 3. On-state gate leakage current density ($V_{GS}=1$ V, $V_{DS}=0$ V), measured on NMOS transistors (worst case) with various dielectrics as a function of the EOTs. At a given EOT, PN dielectrics exhibit lower gate leakage current than furnace nitrided oxides. PN dielectrics have been optimized independently for HP and LP applications.

The beneficial impact of the plasma nitridation is also observed in the off-state gate leakage current for both N- and P-MOS devices (Fig. 4). The use of heavily nitrided oxides using PN clearly reduces the gate leakage in the overlap region by a factor of 5 to 10 yielding 0.5 nA/µm and 0.8 pA/µm for NMOST (worst case) with 1.5 and 2 nm EOT, respectively.

Figure 4. Overlap gate leakage current, $I_{G_ov}$ ($V_{GS}=0$ V, $V_{DS}=+/−1$ V), measured on N- and P-MOS transistors with a gate length of 0.10 µm with 1.5 and 2 nm EOT gate dielectrics. A reduction of the gate leakage current is seen when using PN nitridation process.

The normalized transconductances (used as an indicator of the channel mobility) of PN base dielectrics are compared to pure oxides for both N- and P-MOS transistors in Fig. 5. Less than 5% mobility degradation is observed for NMOS transistors and 5 to 15% for PMOS transistors when applying plasma nitridation.

Figure 5. Normalized transconductance for (a) NMOS and (b) PMOS transistors of W/L=10 µm/0.1 µm.

4. Digital and analog device performance

The intrinsic performance of N- and P-MOS transistors with optimised PN dielectrics are reported in Fig. 6 for both HP and LP applications. The best CMOS performances are summarised in Table 1.
Figure 6. On-state versus off-state currents measured at a supply voltage of $V_{DD}=\pm 1$ V for NMOS (a) and PMOS (b) transistors for both HP and LP applications.

Table 1. Summary of transistor characteristics with the optimal gate dielectric recipes for HP (1.5 nm EOT) and LP (2 nm EOT) applications.

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ (V)</td>
<td>HP</td>
<td>LP</td>
</tr>
<tr>
<td></td>
<td>1/1.2</td>
<td>1/1.2</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1.5</td>
<td>2</td>
</tr>
<tr>
<td>$L_G$ (nm)</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>$I_{on}$ (nA/$\mu$m)</td>
<td>6/9</td>
<td>0.02/0.026</td>
</tr>
<tr>
<td>$I_{off}$ (nA/$\mu$m)</td>
<td>560/765</td>
<td>290/450</td>
</tr>
</tbody>
</table>

The I-V characteristics of 80 nm devices with a 1.5 nm EOT PN oxynitride (Fig. 7 and 8) illustrate good subthreshold behaviour and drive currents of both HP and LP devices.

Figure 7. $I_{on}-V_{DS}$ characteristics of 80 nm gate length CMOS with gate dielectric of 1.5 nm EOT.

Hot carrier degradation has been measured on NMOS transistors with a 1.5 nm EOT PN gate dielectric. Measurements of the 10% degradation of the transconductance parameter show that the device lifetime is well beyond the 10 years limit for the operating voltages up to 1.45 V (Fig. 9).

Figure 9. Time constants for 10% degradation of the transconductance of NMOS transistors. The lifetime of the devices is well beyond the 10 years limit for any supply voltage below 1.45 V.

Finally, the 1/f noise measured for various CMOS technologies using different gate dielectrics is presented in Fig. 10.

Figure 10. 1/f noise measured at $V_{DS}=V_{GS}=V_{DD}$ for different CMOS technologies. PN dielectrics exhibit a low 1/f noise.
As already reported [4], the incorporation of nitrogen in the oxide degrades the noise behaviour for both N- and P-MOS. In spite of the higher amount of N incorporated in a PN dielectric, the 1/f noise for 1.5 nm EOT gate dielectrics seems to follow the general scaling behaviour observed in Fig. 10.

5. SoC applications

The implementation of multiple gate dielectrics and device types within a single chip requires the use of a common PN step to serve both the HP and LP gate dielectrics. A common nitridation for different base oxide thickness gives rise to a variation of the nitrogen content in the gate dielectrics (Fig. 11): more nitrogen is incorporated in the thinnest base oxide.

![Figure 11. Nitrogen content measured with XPS for various base oxide thickness having received a common nitridation. The thinner the base oxide, the more N in the film.](image)

The change in nitrogen content in the various base oxides does not affect the intrinsic gate oxide reliability (Fig. 12). The acceleration slopes obtained are: 6.24, 5.53 and 5.49 dec/V for the respective EOTs: 1.5, 1.6 and 2 nm. These values are in accordance with previous work [5], demonstrating the viability of a common PN step for a multiple-oxide approach.

![Figure 12. T<sub>bd</sub> vs. voltage stress for different base oxide thickness having received the same PN treatment. The T<sub>bd</sub> values were extracted at 63% of a given T<sub>bd</sub> distribution (measured on 40 devices at 25°C) using a maximum likelihood algorithm. The data are scaled to a reference area of 10<sup>-4</sup> cm<sup>2</sup>.](image)

The performance of gate dielectrics formed using a common plasma nitridation is compared with the independently optimised PN dielectrics in Fig 13. While HP performances are not significantly affected using a common nitridation, LP transistors exhibit a slight mobility degradation of 5% and an increase of the gate leakage current when compared to the best LP devices. Yet, the LP gate leakage remains smaller than the off-state leakage (I<sub>off</sub>&lt;30 pA/µm), implying that the common PN approach still yields the off-state leakage control required for a single-chip solution.

![Figure 13. Maximum of the normalized transconductance as a function of the gate leakage current density for PMOS transistors of 150x5 µm<sup>2</sup>.](image)

6. Conclusion

PN gate dielectrics were optimised for both HP and LP transistors leading to reduced gate leakage current with excellent resistance against B penetration. Very good CMOS performance suitable for portable applications was obtained with excellent lifetime and 1/f noise behaviour. By using a common PN step and identical implant conditions, it is feasible to realize HP and LP devices within a single chip with minimum added process complexity.

7. Acknowledgement

This work was partly funded by the European Union under IST-1999-11599 HUNT project.

8. References