Ar Sputter Etch to Improve the Insulator Quality in Metal Capacitors

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Abstract

This paper describes how the use of a short soft Ar sputter etch done on the top of the dielectric film of a metal-insulator-metal (MIM) capacitor improves the quality of this film. It was observed that the insulator film as deposited has higher leakage currents and shows early failures during breakdown measurements, while significant lower leakage and tighter breakdown distributions are obtained when a sputter etch is included.

However TXRF and SIMS analysis did not reveal any contamination, it is believed that the top few nanometers of the film are of poor quality, and in this way degrade the performance of the capacitor.

1. Introduction

RF circuits designed in bipolar or BiCMOS technologies require integrated capacitors with high quality factor. This implies that these capacitors should exhibit extremely low dielectric loss combined with minimal series resistance and parasitic capacitance, excellent capacitor matching and linearity. Moreover they should meet the necessary reliability requirements and be processed with low defectivity. Metal-insulator-metal (MIM) capacitors have proven to be the optimal solution. They demonstrate low parasitic capacitance, especially when fabricated at a higher metal level, low series resistance and the required matching and linearity performance, thanks to the absence of voltage induced depletion, as observed in poly-insulator-poly capacitors.

The data reported here is based on MIM capacitors that have been integrated in a 0.35 µm-BiCMOS technology [1]. They aim at a capacitance per unit area of 1.0 or 1.5 fF/µm², an increase that can be achieved by reducing the dielectric thickness. The bottom plate of the capacitor is making use of a regular metal layer, which also serves as metal interconnect layer. A PECVD nitride with a thickness of about 60 (1.0 fF/µm²) or 40 nm (1.5 fF/µm²) has been chosen as dielectric, because of its higher dielectric constant, which allows to scale down the capacitors [2],[3],[4]. A thin TiN/AlCu/TiN stack acts as top plate, which is patterned first with a selective etch chemistry that stops in the dielectric. After etching the top plate and stripping the remaining photoresist, the bottom plate is patterned, together with the interconnect at this level. Once the complete capacitor is formed an intermetal dielectric is deposited and planarized. The top plate of the capacitor is connected through the subsequent via to the next metal (See figure 1). In this way the MIM capacitor module can be integrated at each metal level, except the top metal level.

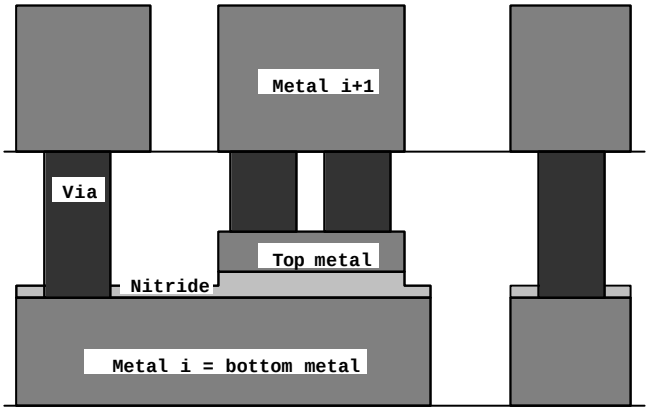

Figure 1. Schematic drawing of a metal-insulator-metal capacitor

2. Experimental data

The electrical performance of the capacitor has been explored. Leakage currents in the order of 1-10 µA/cm² were detected at an electric field of 4.5 MV/cm (about 27 V for 1.0 fF/µm² and 18 V for 1.5 fF/µm², see figure 2). The leakage current variation seemed to be perfectly correlated with the thickness variation across the wafer. In figure 3 the breakdown voltage (electric field) is shown for both thicknesses. Early failures are only observed for the thinnest dielectric. But even so the variation of breakdown voltage is already too high for the thickest dielectric. This becomes clear when the time-to-breakdown (at constant voltage stress) is presented (see figure 4). The large spread in time-to-breakdown implies that failure occurs due to extrinsic breakdown. Lifetimes extracted from this data will not meet the reliability requirements.

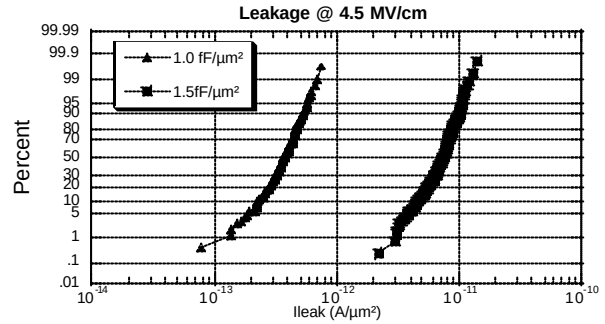

Figure 2. Leakage current of MIM capacitors

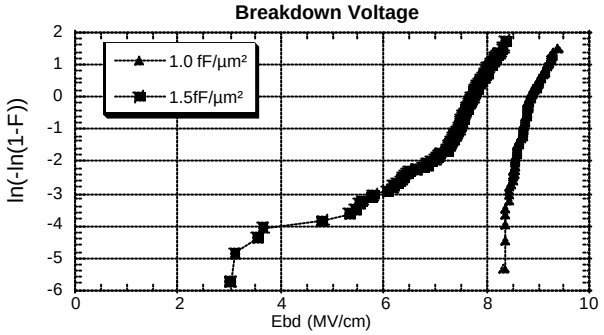

Figure 3. Breakdown voltage of MIM capacitors

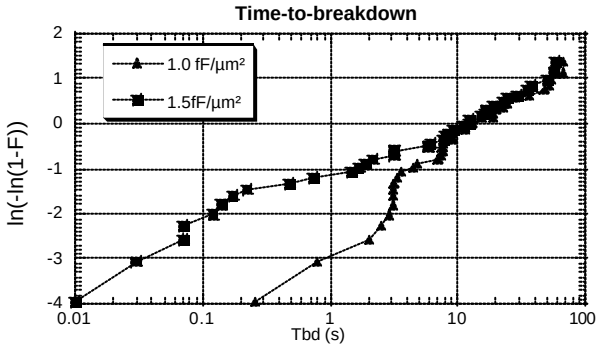

Figure 4. Time-to-breakdown for MIM capacitors (constant voltage stress)

3. Sputter etch

Several experiments were carried out to improve the electrical performance of the MIM capacitors by trying to improve the film quality of the deposited insulator. Films were developed, with different gas ratios and power settings, which allow lower leakage currents, yield higher breakdown voltages and have lower wet etch rates (the latter being some kind of easy in-line measure of the film quality). But none of these films seemed to get rid of the extrinsic breakdown. Above experiments proved that the bulk film quality is not responsible for it.

Contamination of the insulator film during the wait time between insulator and top metal deposition might explain the occurrence of extrinsic breakdown as well. During a short Ar sputter etch prior to the top metal deposition, a few nanometers of the top of the insulator film are removed. Of course the reduction in thickness, which will lead to a capacitance increase, needs to be compensated. A significant reduction of extrinsic breakdown is achieved by implementing a very short sputter etch. It disappears even completely when enlonging the sputtering, but the time-to-breakdown is reduced again due to local thinning of the insulator on the rough bottom metal (see figure 5). When further increasing the sputter etch time, local small peaks in the rough bottom metal become more and more preferential spots for breakdown and yieldloss arises.

Moreover when applying a sputter etch a more uniform breakdown voltage is achieved and a significant reduction of leakage (figure 6 and 7). An optimal sputter etch time should be long enough to remove the contaminated nanometers of the top of the insulator, but not too long to avoid local thinning. Lifetimes in the order of 10^4 years have been extrapolated from the most optimal conditions (100 ppm, at 125°C and 3.63 V).

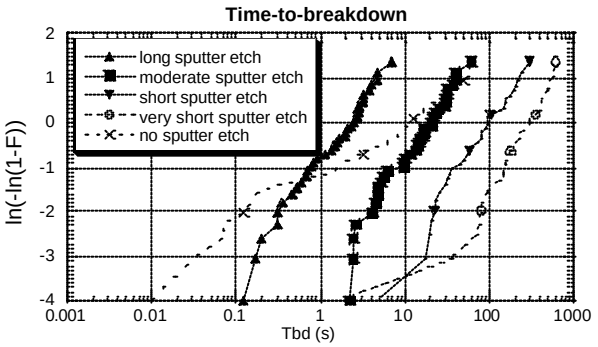

Figure 5. Time-to-breakdown with different sputter etch times (constant voltage stress)

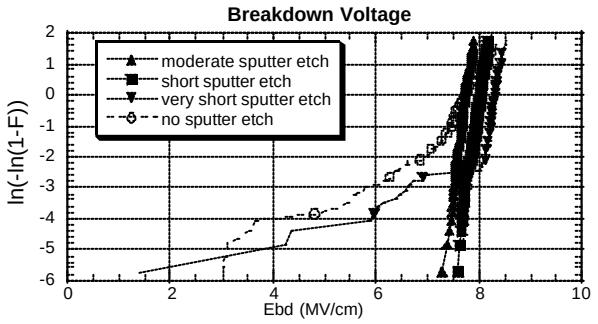

Figure 6. Breakdown voltage with different sputter etch times

TXRF and SIMS analysis has been done to find out what kind of contamination causes the degradation of the electrical performance of the MIM capacitors. Unfortunately the analysis did not reveal something significant.

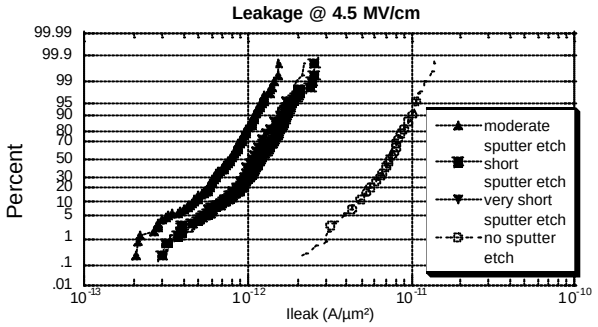

Figure 7. Leakage current with different sputter etch times

4. Sputter etch power

Further tests were performed with different sputter etch conditions. Apparently a sputter etch at low power (low sputter etch rate) yields lower leakage and higher time-to-breakdown than a sputter etch at high power. A higher concentration of Ar in the bulk of the film when sputtering at high power might degrade the insulator somewhat more than when sputtering at low power (see figure 8). The higher leakage current observed with no sputter etch is even not reduced with sputtering at high power (see figure 9).

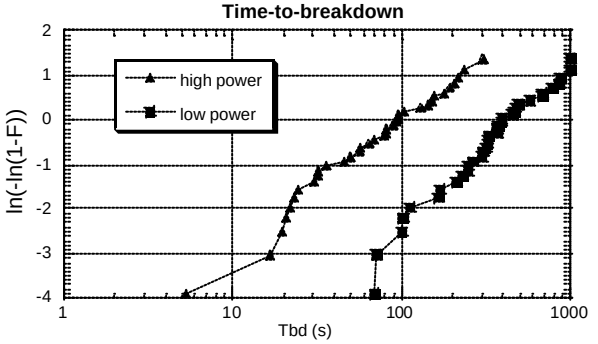

Figure 8. Time-to-breakdown for sputter etch with different power settings (constant voltage stress)

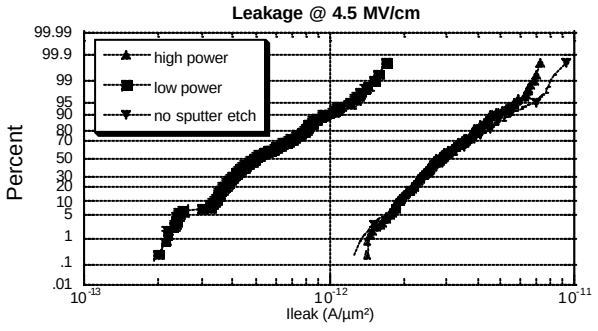

Figure 9. Leakage current for splits with different power settings

5. Conclusion

A short Ar sputter etch at low power prior to the top metal deposition improves the insulator film quality in metal-insulator-metal capacitors. It appears that the top few nanometers of the insulator get contaminated during the wait time between insulator and top metal deposition and need to be removed by the sputter etch. The length of the sputter etching is a compromise between extrinsic breakdown and degradation due to local thinning of the dielectric on top of a rough bottom metal. From the most optimal sputter etch conditions lifetimes in the order of 10^4 years have been extrapolated, together with excellent electrical performance, linearity and matching. Unfortunately TXRF and SIMS analysis did not reveal any significant contamination that might explain the observations.

Sputtering at high power adds more Ar contamination in the film, which reduces slightly the electrical performance of the capacitors compared to sputtering at low power.

6. References

[1] S. Decoutere et al., "A 0.35 µm SiGe BiCMOS Process Featuring a 80 GHz Fmax HBT and Integrated High-Q RF Passive Components", *Proceedings BCTM 2000*, pp. 106-109.

[2] A. Kar-Roy et al., "High Density Metal Insulator Metal Capacitors Using PECVD Nitride for Mixed Signal and RF circuits", *Proceedings IITC 1999*, pp. 245-247.

[3] M. Racanelli et al., "BC35: a 0.35 µm, 30 GHz, Production RF BiCMOS Technology ", *Proceedings BCTM 1999*, pp. 125-128

[4] D. Harame et al., "Current Status and Future Trends of SiGe BiCMOS Technology", *IEEE Trans. Electron Devices*, vol. 48, p. 2575, Nov. 2001