Influence of the Ge-concentration and RTA on the device performance of strained Si/SiGe pMOS devices

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Abstract

Deep sub-micron pMOS Si/SiGe devices have been fabricated. An almost standard CMOS technology has been used for this purpose. The influence of different fabrication options like Ge-concentration and anneal conditions has been investigated. \( I_{ds}-V_{gs} \) curves show good device performance with small Short Channel Effects (SCE) even for the smallest devices.

1. Introduction

During the last few years, strained SiGe devices have gained a lot of importance ([1], [2]). The big advantage of this material is its compatibility with mainstream Si technology. This alloy of silicon and germanium offers a significant increase in device performance due to its superior transport properties as compared to silicon. Carrier mobilities are larger in Si\textsubscript{1-x}Ge\textsubscript{x} than in Si and the energy band gap of Si\textsubscript{1-x}Ge\textsubscript{x} is smaller than that of silicon and scales almost linearly with Ge-concentration [3]. Using the opportunities offered by Si\textsubscript{1-x}Ge\textsubscript{x} band gap engineering, one might be able to tackle a number of shortcomings in CMOS design.

A limiting factor for speed performance in a MOS transistor is the carrier mobility in the channel region. This is especially true for the p-channel devices since the hole mobility is intrinsically lower than the electron mobility. In strained SiGe hetero-structures, hole mobilities are strongly enhanced because of the reduced effective hole mass. Secondly, device speed in classical CMOS is also limited by the phenomenon of carrier scattering at the interface between the gate oxide and the channel. The adjustable band offsets in strained Si/SiGe systems keep the carriers away from this interface by confining them in a quantum well layer, thus forming a buried channel.

In this work, 130 nm p-channel devices have been fabricated in an almost standard CMOS technology using Rapid Thermal Anneal (RTA) conditions typically employed in advanced CMOS. Splits in Ge-concentration and junction anneal have been investigated.

2. Device fabrication

A standard Shallow Trench Isolation (STI) technique was used to isolate the device. The well implantations were done for the p-channel devices. The Si/SiGe layer stack was grown by Selective Epitaxial Growth (SEG). Selective growth of the layers is necessary in order to integrate the Si/SiGe pMOS devices with standard nMOS devices. After careful fine-tuning of the pre-epi surface preparation, using an HCl etch-back of the Si substrate prior to layer deposition, and after fine-tuning of the growth conditions, facet free epi-layers were deposited. This HCl etch has been used in order to avoid the formation of facets by modifying the height of the Si surface relative to the mask material (STI in this case). This can be seen in Figure 1. Selective epitaxial growth (SEG) conditions have been defined by adding a defined amount of HCl to the process gases to avoid deposition on the mask material. The excellent quality of the epi layers grown under selective growth conditions has been verified by Photoluminescence measurements and XTEM analysis. After epi-growth, a 2 nm NO oxide was grown as gate oxide and 150 nm undoped polysilicon was deposited. DUV lithography was used to print the gate lengths down to 130 nm.

Figure 1. Facet free epi-layer growth on standard STI wafers
For further processing of the devices standard 0.18 μm modules were used for nitride spacer formation, halo/LDD and HDD implantations. A 15nm Co/8nm Ti bi-layer was used for silicidation and an anneal of 950°C 30s or 1070°C 1s was used to activate the implantations. Planarisation layers were deposited, contact holes were etched and a standard single level metallisation process with W plugs and AlCu was used. Figure 2 shows a schematic view of the p-channel devices under consideration.

![Figure 2. Schematic presentation of the Si/SiGe devices](image)

**3. Discussion of the electrical results**

**3.1. Device performance**

Devices with a 3 nm Si cap layer, a 8 nm SiGe quantum well and a 15 nm Si buffer layer have been fabricated with dimensions down to 130 nm. As reference devices, p-channel devices with an undoped Si stack have been used for comparison. In Figure 3 the $I_{ds}$-$V_{gs}$ curves of a 130 nm Si/SiGe pMOS and its Si counterpart are shown. The devices exhibit low leakage and a good Drain Induced Barrier Lowering (DIBL) behaviour. For a gate overdrive of $V_{gs}-V_{T}=-1$ V and $V_{ds}=-1.5$ V an increase in on-state current around 15% is seen. In Figure 4 the long channel devices have been compared. In this case, an increase of about 50% was seen for a gate overdrive of $V_{gs}-V_{T}=-1$ V at $V_{ds}=-1.5$ V.

Threshold voltage behaviour is shown in Figure 5. The long channel $V_{T}$’s of the Si devices and the Si$_{0.75}$Ge$_{0.25}$ devices show a difference of 0.21 V. For the 35% devices this difference lies around 0.23 V. This is comparable with a valence band offset of 0.29 eV in the 35% case, and 0.21 eV in the 25% case.

It can be noticed that the SiGe devices exhibit a stronger Reverse Short Channel Effect (RSCE) than the Si reference devices.

![Figure 3. $I_{ds}$-$V_{gs}$ curves at $V_{ds}=-0.1$ V and $V_{ds}=-1.5$ V; $L_{poly}=0.13$ μm; a device with an undoped Si stack grown by SEG has been taken as a reference](image)

For both devices As has been used as a halo dopant. The stronger halo effect (i.e. for channel lengths shorter than 0.25 μm) is probably due to an enhancement of the As diffusion in the Si$_{1-x}$Ge$_{x}$ layers.

![Figure 4. $I_{ds}$-$V_{gs}$ curves at $V_{ds}=-0.1$ V and $V_{ds}=-1.5$ V; $L_{poly}=1$ μm; a device with an undoped Si stack grown by SEG has been taken as a reference](image)

Using the method in [5] the long channel mobility was extracted for the reference and the SiGe devices. The maximum mobility for the Si/Si$_{0.65}$Ge$_{0.35}$ devices (Figure 6) shows an increase of approximately a factor 2.1 over the Si-only pMOS devices.
3.2. Influence of the Ge-concentration

A high Ge-concentration is advantageous in order to provide a good carrier confinement. On the other hand, higher Ge-concentrations are more sensitive to high temperature budgets experienced during the processing of the devices. Strain relaxation might occur which gives rise to defect generation and degradation of the device characteristics. Two different Ge-concentrations have been studied: 25% and 35% Ge. Extracted mobilities from the long channel devices (L=10 μm) are compared in Figure 7. The enhancement in hole mobility, when going from 25% to 35%, arises because of the reduced effective mass when the Ge-concentration is increased.

The higher mobility for the 35% case gives rise to a higher on-state current for the long channel devices. However, this seems not to be true for the shorter channel devices. This can be seen in Figure 8 where the current enhancement at $V_{gs} - V_T = -1$ V and $V_{ds} = -1.5$ V is shown for both Ge-concentrations. A clear cross-over can be seen at smaller dimensions (in this case around 0.4 μm). A shorter energy relaxation time for the 35% Ge case than for the 25% Ge case might provide an explanation. As a consequence, higher Ge-concentrations might provide a better hole confinement but might not necessarily provide a higher current enhancement for smaller devices. A careful choice of Ge-concentration needs to be made dependent on the targeted channel lengths.
3.3. Influence of the anneal conditions

Closely related to the previous paragraph is the use of the RTA used for activation of the dopants. The higher the temperature budget the higher the risk for strain relaxation will be during processing. The current enhancement for the Si/SiGe devices has been monitored for two RTA conditions: 950°C 30s and 1070°C 1s.

In Figure 9 the current enhancement at $V_{gs}$-$V_T$=-1 V and $V_{ds}$=-1.5 V is shown for a 35% device and a 25% device at both anneal conditions. All devices have been normalised w.r.t. their Si counterpart processed at 950°C and 1070°C.

In the case of 35% Ge, the devices annealed at 1070°C behave slightly worse than the devices annealed at 950°C although the difference is almost negligible.

For the 25% Ge, the 1070°C shows an overall higher current enhancement as compared to the devices annealed at 950°C. This effect is seen for all channel lengths.

This can be explained by the fact that for the 35% Ge case an anneal of both 950°C and 1070°C might already induce some strain relaxation and performance degradation while this is not the case for the 25% Ge devices. In the latter case, the better dopant activation at 1070°C will increase the on-state current and the current enhancement factor. Further investigation of this behaviour is necessary.

4. Conclusions

High performance Si/SiGe devices have been fabricated down to 130 nm using a standard CMOS technology including STI isolation, Co/Ti silicidation and a CMOS compatible RTA. The influence of anneal conditions and Ge-concentrations of the buried quantum well has been investigated for both long and short channel devices. Good device characteristics with enhanced current drive and good SCE have been shown. Depending on the choice of Ge-concentrations and anneal condition a pronounced current enhancement for even the shortest channel lengths can still be observed.

5. Acknowledgements

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6. References


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