Three-dimensional Simulation of the Channel Stop Implant Effects in Sub-quarter Micron PMOS Transistors

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Abstract

The possibility to suppress the narrow channel effect due to the crowding of the leakage current near the edge of the active area in sub-quarter micrometer MOS transistors by means of a special channel stop implant has been investigated using coupled three-dimensional process and device simulation. Optimum ion implantation conditions for the suppression of the parasitic current crowding in a $0.16\ \mu\text{m}$ PMOS transistor with an arsenic doped channel were found.

1. Introduction

As it is known from two-dimensional simulations, the electrical performance of MOS transistors and especially the leakage currents are crucially dependent on the doping distribution in the active regions of the transistors. Three-dimensional (3D) simulation of the doping distributions formed in result of the technological processing used in combination with three-dimensional device simulation provides potentially a new insight into the understanding of the physical effects in small size MOS transistors. For example, coupled 3D process and device simulation allows a physically based simulation and visualisation of the distribution of the leakage currents under the gate of a transistor for a certain process flow. Measurement of such a distribution of the leakage currents inside of a small size transistors is currently impossible. An inherently 3D effect of the leakage current crowding at the edges of the shallow trench isolation (STI) leading to the narrow channel effect in small size CMOS transistors is investigated in this paper as well as the possibility to reduce this parasitic effect using an additional large angle tilted implantation step. Earlier, the suppression of the narrow channel effect using a special kind of transistor geometry was considered [1].

2. Simulation approach

STI PMOS transistors with a polysilicon gate length of $0.16\ \mu\text{m}$ and a minimal width of the active area of about $0.16\ \mu\text{m}$ were simulated. Due to the symmetry, one

half of the transistor as shown in Figure 1 was used in the 3D simulations.

Figure 1. 3D shape of the STI transistor

The 3D simulation domain contains the silicon active area, the isolation trench, and the polysilicon gate. The shape of these transistor elements was the same for all 3D simulations in which only the implantation conditions of the channel stop implantation were varied. The covering oxide layers and the gate spacers were modelled in 2D and expanded in the y-direction to build those 3D transistor elements which were specific for each implantation step. The simulation begins two-dimensionally and the 2D mode of simulation was used up to the polysilicon gate deposition. All the process steps after the gate structuring are simulated in 3D taking into account the appropriate boundary conditions. Before the 3D results of the process simulations were used in the device simulator, they have been interpolated on a new grid specially designed for electrical simulation, and the contacts as shown in Figure 1 have been added. To estimate the magnitude of the narrow channel effect, 3D simulations of the minimum width transistors have been compared to

the results of a simulation of the transistors with an infinitely large channel width. The simulation of the infinitely large channel width was performed using a 2D cut in a plane perpendicular to the x-axis through the middle of the gate of the transistor shown in Figure 1. Commercial simulation software of ISE AG (www.ise.com) and also the development version of the process simulator DIOS 3D from ISE AG which includes the new version of the 3D analytical implantation module IMP3D developed at the Fraunhofer Institute of Integrated Circuits in the projects PROMPT [2] and MAGIC_FEAT [3] were used.

3. Results

Two versions of the STI transistors are presented below, a standard one and one with an additional channel stop implantation adopted in a way that the leakage current crowding at the edge to the STI isolation is suppressed.

3.1. Process flow without the channel stop implant

At a first stage, a 2D simulation is performed in a vertical cross section parallel to the gate width. Figure 2 shows geometry and net doping at the end of the 2D part of the simulation before the gate structuring. Left is the isolation trench filled with oxide, right the active silicon area covered with a gate oxide of 3 nm thickness.

Figure 2. A fragment of the STI transistor at the end of 2D simulation after the gate oxide formation and polysilicon gate deposition

There is a small micro trench seen on the surface of the simulated area at the edge between the silicon and oxide. Such micro trenches at the edges of the active area are typical for the CMP (chemically mechanical polishing) planarised silicon wafers and they are the reason for the unwanted crowding of the leakage currents at the edges of the active areas.

The retrograde channel doping in this transistor was realised using arsenic implantation with an energy of 80 keV and a dose varied between $2 \cdot 10^{12}$ and $5 \cdot 10^{12} \text{ cm}^{-2}$,

depending on implantation conditions chosen for other implantation steps. The maximum of the arsenic profile is about 33 nm deep in silicon. Logarithmic iso-concentration levels for net-doping are drawn in Figure 2. As it is seen in Figure 2, there is a depletion of the doping concentration in silicon at the edge to the isolation trench already at this stage. The physical reason for this depletion is the non-planarity of the silicon due to the presence of the CMP micro trench. The depletion effect at sharp edges is especially remarkable, if the size of an open trench is larger than the lateral range straggling of the implanted ions. In our case the lateral range straggling for arsenic ions of 80 keV is 17.6 nm, and the lateral width of the micro-trench is about 20 nm. This results in an about 20% lower concentration of the total doping at the edge compared to the concentration in the middle of the active area under the gate at the end of 2D simulation.

The non-uniformity of the doping along the lateral direction remains also after the whole process flow has been simulated. Besides the non-uniformity in x-direction formed before the gate structuring, doping non-uniformity in y-direction under the gate comes from the pocket and source drain extension implantation steps after the gate structuring.

Figure 3. Doping distribution on the silicon surface under the gate of the PMOS transistor at the end of 3D process simulation

Figure 3 shows the doping distribution on the surface of silicon under the gate at the end of 3D process simulation. The pn-junctions to source (lower part) and to drain (upper part of the figure) are seen. The edge of the active area adjacent to the isolation is on the left hand side of the figure, the right hand side of the figure corresponds to the middle of the gate. There is a minimum of the channel doping close to the edge of the active area adjacent to the STI trench resulting mainly from the depletion of the doping on the surface of silicon due to the influence of the CMP micro-trench on the implantation

distributions because ions implanted into the micro-trench are not sufficiently back-scattered to dope the surface of the active area besides the trench.

Figure 4. Leakage current distribution on the silicon surface under the gate of a transistor for a narrow channel PMOS transistor without the channel stop implant

Figure 5. Transfer characteristics of 0.16 μm PMOS transistors with different channel widths

The distribution of the leakage currents on the silicon surface under the gate shown in Figure 4 was simulated for 1.5 V voltage applied to the drain electrode and zero voltage for all other transistor electrodes using the DESSIS device simulator. The iso-lines of the leakage current are distributed logarithmically and a number of current values in A/cm^2 are shown in the figure. The leakage current distribution shown in Figure 4 exhibits a maximum at the edge of the active area (in the left part of the figure) which is a factor of 20 larger than the current density in the middle of the channel (right part of the figure). The physical reason for the observed maximum of the leakage current at the edge of the active area is twofold, the non-uniform doping under the gate and the electric field crowding due to the gate surrounding the active area. The strongly laterally non-uniform

distribution of the leakage currents results in a significant narrow channel effect which is demonstrated in Figure 5.

Figure 5 shows a comparison of the sub-threshold transfer characteristics for a narrow channel and a wide channel transistor with the same gate length of 0.16 μm . If the threshold voltage is defined as the gate voltage at drain current of $10^{-7} \text{ A}/\mu\text{m}$, then an about 70 mV difference in the threshold voltage between the wide and narrow channel transistor due to the narrow channel effect is observed. The next section deals with conditions for the channel stop implant with the aim to suppress the narrow channel effect.

3.2. Process flow with a channel stop implant

A first idea to optimise the conditions for a channel stop implant was to choose such a tilted implantation into the wall of the isolation trench before the trench filling that just compensates the depletion of the doping in the corner of the active area adjacent to the isolation. The coupled 3D process and device simulations showed that such a channel stop implant only reduces the narrow channel effect but not completely compensates it: A somewhat overcompensating channel stop implant should be used to really suppress both the doping depletion at the edge of the active area and the effect of the field crowding at the edge.

Figure 6. Doping distribution under the gate of the PMOS transistor with a channel stop implant

An arsenic implantation with an energy of 10 keV and a dose of $2.4 \cdot 10^{11} \text{ cm}^{-2}$ and tilt angle of $\pm 80^\circ$ in a plane perpendicular to the isolation trench edge was found to be optimum for the channel stop implant in view of the suppression of narrow channel effects. Such an implant overcompensates the doping depletion in the corner of active area, but does not reduce the effective transistor width yet. The dose of the regular arsenic channel implantation was reduced for transistors with the channel stop implant to compensate for the doping con-

tribution coming onto the surface of silicon from the large angle tilted channel stop implant.

Figure 7. Leakage current distribution on the silicon surface under the gate of a transistor for a PMOS transistor with the overcompensating channel stop implant

Figure 8. Transfer characteristics of 0.16 μm PMOS transistors with different channel widths

The distribution of the doping under the gate in the narrow channel transistor is shown in Figure 6. Similar to Figure 3, twelve linearly distributed iso-concentration levels for the net-doping between $2 \cdot 10^{17} \text{cm}^{-3}$ and $4 \cdot 10^{17} \text{cm}^{-3}$ are shown. The relative non-uniformity of the net doping across the active area under the gate is somewhat reduced due to the fraction of the ions from the channel stop implant which hit the silicon surface which later appears under the gate. An extremely large tilt angle of the channel stop implant allows to put the maximum dose into the walls of the trench, minimising the dose implanted into the silicon surface in order to keep the retrograde shape of the net-doping profile which is needed to ensure the transistor performance [4].

The result of the 3D device simulation of the PMOS transistor with the overcompensating channel stop implant described before is shown in Figure 7. The distri-

bution of the leakage current under the gate of the narrow channel transistor with an overcompensating channel stop implant is much more uniform in comparison to the distribution presented in Figure 4. The maximum current density at the edge of active area is only about 50% higher in comparison to the density in the middle of the channel.

As it is shown in Figure 8 by a direct comparison of the transfer characteristics, such non-uniformity of the leakage current is tolerable and leads to a complete suppression of the narrow channel effect. Both characteristics for narrow channel and for wide channel device are nearly not distinguishable in the figure.

4. Conclusions

An overcompensating channel stop implant has to be used in order to compensate for both the doping depletion in the corner of the active area and also for the crowding of the electric field in the corner. Large angle (80°) tilted implantation for the channel stop implant allows to suppress the narrow channel effect and to preserve the retrograde shape of the channel implant because the dose per area for such a tilted implantation is much larger for the trench wall compared to the dose for the horizontal surface of the active area.

5. Acknowledgements

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6. References

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