Cost Effective Implementation of a 90 V RESURF P-type Drain Extended MOS in a 0.35 μm Based Smart Power Technology

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Abstract

This paper describes a 90 V, 300 mΩ.mm^2 RESURF P-type drain extended MOS (PDEMOS) transistor in a 0.35 μm based smart power technology.

The excellent performance of the device is realised with a dedicated Pdrift layer, designed to achieve maximum benefit from the RESURF effect. The proposed approach is very cost effective since there is only one extra mask for the Pdrift layer, no high-tilt implant (no extra mask for a Nbody) and no extra thermal budget.

1. Introduction

The integration of 80 V lateral devices into a standard CMOS technology is needed for automotive applications of the future, as the car power net will change to a 42 V battery supply [1].

Recent reports on lateral devices in submicron technologies use a large angle tilt implant (LATID) to define the body of the so-called LDMOS devices [2]. The advantages of this approach are that the body is self-aligned to the polysilicon gate edge (resulting in short channel lengths) and that no extra thermal budget is needed. The disadvantage is that two extra masks are needed in the case of complementary LDMOS transistors: one for the Pbody and one for the Nbody.

This paper describes a different approach for the P-type lateral device, where the standard Nwell will define the channel. The focus is mainly on the drift region of this device. This will be a dedicated Pdrift layer, determined by the breakdown – specific on-resistance trade-off, using the RESURF effect.

This RESURF technique is one of the most widely used methods for the design of high voltage, low on-resistance NLDMOS devices. This is the first time this technique is used for the design of a dedicated Pdrift layer for a PDEMOS, and to the best of our knowledge, resulting in the best performance for a lateral PDEMOS to date [2,3].

2. Process and Device Description

The presented PDEMOS is developed for the so-called I3T80 system-on-chip technology from Alcatel Microelectronics [4]. It is based on a 0.35 μm standard 3.3 V CMOS platform, consisting of twin retrograde wells in a low doped N-epi on a P-substrate, a thin gate oxide and dual flavoured gates. The CMOS core is extended to a smart power technology using 5 masks only: N and P buried layers, N and P sinkers and the Pdrift layer. The field oxidation is used to drive in the boron of the Pdrift layer, therefore no extra thermal budget is needed.

Figure 1 shows a cross-section of the PDEMOS device with its most important layout parameters. The most critical parameters for the on-resistance will be the Pdrift implantation dose and the layout parameters nwfi, y and t; for the breakdown voltage it will be the Pdrift implantation dose and the layout parameters y, t and z.

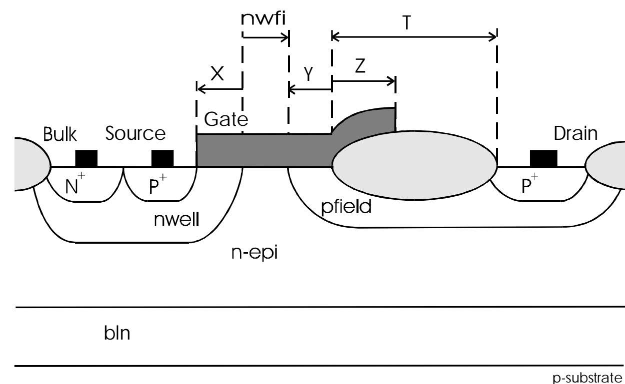

Figure 1. Cross-section of the PDEMOS and its most important layout parameters. Note the Pdrift layer (or pfield).

3. Background

The principle of the RESURF technique states that the Pdrift region must be depleted before a lateral breakdown occurs. This requirement yields an optimum RESURF dose, depending on the doping level and thickness of the Pdrift layer itself, the doping level and thickness of the N-epi and the layout parameters of the device [5]. Due to the complex correlation between these parameters, the optimisation will be a trial and error procedure.

Nevertheless, some basic observations lay severe restrictions on the nature of the N-epi and Pdrift layers. The drain side of the PDEMOS is a punchthrough diode (P+ and Pdrift/N-epi/BLN) with a breakdown voltage, which is a function of the doping level and thickness of the N-epi [6]. Thus, given the required breakdown voltage of ~ 85 V, the N-epi thickness and doping level are easily determined. The optimum Pdrift implantation dose is completely defined by the requirement set by the RESURF effect, as will be discussed in the next section.

4. Results and discussion

4.1. The breakdown voltage – specific on-resistance trade-off

The development of the PDEMOS device, together with its Pdrift layer, has been performed with the aid of TCAD simulations.

Figure 2 plots the measured breakdown voltage (V_{br}) and specific on-resistance ($R_{on,sp} = R_{on}$ x area) for three different layout variations of the PDEMOS as a function of the normalised Pdrift dose. Several conclusions can be drawn from this figure.

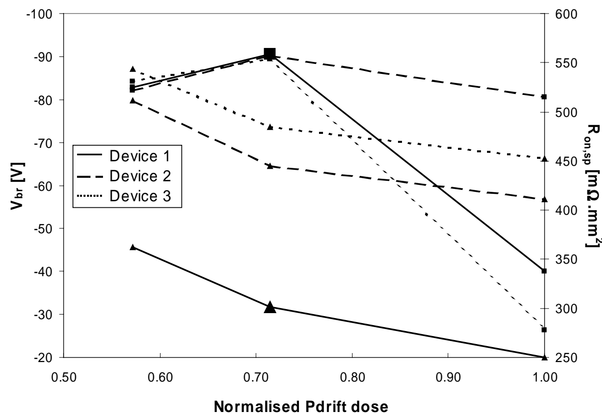

Figure 2. Measured breakdown voltage (squares) and specific on-resistance (triangles) as a function of the normalised Pdrift dose for 3 different PDEMOS devices (layout variations). The biggest data point corresponds to the best device.

First of all, the maximum achievable breakdown voltage is fully determined by the Pdrift dose. That is, of course, if the drift region and the field plate length (i.e., t and z, see Figure 1) are large enough. The $R_{on,sp}$ continues to decrease with increasing Pdrift dose, as expected. The overall decrease in $R_{on,sp}$ from Device 3 to 1 is purely layout related (parameters x, y and nwfi are optimised, t and z are held constant).

Another interesting phenomenon seen in Figure 2, is the difference in breakdown voltage behaviour for the 3 devices left and right from the optimum peak Pdrift dose. To understand this, simulations were performed on Device 3 (see Figure 2). Figure 3 plots the electrical field strength just before breakdown (V_{gs} = 0 V & $|V_{ds}| = |V_{br}|$ - 2 V) along the mid-current flowline for the 3 Pdrift doses as indicated in Figure 2. Note that this flowline is different in all three cases, its starting point is taken where the electric field starts to increase and its ending point is always at the drain contact.

For the lowest Pdrift dose, the drift region depletes too fast (therefore called the "over resurfed" device, see Figure 3) and the highest electrical fields are located near the drain. The fast upward depletion is independent of the layout of the device and explains why the breakdown voltages for all 3 devices are the same for this lowest Pdrift dose.

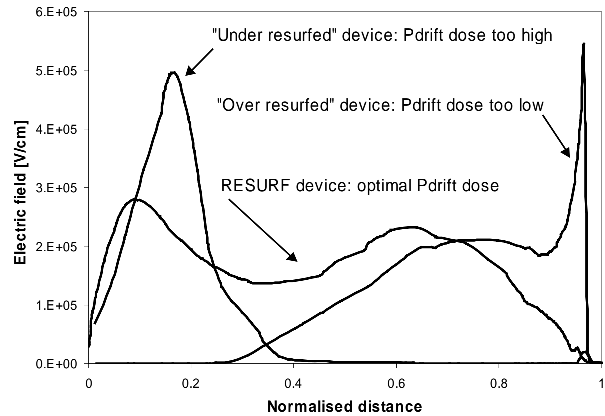

Figure 3. Electrical field just before breakdown along the mid-current flowline for Device 3 for three different Pdrift doses (see Figure 2).

At optimal Pdrift dose, Figure 3 clearly proves that the electrical field is growing at different places, resulting in the highest possible breakdown voltage. Once again, the parameters x, y and nwfi do not have an influence on this phenomenon.

An interesting trend in Figure 2 is that it seems possible to diminish the sensitivity of the breakdown voltage to the Pdrift dose (at the right of the peak), solely by changing the layout of the device. Indeed, the difference between Device 2 and the other devices is that this device has a small drift region under the gate oxide.

Figure 3 shows what happens in Device 3 for the highest Pdrift dose: one electrical field peak is growing in the drift region under the bird's beak, meaning that the RESURF effect is no longer present (therefore called the "under resurfed" device, see Figure 3). However, by decreasing the length of the drift region under the gate oxide, the breakdown voltage can be augmented to a certain extent (see Device 2 in Figure 2).

4.2. The Safe Operating Area

Until now the focus was on the $V_{br} - R_{on,sp}$ trade-off. Recent articles [7] take into account an extra parameter, the Safe Operating Area (SOA), creating a triangle of trade-offs. It is known that in RESURF devices at high current densities, the charge of the carriers can influence the depleted Pdrift region [5]. This yields a shift of the electrical field peaks towards the drain. This so-called Kirk effect, together with the possibility of a parasitic bipolar turn-on (snapback), limits the SOA.

For the PDEMOS device (see Figure 4 for the measured I_{ds} (V_{ds}) curves of Device 1), the Kirk effect is only slightly present because the drift region's doping level is high enough to resist the influence of the charge of the moving carriers. Figure 4 also shows that there is no snapback up till -90 V, resulting in a virtually rectangular SOA boundary (in DC mode).

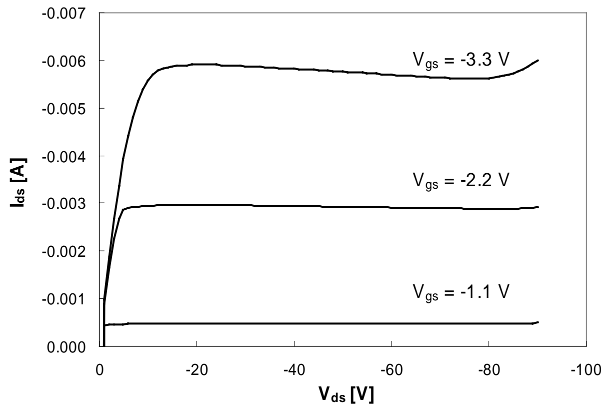

Figure 4. Measured I_{ds} (V_{ds}) characteristics for the PDEMOS (Device 1, see Figure 2).

The PDEMOS device can be forced into the Kirk effect, if the gate voltage is "accelerated" ($|V_{gs}| >> 3.3$ V). This results in higher current densities, and eventually these charges will push the region of impact ionisation towards the drain. This particular behaviour is seen when the gate current (I_{gs}) is plotted as a function of the gate voltage at several drain voltages (Figure 5).

The first peak in the gate current is due to impact ionisation near the bird's beak under the gate (see Figure 6) and the direction of the electrical field in the gate oxide above the Pdrift region, which is in favour of electron injection (see the insert of Figure 6).

As the current densities in the device increase (higher $|V_{gs}|$), the potential lines, and thus the electrical field peaks, are pushed towards the drain, and the hot electrons no longer originate in the vicinity of the gate, but at the drain (compare Figures 6 and 7). This, together with the fact that the electrical field across the gate oxide (above the Pdrift region) is becoming less favourable for electron injection (compare the inserts of Figures 6 and 7), causes the gate current to decrease. These effects are again counteracted by the even higher current densities and the global heating of the device, as $|V_{gs}|$ further increases (starting from $|V_{gs}| > \sim 2.6$ V).

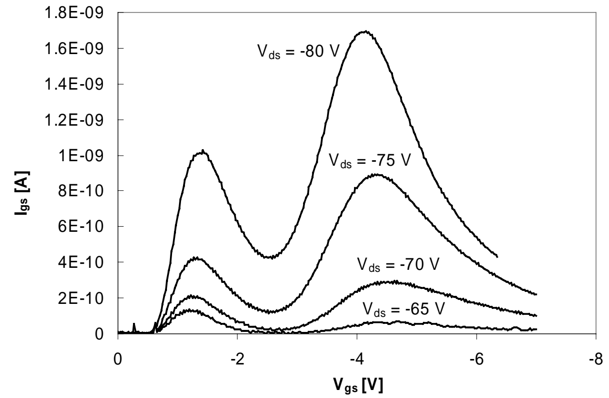

Figure 5. Measured I_{gs} (V_{gs}) characteristics for the PDEMOS (Device 1). Note that V_{gs} is forced far beyond its maximum working voltage (= -3.3 V).

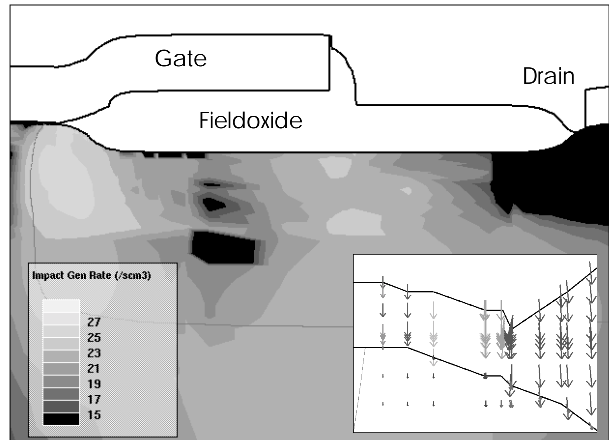

Figure 6. Simulation of the impact ionisation at $V_{gs}\sim$ -1 V and V_{ds} = -70 V (Device 1). The insert shows the electrical field in the gate oxide above the Pdrift region.

The second peak in the gate current is rather misleading, since the hole injection into the gate oxide is becoming more and more important. Indeed, simulations (Figure 8) of these gate currents show that the gate current at these elevated $|V_{gs}|$ values is the sum of hot electron (positive term) and hot hole injection (negative term). At very high $|V_{gs}|$ values, the gate current even becomes negative as the electric field across the gate oxide is growing more and more in favour of injection of hot holes (see also the insert of Figure 7).

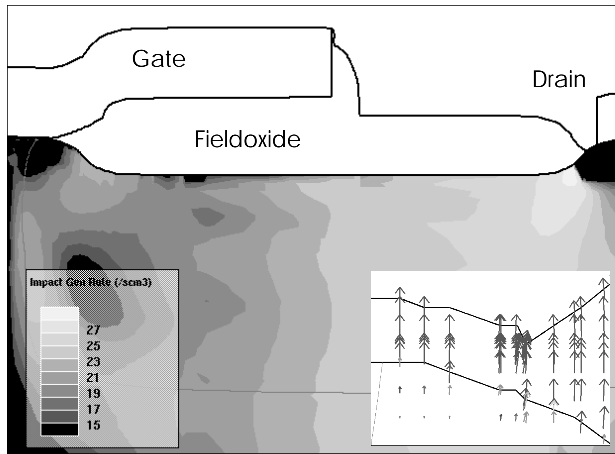

Figure 7. Simulation of the impact ionisation at V_{gs}~ -4 V and V_{ds} = -70 V (Device 1). The insert shows the electrical field in the gate oxide above the Pdrift region. Note that the electrical field has changed sign compared to the insert of Figure 6.

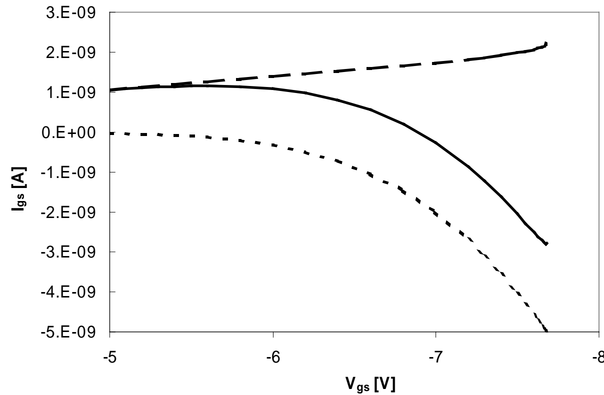

Figure 8. Simulated gate current for the PDEMOS (V_{ds} = -70 V): the dashed line is the contribution from the hot electrons, the points are the contribution from the hot holes, and the full line is the total gate current.

4.3. Degradation

The gate current is a direct measure for the carriers that are injected in the gate oxide and thus for the damage caused to the gate oxide. Therefore the maximum gate current at a real life bias (V_{gs} = -1.5 V & V_{ds} = -70 V) was chosen as a stress condition.

It has also been observed that the on-resistance is the most degrading parameter. It is therefore chosen as the monitor for degradation (see Figure 9). Figure 9 also shows that the degradation of the on-resistance of the PDEMOS obeys the conventional power law [8]: $\Delta R_{on}/R_{on\ 0} = A\ t^n$ (A = 0.44, n= 0.15). Although the stress measurements were carried out up to 1.6e5 s, no saturation was observed.

The very low value for n (whether or not saturation would occur at longer stress times) guarantees a full lifetime (25 years) at the most severe stress condition.

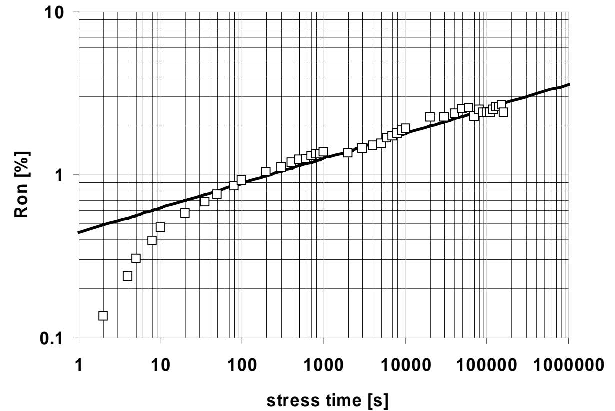

Figure 9. Degradation for the PDEMOS: Measurements (squares) and the fitted line.

5. Conclusion

It has been demonstrated that by adding one mask only in a System-on-Chip technology, P type DEMOS devices can be created, based on the RESURF principle. This approach even yields P type DEMOS devices with the best specific on-resistance – breakdown voltage trade-off ever reported to the best of our knowledge. Moreover, these devices exhibit a very wide Safe Operating Area, and no snapback or Kirk effect occurs, even at very high current densities (V_{gs} = -3.3 V and V_{ds} = -90 V). It has also been shown that the degradation of these devices is very slow.

6. References

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