Temperature dependence of the hard breakdown current of MOS capacitors

Abstract

I-V curves as a function of temperature of broken down n- and p-type MOS capacitors with different oxide thicknesses are presented. In accumulation, a crossover of the temperature dependent curves is observed. At low voltages the hard breakdown current increases with temperature whereas it decreases with temperature for higher voltages. This behaviour can be straightforwardly linked to the available charge for conduction at the electrodes. MINIMOS simulations as well as theoretical considerations were performed that clearly support this idea.

1. Introduction

As MOS devices are continuously scaled down, reliability issues are becoming increasingly important. Devices of next generations will be operated under conditions hard to withstand, this leading to a high failure probability. In this regard, understanding the mechanisms involved is therefore a key point for developing a physical-based approach to the simulation of circuits with malfunctioning devices. The most important failure mechanism in such devices is the breakdown of the gate oxide. According to the severity of the event, post breakdown characteristics of ultrathin oxides are classified as soft or hard, the latter leading to a complete local loss of the insulating property. However, due to the tiny size of the breakdown spot, the rest of the structure is expected to be scarcely altered with respect to the fresh device. In this work, we will only focus our attention on the hard breakdown (HBD) mode with special emphasis on its temperature dependence, and we will show that the associated characteristics are mainly driven by the available charge for conduction at gate and substrate. This is consistent with the general belief that the breakdown spot is a highly transparent and localized leakage path [1].

2. Experimental setup and simulation tool

For this study, we have used industry standard n- and p-type MOS capacitors with oxide thicknesses of 2.9nm and 4.4nm grown with rapid thermal oxidation (RTO). Substrate doping is about $3 \times 10^{17}$ cm$^{-3}$ and gate doping (n+) about $7 \times 10^{19}$ cm$^{-3}$. The oxides were stressed at constant current until an abrupt change in the characteristic occurred. The I-V-measurements were performed using a Keithley SCS-4200 Semiconductor Characterization system on a Karl Süss PA 200 prober bench and the temperature was controlled with aers AirCool-Chuck System SP72 in a range between 293 and 433K. MINIMOS6.1 was used for calculating the charge concentration at the interface and the potential distribution for a virgin sample in accumulation.

3. Measurements and simulations

The temperature dependence of post-breakdown I-V-characteristics corresponding to both substrate types is shown in Fig. 1.
As can be seen, the current in inversion is limited by the charge generation rate in the substrate in total agreement with the behaviour of the Fowler-Nordheim tunneling current reported in [2]. Since this generation rate increases with temperature, the current also does so for both polarities.

Under accumulation conditions the current levels exceed the ones observed in inversion by several orders of magnitude. Contrarily to what is intuitive, when thoroughly analysed, the curves exhibit a distinctive feature, namely a change of temperature dependence at a particular bias point. The effect is magnified in Fig. 2, where a clear decrease of the current slopes with temperature is seen at high voltages.

The fact that the crossovers shown in Fig. 3 are not strongly dependent on oxide thickness indicates that the thickness plays a minor role for the post breakdown behaviour. This parameter will mainly influence the potential distribution in the undamaged part of the device.

When Fig. 3 is replotted in log-log-axis, S-shaped characteristics are obtained (Fig. 4a), which are notoriously similar to the simulated electron concentration at the interface of a fresh device (Fig. 4b). The simulations also capture the temperature dependence in the whole bias range.

Moreover, when the fractional increase in current is calculated (Fig. 5a), simulations are able to reproduce the crossing in the temperature dependence (Fig. 5b). It is noted that this crossing is bounded within a narrow bias range.

Figure 2. Temperature dependence of the post breakdown I-V-characteristics for p- and n-type substrate in accumulation

This leads to the appearance of a crossover which is nearly independent of the temperature. Notice that the crossing bias not only depends on the substrate type but also on the magnitude of the current. Fig. 3 shows similar I-V-characteristics for two oxide thicknesses.

Figure 3. Temperature dependence of the post breakdown I-V-characteristics for n-type substrate in accumulation with different oxide thicknesses

Figure 4. (a) Measured I-V-characteristics plotted in log-log-scale for n-type substrate (s. Fig. 3)
(b) Simulated electron concentration at the interface of a virgin sample plotted in log-log-scale
4. Discussion

In recent years, the analysis of the post breakdown characteristics has attracted renewed interest because of the increased probability of its occurrence in ultrathin gate oxides. Despite this fact, there is a lack of physical-based models able to explain these characteristics in detail and particularly their behaviour with temperature. In view of what has been shown above, we propose that the conduction is fundamentally governed by the charge available and that the transmission properties of the leakage path across the oxide layer play a minor role. Of course, the area of the breakdown spot scales the current accordingly. Although we have used the charge concentration corresponding to a thermal equilibrium situation in an undamaged sample, it is likely that this is not the actual value at the entrance of the spot. Accurate modelling would require a self-consistent calculation between current and potential distribution in a 3D-configuration. In spite of this oversimplification, the shape of the curves can be nicely explained in terms of the majority carrier concentration in accumulation.

In a first attempt, the observed temperature dependence of the n-type samples can be obtained following the basic equations involved in the calculation of the carrier density for the non-degenerate semiconductor [3]. The intrinsic carrier density $n_i$ is given by the well-known expression:

$$n_i = (M_vM_c)^{1/2} \exp\left(-\frac{E_g}{2kT}\right)$$

(1)

where $M_v$ and $M_c$ are the effective density of states in the valence and conduction bands, respectively, $E_g$ is the energy gap of silicon in eV, which in this approach is assumed constant, $k$ is the Boltzmann constant and $T$ the temperature. The electron density in the surface charge layer reads as:

$$n = n_i \cdot \exp\left(\frac{\Phi_s}{kT}\right)$$

(2)

where $\Phi_s$ is the surface potential in eV. Combining eq. 1 and 2 gives the electron density in the surface layer as a function of temperature:

$$n = 3.02 \cdot 10^{15} \cdot T^{3/2} \cdot \exp\left(\frac{\Phi_s - E_g}{2kT}\right)$$

(3)

According to eq. 3, the electron density increases with temperature for $\Phi_s < E_g/2 \approx 0.55$eV. For a potential at the breakdown spot $\Phi_s$ higher than 0.6eV, the exponential in eq. 3 is the leading factor in the investigated temperature range and the electron concentration becomes a decreasing function with temperature. Fig. 6 shows the simulated surface potential $\Phi_s$ and oxide voltage $V_{ox}$ for an undamaged structure.

As can be seen in Fig. 6, $\Phi_s \approx 0.6$ eV is reached for $V_G > 1.5$V, which is in close agreement with the crossover voltage seen in Fig. 5a.

To further support this view, a simple expression for the current can be derived as follows. The basic equation...
for the electron current density across a barrier can be written as [4]
\[
J = \frac{4\pi q m}{h^3} \int_{E_c}^{\infty} F(E - E_{FC}) \int_0^{E-E_c} D(E-E_t) dE_t dE
\]  \tag{4}
where \(q\) is the elementary charge, \(m\) is the electron effective mass, \(h\) is Planck's constant, \(E\) is the electron energy, \(E_t\) is the energy associated with the momentum components tangential to the surface, \(F(E)\) is the well-known Fermi-Dirac distribution function, \(E_{FC}\) is the quasi-Fermi energy of the electrons, \(E_C\) is the conduction band edge, and \(D\) is the transmission probability across the barrier. Eq. 4 corresponds to eq. 2 in [1], taking into account that no electrons are available from energies in the bandgap. The current density of electrons travelling in the reverse direction can be neglected at sufficiently high gate voltages.

In the HBD mode we expect that the top of the barrier is low [1]. If it is lower than the conduction band edge \(E_C\), the barrier is transparent to all electrons in the conduction band. The transmission probability then is unity throughout the integration range of \(E_t\) (neglecting quantum reflections), and we obtain
\[
J = \frac{4\pi q m}{h^3} \int_{E_c}^{\infty} (E - E_C) \cdot F(E - E_{FC}) \, dE
\]  \tag{5}
Assuming a non-degenerate semiconductor as before, \(F(E)\) becomes the Maxwell distribution, and eq. 5 can be evaluated to give
\[
J = \frac{4\pi q m}{h^3} (kT)^2 \exp\left(\frac{\Phi_s - E_g}{2} \frac{1}{kT}\right)
\]  \tag{6}
In eq. 6, the quasi-Fermi energy has been rewritten using \(E_C - E_{FC} = -\Phi_s + \frac{1}{2} E_g\), \tag{7}
which follows from the definition of the surface potential [3]. We thus observe that the expression of the current density preserves the same exponential temperature dependence shown in eq. 3 for the electron concentration. The experimental data, analysed in terms of eq. 6, reflects this exponential dependence as seen in fig. 7, where the two curves correspond to low and high applied bias condition. Recall that eq. 6 was achieved for high voltages when the reverse current becomes negligible and that the temperature dependence of \(\Phi_s\) was also disregarded.

5. Conclusion

A thorough analysis of the post breakdown IV-characteristics of MOS capacitors has revealed interesting features which strongly correlate the measured current with the calculated carrier population at the interface and a theoretically derived expression for the current. By means of a simple model based on the fundamental equations of electron transport across a barrier as well as the equilibrium equations for the majority carrier density in accumulation, we were able to explain the anomalous temperature dependence of the post breakdown current at high bias. Even though the temperature behaviour is well captured by our derived expressions, the voltage dependence of the current requires further investigation because precise knowledge of the surface potential under breakdown conditions is necessary.

6. References