

Use of Oxynitride Dielectric to Maximise the Growth Rate of Selective Epitaxial Base Layer in a Self-Aligned Double-Polysilicon SiGe Bipolar Transistors

J. Ackaert, P. Chevalier, J.-L. Lohéac, H. Ziad, E. De Backer, M.Tack
Alcatel Microelectronics, Westerring 15, B-9700 Oudenaarde, Belgium
jan.ackaert@mie.alcatel.be

Abstract

State of the art SiGe BiCMOS processed with a double-polysilicon self-aligned Heterojunction Bipolar Transistor (HBT) is fabricated by means of selective epitaxial deposition. Typically the deposition rate of the epitaxial layer is kept very low to ensure the selectivity. This is having a negative impact on manufacturability and cost. The paper is describing the development, properties and use of a new oxynitride interpoly layer that allows an improvement of growth rate of the selective epitaxial layer by a factor 4 to 5.

This development is implemented in an industrial 0.35 μm SiGe BiCMOS technology [1].

1. Introduction

SiGe BiCMOS technology offers high-performance together with high-integration capabilities for low-noise high-speed and low-power wireless and optical communications [2]. The epitaxial growth of the SiGe base layer can be done in a non-selective or a selective way. The selective method has the advantage of producing an almost ideal self-aligned structure with reduced collector-base parasitics and then improved f_{MAX} over f_{T} ratio of the HBT device [3]. In the previous state-of-the-art the so-called interpoly dielectric layer, isolating the polybase from the subsequent polyemitter, consisted of silicon nitride. This layer withstands the wet etch during further processing, but shows a limited selectivity during the epitaxial deposition. To maintain enough selectivity, the deposition rate of the epitaxial layer has to be kept very low. This is done introducing a high flow of HCl in the gas chemistry. In addition, the nitride layer has often to be used in combination with an extra underlying oxide layer [4]. The factors mentioned above have a severe negative impact on manufacturability and processing cost. The innovation brought in our technology is the use of a PECVD oxynitride layer instead of the nitride layer to allow a much higher

deposition rate of the epitaxial layer¹. This paper is describing the development, properties and implementation of the oxynitride into the HBT interpoly dielectric layer module of a SiGe BiCMOS technology.

2. Process flow

Only the bipolar part of the BiCMOS process flow is described in this section. The process starts with the implantation of a n+ buried layer in a p-substrate followed by the epitaxy of a 1- μm n-type bipolar collector layer. After definition of the active area, a 100 nm oxide (TEOS) sacrificial layer for the epitaxy of the SiGe base is deposited and densified. A 200 nm polybase layer is deposited and implanted. The oxynitride (SiON) layer is deposited by PECVD, followed by a densification. Next the polybase/oxynitride stack is patterned and etched, stopping on the TEOS layer to open the internal base region. Phosphorous implantation of a selective collector (SIC) follows. Nitride sidewalls are formed to protect the polybase during the selective epitaxy. Then the TEOS layer is laterally wet etched under the polybase. After a HF-dip the selective growth of the base is performed in an ASM Epsilon 2000 RP-CVD epitaxy reactor. The process sequence is illustrated on figure 1.

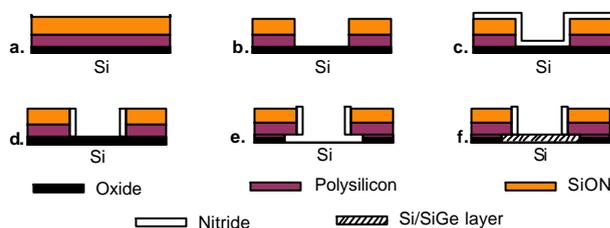


Figure 1. Process steps used in the manufacturing of the fully self-aligned SiGe HBT

A H_2 bake is applied prior to the deposition. The process gases used are H_2 as carrier gas, SiCl_2H_2 as

¹ Patent filed on July 2001 with the application number 01 401 908.7 for the European Patent Office.

silicon source, GeH_4 as Ge source, B_2H_6 as doping gas and HCl for obtaining selectivity. The SiGe layer is grown with a linearly graded profile with a targeted maximum Ge fraction of 15 %, followed by a Si capping layer of 15 nm. The top 40 nm of the epitaxial layer is boron doped with a uniform concentration of $8.10^{18} \text{ cm}^{-3}$. The first 40 nm of SiGe are not doped in order to allow boron diffusion from the base and arsenic push from the emitter, without forming potential barriers in the conduction band at the collector-base junction. SiGe and Si layers are respectively grown at 750°C and 810°C , both at 20 Torr.

Once the SiGe epitaxy is performed, a composite oxide/polysilicon inside spacer module is applied to reduce the emitter window to $0.35 \mu\text{m}$. After the oxide etch, that enlarges the emitter width to $0.5 \mu\text{m}$, a 300 nm Arsenic in-situ doped polysilicon layer is deposited to form the emitter. Polyemitter, interpoly dielectric and polybase layers are then patterned to define the bipolar device. Figure 2 shows a SEM cross-section of the finalised emitter/base region of the HBT.

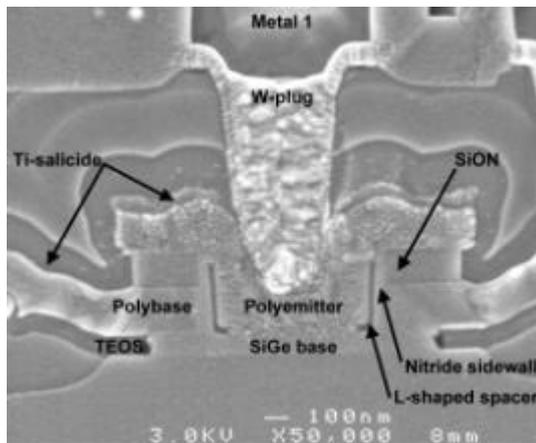


Figure 2. SEM cross-section of the emitter/base region of the HBT

3. The development, properties and use of the oxynitride interpoly layer

The interpoly dielectric film used in the self-aligned bipolar module requires the following characteristics:

- The layer should show a good selective behaviour towards SiGe deposition in the emitter window.
- The film needs to have a low stress to avoid delamination.
- The etchrate during the opening of the intrinsic base should be as low as possible.
- A good thickness uniformity over the wafer is required to ensure a low range of the electrical characteristics.

LPCVD nitride has a low etchrate but induces high stress and shows limited selectivity towards epitaxial SiGe deposition: A very low deposition rate of the SiGe is

required. PECVD oxide introduces low stress and shows high selectivity towards SiGe deposition: A high SiGe deposition rate can be used. On the other hand, this layer is etching too fast during the opening of the intrinsic base. Therefore properties of PECVD oxynitride have been explored. Several ratios between NH_3 and N_2O flows were used. The experimental conditions are represented in Table 1.

Table 1. Experimental conditions of the PECVD oxynitride depositions

Recipe	SiON35-95	SiON50-80	SiON65-65
NH_3 (sccm)	35	50	65
N_2O (sccm)	95	80	65
SiH_4 (sccm)	75	75	75
RFpower (W)	350	350	350

3.1. Selectivity of epitaxial deposition

With LPCVD nitride as an interpoly dielectric layer, the selectivity is the limiting factor for the deposition rate of the SiGe epitaxy: Only a maximum of 9 nm/min could be achieved. With the oxynitride as interpoly dielectric layer, the deposition rate could be increased by a factor 4 to 5. This is done reducing the HCl flow during the epitaxial deposition. The Ge concentration profile needs to have a 'staircase' shape. For this reason, the deposition consists of a number of small steps, each with a decreasing Ge concentration. For a process of this nature a very tight process control is required. For high deposition rates, the individual process steps become too short to ensure the required process control: The control of the epitaxial deposition itself now becomes the limiting factor in stead of the selectivity. For this reason, the maximum deposition rate is limited to 33 nm/min.

The sharp increase of selectivity can be explained by the hydrogen terminated surface of the PECVD interpoly layer. The hydrogen would reduce the Si (respectively SiGe) nucleation on the SiON, in the same way the hydrogen desorption is believed to act for the precursors in the Si-H-Cl system, i.e. as a reaction rate limiting process [5].

3.2. Stress

High stress in the interpoly dielectric layer can lead to delayering at the level of the underlying poly (see figure 3). Therefore, it was necessary to optimise the oxynitride recipe towards stress. Both, the stress as deposited and after the densification need to be considered. Figure 4 shows the stress evolution as a function of the composition of the layer.

Low $\text{NH}_3/\text{N}_2\text{O}$ ratios result in low stress both as deposited and after densification. No delayering has been observed with stress levels in between 0.2 and -0.2 Gpa.

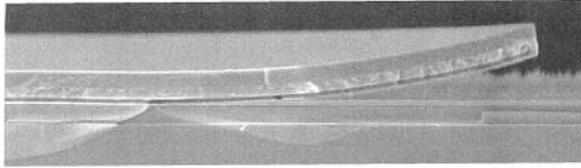


Figure 3. SEM X-section of the delayering of a high stress interpoly layer

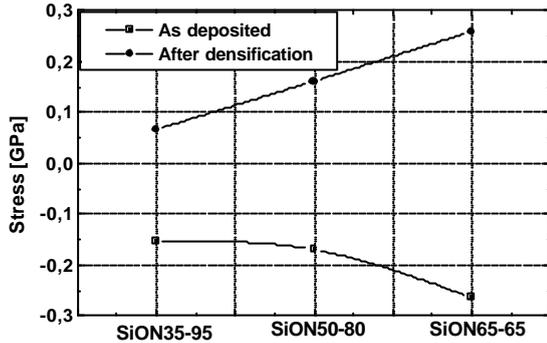


Figure 4. Stress evolution as a function of the composition of the layer as deposited and after densification

3.3. Etchrate

When the TEOS layer is laterally wet etched under the polybase, also the oxynitride layer is exposed to the etchant. The ratio of the etch rate of the oxynitride towards the TEOS should be as low as possible. A ratio less than 0.2 has proven to be acceptable in our process flow. Etch-selectivity on two oxynitrides has been measured for three etchants. The results are represented in figure 5.

1:9 Buffered HF shows the best etch selectivity of oxynitride vs. LPCVD TEOS. For this etchant, both oxynitride composition show an etch rate ratio of less than 0.2. For all etchants, SiON50-80 is etching slower than SiON35-95.

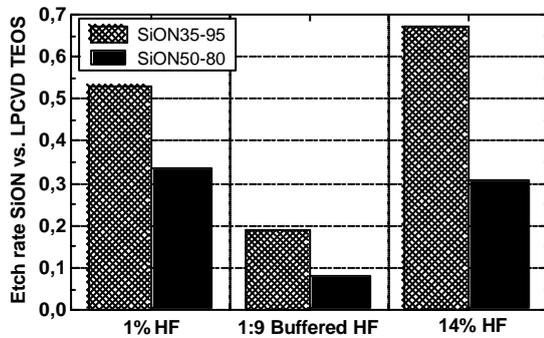


Figure 5. Etch rate ratio of 2 oxynitrides versus LPCVD TEOS for 3 different etchants.

3.4. Thickness Uniformity

Electrical properties of the SiGe HBT are very sensitive to the deposition temperature of the SiGe [4]. The thickness of the interpoly dielectric is influencing the emissivity and as such the temperature during the SiGe deposition. As a consequence, thickness non uniformity has to be limited. A range of $\pm 3\%$ was found to be acceptable.

4. Process window definition

Stress is minimal for low NH_3/N_2O ratio. The ratio of the etchrate of the oxynitride towards the TEOS should be as low as 0.2 to ensure sufficient remaining interpoly dielectric. For these reasons the composition SiON35-95 is selected. With this layer, the selectivity towards the epitaxial deposition is no longer the limiting factor for the SiGe deposition rate, The epitaxial deposition rate now is determined only by process control limitations.

In order to define the full process window, oxynitride layers of different compositions have been evaluated on stress and etch rate ratio as a function of RBS analysis results. Figure 6 shows the evolution of both the etch rate ratio between the SiON and the TEOS in 1:9 BHF, and the stress in the layer, as a function of the nitrogen content in SiON.

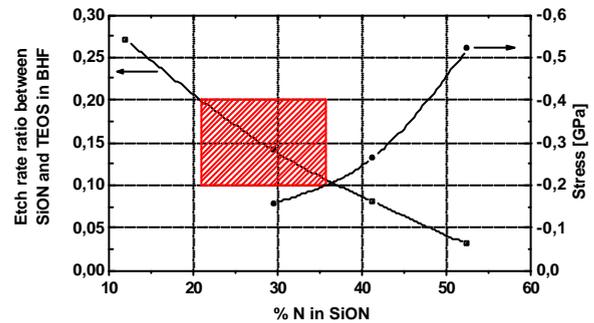


Figure 6. Etch rate ratio between SiON and TEOS and stress versus the nitrogen content (RBS) in the SiON layer. The striped area is representing the process window.

The process window limits are defined by the etch rate ratio oxynitride vs. TEOS that has to be lower than 0.2 and the absolute value of the stress that has to be lower than 0.2 GPa. Nitrogen content in the layer is therefore between 21 % and 37 %. The SiON layer that is currently used in our process is about 30 % nitrogen.

5. Performance and yield of the bipolar

The Gummel plots of a single $0.5 \times 1.7 \mu m^2$ SiGe HBT and of a yield array of 10.000 HBT devices connected in parallel are both shown in figure 7. It illustrates the good

electrical yield obtained on our 0.35 μm BiCMOS technology.

Average current gain of the HBT is 110. Good process uniformity is demonstrated by standard deviation of the HBT current gain of 8.5%. BV_{ce0} is 4.1 V and Early voltage is -125 V. f_T and f_{MAX} cut-off frequencies are respectively about 40 GHz and 85 GHz at V_{ce} of 1.5 V. The f_{MAX}/f_T ratio larger than 2 exhibits the benefit of the fully self-aligned architecture.

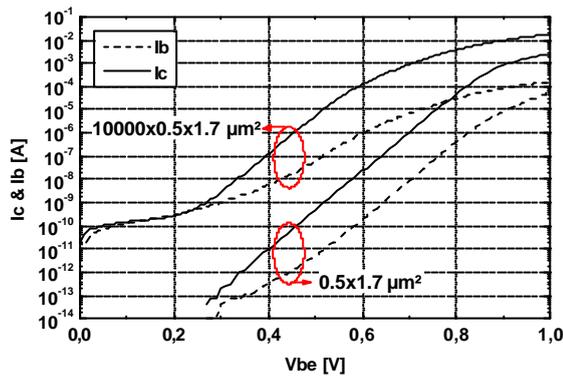


Figure 7. Gummel plots of a single $0.5 \times 1.7 \mu\text{m}^2$ SiGe HBT and of a yield array of 10,000 HBT devices connected in parallel

6. Conclusion

The manufacturability of the selective SiGe processing is significantly improved by replacing LPCVD nitride as interpoly dielectric by a single layer PECVD oxynitride layer. The composition of the oxynitride layer was chosen as a function of selectivity, etchrate ratio, and stress. This layer allows a significant improvement of growth rate of the selective epitaxial deposition by a factor 4 to 5. The oxynitride interpoly dielectric is implemented in an industrial 0.35 μm SiGe BiCMOS technology. Good electrical performance and yield have been proven.

7. Acknowledgements

The authors acknowledge the IWT and MEDEA T204 project authorities for the funding of part of this work and IMEC for the technical support.

8. References

[1] P. Chevalier, F. De Pestel, H. Ziad, M. Fatkhoutdinov, J. Ackaert, P. Coppens, J. Craninckx, S. Günçer, A. Pontiöglu, P. Tasci, F. Yayil, B. S. Ergun, A. I. Kurhan, E. Vestiel, E. De Backer, J.-L. Lohéac and M. Tack, "An Industrial 0.35 μm SiGe BiCMOS Technology for 5 GHz WLAN Featuring an Improved Selective Epitaxial Growth Process", Proceedings of 9th IEEE International Symposium on Electron Devices for

Microwave and Optoelectronic Applications (EDMO), Vienna (Austria), 15-16 November 2001, pp. 175-180.

[2] M. Soyuer, "The Impact of the SiGe BiCMOS Technology on Microwave Circuits and Systems", 30th European Solid-State Device Research Conference (ESSDERC), Cork (Ireland), 11-13 September 2000, pp. 34-41.

[3] A. Gruhle, "Prospects for 200 GHz on Silicon with SiGe Heterojunction Bipolar Transistors", Proceedings of the 2001 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Minneapolis (USA), 30 September - 2 October 2001, pp. 19-25.

[4] W. Klein and U. Klepser, "75 GHz Bipolar Technology for the 21st Century", Proceedings of ESSDERC'99, pp. 88, 1999.

[5] S. A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, 1996, p. 349.