Lithography Independent Fabrication of Nano-MOS-Transistors with 
$W = 25$ nm and $L = 25$ nm

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Abstract

The 2001 update of the International Technology Roadmap for Semiconductors predicts a printed minimum MOS-transistor channel length of 13 nm for the year 2016, which results in a physical gate length of only 9 nm [1]. The resolution of optical lithography still dramatically increases, but known and proved solutions for structure sizes significantly below 100 nm do not exist up to now. This paper presents a new method for the fabrication of extremely small MOS-transistors with a channel area down to $W = 25$ nm and $L = 25$ nm with low demands to the used lithography. It is based on our deposition and etchback technique which was used in earlier research to produce transistors with a very small channel length down to 30 nm, while the channel width was not scaled. The used technique is easily transferable to almost any other technology line and results in an excellent homogeneity and reproducibility of the generated structure size.

1. Introduction

Regarding the update of the year 2001 of the International Technology Roadmap for Semiconductors, a significantly increased scaling of the minimum MOS-transistor channel length is predicted for the next 15 years in comparison to the 1999 edition [1]. While the 1999 edition predicted a minimum channel length of 20 to 22 nm for the year 2014 [2], the 2001 update predicts a printed gate length down to 13 nm for the year 2016, which will result in a physical channel length of 9 nm.

Although the resolution of optical lithography continually increases, up to now, no solutions for mass production of transistors with structure sizes below 100 nm with the needed accuracy and reproducibility are existing [1].

In previous publications we already demonstrated a novel deposition and etchback technique which made it possible to produce transistors with a channel length down to 30 nm with excellent homogeneity and reproducibility and low demands to the used lithography [3-5]. The technique applied only conventional optical lithography. The main idea of that technique was the use of optical lithography only to define the local position of the transistors' gate electrodes, while the channel length was defined by very precise and accurate deposition and etching techniques. Unfortunately only the channel length was in the sub-100 nm-region, the channel width was limited by the optical resolution. Now we developed a new method which enables to structure both – the channel width and channel length – by the deposition and etchback technique, so real "Nano-Transistors" – transistors with a channel length and a channel width down to 25 nm – can be fabricated without high demands to the used lithography.

2. Structure Definition Process

Figure 1 shows the significant steps of the structure definition of the MOS-transistor's active area, which defines the channel width of the transistor. The cross sections were generated with the technology simulation software DIOS from ISE Integrated Systems Engineering Inc. [6]. First a pad-oxide is thermally grown and a nitride layer is deposited by LPCVD (Low Pressure Chemical Vapour Deposition) for the LOCOS technique (Local Oxidation of Silicon). These first steps are identical to the standard CMOS process. On top of these layers a sacrificial polysilicon layer is deposited and structured by conventional optical lithography (Figure 1a). The resolution of the applied lithography process is not important, because the resist mask only defines the local position of the transistor's channel area, but not the geometrical size (in this case channel width) of the transistor. The used etch process for the polysilicon layer is very anisotropic, because vertical sidewalls of this layer are very important for the deposition and etchback technique. After the removal of the resist mask a TEOS-oxide layer is deposited conformally (Figure 1b) by LPCVD and etched back anisotropically in a special RIE-Process (Reactive Ion Etching) until a spacer surrounding the sacrificial oxide layer appears (Figure 1c). Only a very slight overetch is allowed for the etchback step, else the TEOS-nano-spacer would be reduced in its height in a non tolerable manner. The next step is the removal of the sacrificial polysilicon layer in an SF$_6$-Plasma with high selectivity to all other layers followed by the transfer of the TEOS-nanostructure into the nitride and oxide layer by a high anisotropic RIE-process (Figure 1d).
If the deposition process for the TEOS-oxide is absolutely conformal and the etchback process is ideal anisotropic, the linewidth is identical to the thickness of the prior deposited TEOS-oxide layer. However, if the real processes are not absolutely conformal respectively anisotropic, the linewidth is thinner but still reproducible and exactly determined by the TEOS-oxide thickness. With our equipment the linewidth of the TEOS-mask equals 0.9 times the TEOS-oxide thickness. The accuracy and homogeneity of the linewidth is due to the well controllable layer deposition and etchback techniques very high compared to other lithography techniques for such small structures. We achieve a uniformity of ± 1.5 % over a whole 4 inch wafer and of ± 3 % from wafer to wafer.

To prevent the lateral oxidation under the nitride mask (birds beak), a nitride spacer is formed on the vertical sidewalls of the masking layers by deposition and etchback of a second nitride layer (Figure 1e). This complete structure is used as mask for the local field oxidation (Figure 1f). The width of the active area is defined by the thickness of the TEOS-oxide and by the thickness of the second nitride layer, not by any lithography. Due to the high accuracy of layer deposition techniques, sub-100 nm feature sizes with high precision and homogeneity are producible.

To generate active area structures with standard dimensions, which are needed for larger transistors or for the contact regions of the Nano-Transistors (see Figure 5 and text below), a resists mask is structured by normal lithography before the TEOS is etched back (this is not shown in the cross sections of Figure 1 and is done between the steps of Figure 1b and Figure 1c).

Figure 2 shows a SEM-photo (Scanning Electron Microscope) of the cross section after the local oxidation. In the center the active area – only 180 nm wide – surrounded by the field-oxide can be seen. The nitride layer for the masking during the local field oxidation is still on top of the active area.
After the removal of the masking layers by wet etching in hot phosphoric acid and HF-solution the gate-oxide is formed by thermal oxidation and the polysilicon layer is deposited by LPCVD. For the nano-MOS-transistors this polysilicon layer is structured with a similar deposition and etchback technique, while larger structures are masked by a normal optical lithography.

We already presented the deposition and etchback technique for the polysilicon gate electrode before [3-5]. In this case TEOS-oxide is used as sacrificial layer and nitride is used as masking layer. With the materials of the first deposition and etchback technique masking of a polysilicon layer would not be possible.

Figure 3 presents the significant steps of that structure definition technique, which defines the channel length of the MOS transistor with sizes in the deep-sub-100 nm-region and high accuracy of the line width.

Figure 4 shows a SEM-photo of a 25 nm wide polysilicon line which was structured by the presented deposition and etchback technique. The nitride line for masking that layer is still on top of the polysilicon line. The photo reveals the extreme high anisotropy of the special developed etching process for this step.

Figure 5 shows the layout of the presented Nano-MOS-Transistor. The sacrificial polysilicon layer is used for the first deposition and etchback step to define the width of the Nano-MOS-Transistor. The TEOS-mask which is used to structure the nitride-layer for the LOCOS-step is also shown. To contact drain and source of the nano-MOS-transistor larger areas are necessary, because the contact holes and the metal layer are structured by conventional optical lithography. So the
small active area of the transistor gets much wider in the contact regions. These areas with standard dimensions (around 2 µm x 2 µm big) are defined by normal optical lithography, as described before.

The sacrificial oxide layer is used for the second deposition and etchback step and defines the channel length of the nano-MOS-transistor. Larger polysilicon areas (for example the 2 µm x 2 µm large square to contact the polysilicon gate) are structured by conventional optical lithography.

The active channel region is defined by the intersection of the sub-100 nm-polysilicon-line and the sub-100 nm wide active area. All other regions are defined by conventional optical lithography and are therefore large compared to the channel.

3. Conclusion

A technique to fabricate real “Nano-Transistors” – MOS transistors with the channel length and the channel width in the sub-100 nm-region – with low demands to the used lithography has been developed. Main idea of this technique is to use optical lithography only to define the local placement of the transistor, while the channel length and width are both defined by deposition and by etching processes with a high precision in the sub-100 nm region. The standard deviation of the linewidth is about 1.5 % on a 4 inch wafer, and around 3 % from wafer to wafer. Only standard CMOS process equipment is used and only a few additional process steps compared to a standard CMOS process are necessary, so the technique is easily transferable to any other CMOS process line.

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5. References


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