Reduction of parasitic capacitance in vertical MOSFET’s by fillet local oxidation (FILOX)

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Abstract

Application of vertical MOSFET’s is hindered by the parasitic capacitance associated with its layout, which is considerably larger than for a lateral MOSFET on the same technology node. A simple self-aligned process has been developed to reduce the parasitic gate capacitance in vertical MOSFET’s using nitride fillets on the sidewalls of the trench or pillar and a local oxidation. This will result in an oxide layer on all exposed planar surfaces, but no oxide layer on the protected vertical channel area. Capacitors have been made according to the above process and it is shown that the capacitance in the trench is reduced by a factor of 10. Simulation results and analysis of the C-V measurements show that the local oxidation process has negligible influence on the oxide thickness of the vertical sidewalls.

1. Introduction

In recent years, an increasing interest in vertical transistor structures has emerged. The radically changed design enables increased packing density at a defined lithographical length as compared to standard CMOS transistors. A further advantage of the vertical layout is the improved control of the source to drain region, including the channel length. Main disadvantage of the vertical MOSFET is the large overlap capacitance of the gate with source and drain and reduction of this capacitance is a recurring theme in recent research. Gate oxide formation before selective epitaxial growth has been used in epitaxial vertical MOSFET’s [1]. A vertical replacement gate reduces the capacitance in a vertical MOSFET defined by solid-state diffusion [2]. For vertical MOSFET’s defined by ion implantation of source and drain [3], the parasitic capacitance is still considerable. The ion implanted vertical MOSFET is, however, the preferred manufacturing method since it is CMOS compatible. Reduction of these parasitic capacitances as shown in Figure 1 is of paramount importance. In this paper a simple method to reduce the parasitic capacitance in ion implanted vertical MOSFET’s is proposed and tested by means of C-V measurements [4].

2. Fillet local oxidation (FILOX)

The process developed to reduce the capacitance of the gate overlap with the active area is shown in Figure 2. The fillet local oxidation (FILOX) process is a self-aligned to grow a thin second field oxide in the active area without oxidizing the sidewalls of the pillars. The process is incorporated as follows. After etching of the pillar or trench of the vertical MOSFET, a thin stress relief oxide has been used in epitaxial vertical MOSFET’s [1]. A vertical replacement gate reduces the capacitance in a vertical MOSFET defined by solid-state diffusion [2]. For vertical MOSFET’s defined by ion implantation of source and drain [3], the parasitic capacitance is still considerable. The ion implanted vertical MOSFET is, however, the preferred manufacturing method since it is CMOS compatible. Reduction of these parasitic capacitances as shown in Figure 1 is of paramount importance. In this paper a simple method to reduce the parasitic capacitance in ion implanted vertical MOSFET’s is proposed and tested by means of C-V measurements [4].

Figure 1. A schematic of a typical ion implanted vertical MOSFET with surround gate contacted at one side. Parasitic capacitances arise from the gate track on the drain and the gate overlap with the source due to the alignment tolerance.
active area, while the vertical sidewalls of the pillar only contain the original stress relief oxide which doubles up as sacrificial oxide. After stripping of the nitride, processing of the transistors can be continued as usual. The method is hence a simple maskless process to strongly reduce the parasitic capacitance of a vertical MOSFET.

The results of Silvaco simulations of the process are shown in Figure 3. To limit the size of the bird’s beak, it is essential that the temperature of the oxidation process is high enough to allow viscous flow of the oxide to take place. The simulations mimic the experimental procedure and consist of a 20 nm stress relief (sacrificial) oxide, 70 nm nitride fillet, and a 100 nm local oxidation at 1000°C. The simulation shows that the bird’s beak extends only a few tens of nanometers laterally under the nitride fillet. It is essential that in a transistor, the drain implant should diffuse further than the bird’s beak. This can be assured by using the same nitride fillets as a mask for the implant to create a self-aligned process.

In the fillet local oxidation process as described above, the FILOX oxide will also be grown on top of the pillar since the anisotropic nitride etch exposes all horizontal surfaces. Hence, at the same time the parasitic gate-source capacitance due to the gate overlap on top of the pillar will be reduced. We have, however, de-emphasised the growth on top of the pillar, since this oxide can be easier realised by forming an insulator on the plane Si wafer before the pillar is etched. Figure 4 shows the FILOX oxidation on top of the pillar for three different scenarios. The left figure shows a bare silicon pillar, the middle figure a pillar with an 100 nm oxide thermally grown on top before the pillar etch and the right figure a stack of 20 nm stress relief oxide, 130 nm nitride layer and 50 nm low temperature oxide (LTO) all deposited before the pillar etch. The bare silicon wafer has a large variation in FILOX oxide thickness on top of the pillar and a significant thickening of the oxide on the side of the pillar. The oxide layer on top prevents this variation only partly. However, the nitride stack completely eliminates the variation of the oxide thickness in both vertical and horizontal direction. This latter process is used in device fabrication.

3. Device Fabrication

Three different processes have been applied to the pillar structures as shown in Figure 5. The first type is a basic pillar as defined by a HBr Si etch. The chosen height was 400 nm, roughly the required height to grow a 100 nm channel length ion implanted vertical MOSFET.
The pillar height has been measured with a profilometer and heights ranged from 400 nm to 450 nm for a 3 minute etch. The second type of process has an insulating stack grown on the bare Si wafer which has been etched before the Si pillar etch using the same mask. The oxide-nitride-oxide stack used was the remainder of the standard LO-COS oxidation in the active area, namely a 20 nm stress relief oxide and a 150 nm nitride layer. To protect the nitride from being etched away in subsequent processing, a 50 nm LTO has been deposited on top before the pillar etch. The third type of process incorporates both the FILOX process and the insulating stack to reduce the capacitance. After etching of the pillars in similar fashion as described for the type 2 process, a 20 nm stress relieve oxide was grown followed by deposition of a 70 nm SiO$_2$N$_x$ layer over the pillar and trenches. This layer is anisotropically etched in CHF$_3$ to leave fillets on the sidewall. A 100 nm dry (FILOX) oxide was grown using the fillets as a mask. Optical measurements showed that 60 nm of the FILOX oxide was left after removal of the stress relief oxide. The LTO on top of the pillar that protected the pillar during the anisotropic nitride etch is completely removed.

The capacitor structures consist of 40 or 50 pillar elements that have been etched into the silicon. The width of the pillar and the trenches corresponds to the minimum lithography definition of 1.5 μm. The length of the pillars was 94.5 μm, sufficiently long to neglect effects at the corners of the pillars. After growth of the gate oxide, 200 nm of 5 × 10$^{19}$ cm$^{-3}$ P-doped polysilicon has been deposited by CVD followed by a 700 nm Al(1% Si) layer.

Two different structures were tested on the wafers as shown in Figure 6. The first structure consist of the row of pillars entirely overlayed by polysilicon and metal. For the second structure, a pattern has been etched in the metal to leave 3 equidistant 8 μm stripes going over the row of pillars. Using the same masking step, the polysilicon was subsequently anisotropically etched, which left gate fillets (not to be confused with the nitride fillets) on the sidewalls of the pillars. The latter devices have hence a large proportion of the capacitance due to the sidewalls, while the former structure has most of the capacitance consisting of the horizontal surfaces of the trenches and pillars. Besides the aforementioned structures, planar capacitors were available consisting of either 20 μm wide pillars or 20 μm wide trenches to enable independent measurements of these capacitances. All contacts were made on metal pads on the field oxide and separate structures were available to correct for the influence of the pad capacitance.

The results and discussion section is as follows:

### 4. Results and Discussion

C-V measurements were performed with a HP4280A at 1 MHz. The capacitors had planar gate oxide thickness of 4.0 nm and 8.9 nm as measured by ellipsometry. Figure 7 compares the C-V characteristics for an overlay structure with basic vertical pillars, pillars with a nitride stack, and pillars with a nitride stack and the fillet local oxidation process. A strong decrease in the total capacitance in accumulation has resulted from the application of the oxide-nitride-oxide stack and the FILOX process. The pillar stack almost halves the capacitance and the FILOX process gives a reduction of a factor of five for the 4.0 nm gate oxide. The accumulation capacitances as measured at -4V (4.0 nm) and -5V (8.9 nm) are collected in Table 1.
Table 1. Capacitance values for overlay structures, fillet structures, pillar tops, and bottom trenches after correction for the pad capacitance. Also given are the calculated equivalent oxide thickness \( t_{ox} = \varepsilon_0 \varepsilon_{SiO_2} \times A/C \) of pillar tops, bottom trenches, and vertical sidewalls as deduced from the fillet structures.

<table>
<thead>
<tr>
<th>( t_{ox} ) (nm)</th>
<th>process</th>
<th>overlay (pF)</th>
<th>fillet (pF)</th>
<th>trench (pF)</th>
<th>pillar (pF)</th>
<th>trench (nm)</th>
<th>pillar (nm)</th>
<th>side walls (nm)</th>
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<tr>
<td>4.0</td>
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<td>32.4</td>
<td>44.1</td>
<td>14.8</td>
<td>14.9</td>
<td>5.0±0.2</td>
<td>4.9±0.2</td>
<td>12±1</td>
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<td></td>
<td>stack</td>
<td>18.5</td>
<td>29.8</td>
<td>14.3</td>
<td>1.9</td>
<td>5.3±0.4</td>
<td>35±8</td>
<td>11±1</td>
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<td></td>
<td>FILOX</td>
<td>7.6</td>
<td>16.7</td>
<td>1.6</td>
<td>1.7</td>
<td>50±8</td>
<td>35±8</td>
<td>12±1</td>
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<tr>
<td>8.9</td>
<td>basic</td>
<td>20.3</td>
<td>29.5</td>
<td>8.7</td>
<td>9.1</td>
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<tr>
<td></td>
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<td>49±8</td>
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</tr>
<tr>
<td></td>
<td>FILOX</td>
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<td>12.2</td>
<td>1.1</td>
<td>1.3</td>
<td>68±5</td>
<td>58±5</td>
<td>16±2</td>
</tr>
</tbody>
</table>

capacitance of the overlay structure due to the capacitance of the sidewalls in the overlay structure.

The second part of Table 1 shows the calculated equivalent oxide thicknesses of the trench structures, the pillar structures and the sidewall capacitance as deduced from the fillet structures. The gate oxide thickness derived from the capacitance measurements is slightly lower than as measured by ellipsometry. This is mainly due to the series capacitance in the accumulation region of the semiconductor (surface quantisation) as explained by Maserjian et al. [5]. The trench capacitance is reduced dramatically by the application of the FILOX process and corresponds within measurements accuracies with the measured oxide thickness of the FILOX oxide of 60±10 nm. This means a reduction of trench capacitance by more than a factor of 10. The insulating pillar stack on top has a capacitance slightly larger than calculated from the relative dielectric constant of the nitride and the stress relief oxide.

Accurate determination of the sidewall capacitance is done on the structures with the polysilicon gate fillets. To calculate the equivalent oxide thickness of the sidewalls of the fillet structure, it has been assumed that the FILOX oxidation extends under the 70 nm fillet (bird’s beak) and that the gate fillets are 150 nm thick on the bottom (original polysilicon gate deposition was 200 nm, but resistance measurements along the gate fillets indicate an slight overetch). The thickness is considerably larger than the gate oxide thickness. Part of this discrepancy is due to the fact that pillars are etched with their sidewall facing the <011> direction and that the gate oxide is expected to grow faster in this direction than in the <100> plane of the wafer. Recent measurements in the context of vertical MOSFET’s show an increase in oxidation rate of a factor of 1.4 [6]. This gives an expected value of the sidewall oxide of 5.6 and 12.5 nm for the planar gate oxides of 4.0 and 8.9 nm, respectively. The thickness of the gate oxide on the sidewall could further be explained by assuming that the sacrificial oxide has not been removed completely from the sidewalls before gate oxidation.

Nevertheless, it is clear from the comparison of the sidewall oxide thickness for the FILOX process with the basic vertical process and the stack process that the fillet local oxidation does not lead to extra oxide on the sidewalls. It can thus be concluded that the nitride fillets have given a good protection during the local oxidation. Fabrication of MOSFET’s and TEM graphs with the FILOX process incorporated are under way. However, a preliminary conclusion can be made that the FILOX process provides a simple self-aligned method to reduce the parasitic capacitance in vertical MOSFET’s.

![C-V measurements for overlay structures for 4 nm gate oxide. Curves are given for the three different processes: basic, with oxide-nitride-oxide stack, and with oxide-nitride-oxide stack and FILOX process.](image)

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