On the Origin of the 1/f$^{1.7}$ Noise in Deep Submicron Partially Depleted SOI Transistors

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Abstract

Results are presented of a systematic low-frequency (LF) noise study of deep submicron transistors processed in a 0.1 μm partially depleted (PD) Silicon-on-Insulator (SOI) technology. The focus is on a particular kind of noise, which is termed 1/f$^{1.7}$ noise, due to the frequency dependence of the noise amplitude. It dominates at the low frequency part of the spectrum in linear operation, for a wide range of gate biases. The observed bias and device length dependences lead to the conclusion that the underlying fluctuations are generated by traps in the gate oxide. It is furthermore shown that the noise is not found for the back-channel transistor and is most likely not related to the gate current. As argued, a possible origin of such a 1/f$^{1.7}$ noise is carrier trapping and release from oxide traps in the 2.5 nm NO oxide, which are related to the polysilicon gate/oxide interface.

1. Introduction

Deep submicron Silicon-on-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) has proven its merits for RF/analog applications [1],[2]. However, one of the important aspects to deal with is the low-frequency (LF) noise on a device and circuit level. From the past, it is known that partially depleted (PD) SOI transistors suffer from some specific excess noise sources. By now well known is the excess noise associated with the floating body kink effect [2]-[5], which manifests itself as a Lorentzian-like additional component in the noise spectrum, for sufficiently large drain bias V_{DS}. A similar type of spectral density is associated with the thermal noise of the body resistance, which shows up both in the ohmic and the saturation regime [6]. In subthreshold operation, on the other hand, the floating body latch phenomenon induces extra 1/*f* or flicker noise [7]. Finally, it has been shown that the defectiveness/quality of the silicon film can play an important role in the noise performance of the transistors made in it [8]-[10]. The presence of defects, resulting from the SOI fabrication process, may lead to the appearance of Generation-Recombination (GR) noise.

Here, a new kind of noise will be described, occurring in 0.1 μm PD SOI p- and n-channel transistors with 2.5 nm nitrided oxide gates, which is characterised by a 1/f^n spectrum with n~1.7, therefore called "1/$f^{1.7}$ noise". It has been seen in the ohmic regime for the front channel, but is absent in the back-channel transistors. The length (L) dependence of both the drain current (S_I) and gate-referred power spectral density (S_{VG}) will be described, from which the origin of the noise source is discussed in terms of a number-fluctuations model.

2. Experimental

The devices studied have been processed in a 0.1 μm PD SOI technology on 200 mm UNIBOND wafers. The final film thickness is 100 nm and the buried oxide thickness 400 nm. A Polysilicon Encapsulated Local OXidation of Silicon (PELOX) isolation scheme was applied to define the active areas. The gate stack consists of a 2.5 nm NO oxide and a 150 nm polysilicon layer. Two wafer splits have been studied either with or without (abbreviated no) a HALO implantation, to control the short-channel effects.

N- and p-channel transistors with a fixed width W=10 μm and a drawn gate length L ranging from 0.15 to 10 μm have been evaluated applying a drain bias V_{DS}=25 mV in absolute value. They share a common gate and source contact. The channel current I was changed from 0.04 to 40 μA, while the noise spectrum has been evaluated in the frequency (f) range from 0.7 Hz to 100 kHz.

3. Results

Typical spectra for the n- and p–channel devices are represented in Figs 1a and 1b, corresponding with a gate voltage V_{GS} varying from below to above threshold V_{th}. The gate overdive voltage V_G* is defined by V_{GS}-V_{th}. In the range 0.7 Hz≤f≤50 Hz one can see that the spectrum has a 1/$f^{1.7}$ character, which is rather unusual. In fact, the frequency index 1.7 remains constant in the gate voltage range studied for the no-HALO n-MOSFETs, while it changes from n=1.7 in weak inversion to n=1.1-1.2 in strong inversion for the no-HALO p-MOSFETs. A similar variation of n has been observed for the HALO n- and p-MOSFETs.

It should be noted that besides the $1/f^{1.7}$ component, also the standard $1/f^n$ noise with n close to 1 has been found for the intermediate frequency range for $L \leq 1$ µm (see Fig. 1a). The white noise part occurring at higher frequencies corresponds with the Nyquist noise of the parallel connected channel and load resistances. For the remainder of the paper, the focus will be on the low-frequency $1/f^{1.7}$ noise.

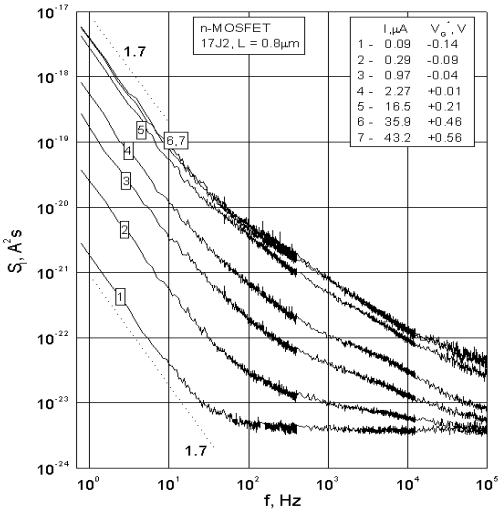

Fig. 1.a. Front-channel drain current noise spectra measured for a 0.8 µm no-HALO PD SOI n-MOSFET. Zero back-gate bias V_{GB} was applied.

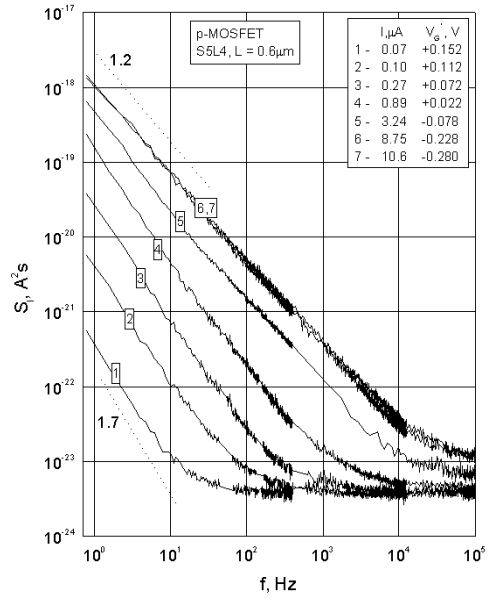

Fig.1.b. Front-channel drain current noise spectra measured for a 0.6 µm no-HALO PD SOI p-MOSFET. Zero back-gate bias V_{GB} was applied.

In order to emphasise the typical character of the $1/f^{1.7}$ noise, Figs 2a and 2b compare the spectra for a L=10 µm no-HALO n-MOSFET. While the front-channel clearly exhibits the $1/f^{1.7}$ noise, spectra with a smaller n are found in the back-channel results of Fig. 2b.

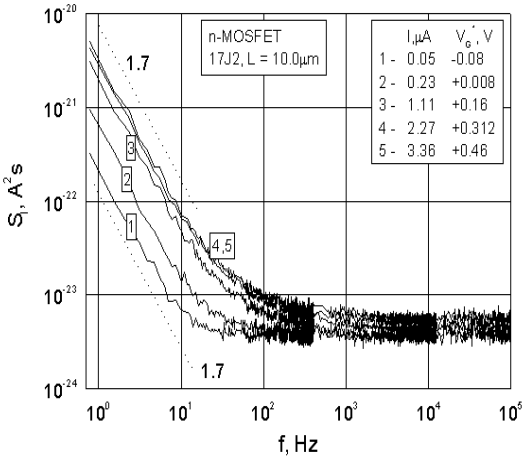

Fig. 2.a. Drain current noise spectra measured for a 10 µm no-HALO PD SOI n-MOSFET in the front channel. V_{GB}=0 V.

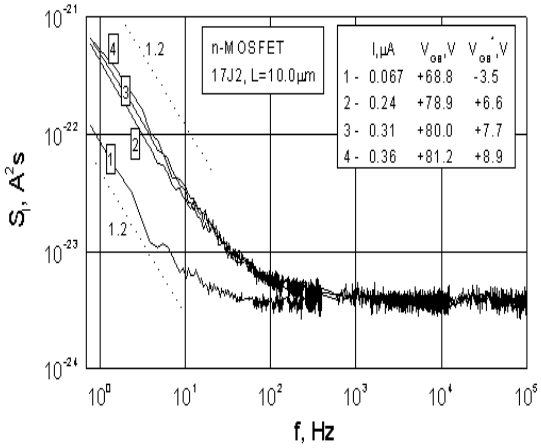

Fig. 2.b. Drain current noise spectra measured for a 10 µm no-HALO PD SOI n-MOSFET in the back channel.

The dependence at f=1 Hz of the current noise spectral density S_I on the gate overdrive voltage V_G* is illustrated in Fig. 3a, for no HALO n-MOSFETs, while Fig. 3b compares LxS_{VG} versus V_G* for n-MOSFETs with and without HALO. The input-referred noise power spectral density S_{VG} has as usual been obtained from S_I/g_m^2, with g_m the device transconductance. The following conclusions can be drawn. S_I increases with increasing gate overdrive voltage until saturation sets in. The saturation value $(S_I)_{sat}$ decreases with increasing L according to an L^{-3} law. In weak inversion, S_I increases proportionally to I^2. Second, the LxS_{VG} product is independent of the gate overdrive voltage or device

length and is a factor ~1.8 higher for the no HALO n-MOSFETs, i.e., 4.5×10^{-14} $V^2 cmHz^{-1}$ versus 2.5×10^{-14} $V^2 cmHz^{-1}$.

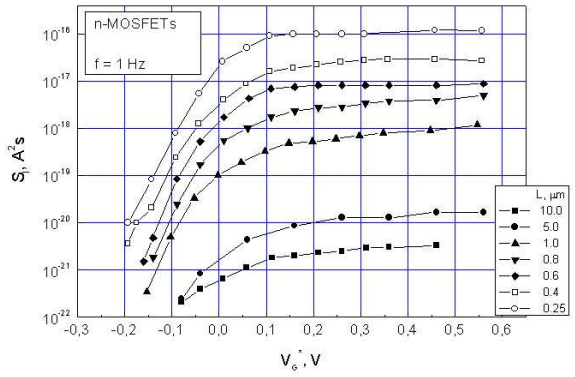

Fig. 3a. Dependences of S_I on gate overdrive voltage for f=1 Hz and no HALO PD SOI n-MOSFETs, corresponding with different length.

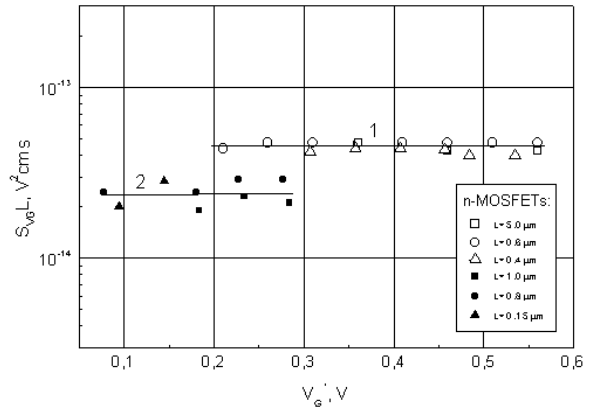

Fig. 3b. Dependences of $L \times S_{VG}$ on gate overdrive voltage at f=1 Hz for no-HALO (1) and HALO PD SOI n-MOSFETs (2).

4. Discussion

Based on the trends of Figs 3a and 3b, some conclusions can be drawn with respect to the nature of the reported $1/f^{1.7}$ noise. The scaling of S_I with $\sim I^2$ in weak inversion, the saturation of the dependence of $S_I(V_G^*)$ in strong inversion, the variation of $(S_I)_{sat}$ with $1/L^3$ and the independence of $S_{VG}L$ of L and V_G^* are all strong arguments in favor of a McWhorter or trapping related noise. In other words, it is strongly believed that carrier trapping-detrapping through oxide traps is responsible for the observed LF noise. In addition, based on Fig. 2b, it is concluded that the behaviour is typical for the thin (2.5 nm) front gate NO oxide. The question arises, however, why no standard $1/f$ noise is obtained below 50 Hz?

Before tackling this question, it should be ruled out that the observed noise is not generated by the gate current. Due to the common gate contact, a significant gate current I_G flows. It is well-known that I_G in deep submicron transistors can be a source of $1/f$ or Random Telegraph Signal (RTS) noise [11]-[12], especially for larger gate areas. Therefore, the LF noise in the front-gate current has been evaluated, whereby the source, and drain contacts of all the p-MOSFETs of the common-gate array were grounded. In this way, all the devices are connected like MOS capacitors in parallel. The corresponding spectra, for a gate bias V_G varying between –0.025 and –0.5 V are represented in Fig. 4. The spectra have clearly a slope n which is significantly smaller than 1.7, with evidence of GR humps for most biases. From this, one can derive that the gate current is most likely *not* at the origin of the $1/f^{1.7}$ front channel noise.

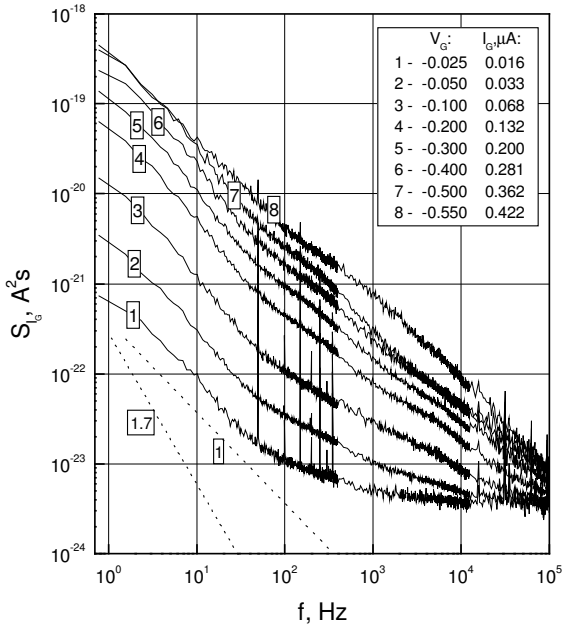

Fig. 4. Gate current noise spectra for a set of common-gate, common-source p-MOSFETs, biased as a parallel MOS capacitor.

Having established the trapping origin of the noise under investigation, the remaining problem is to explain the large frequency exponent $n \geq 1.2$. In fact, it has been shown in the past that an n significantly different than 1 could be explained by a trap concentration profile [13]. Such a profile could be the result of the nitridation treatment, which introduces a peak concentration of N and N-related oxide traps close to the interface [13]. In order to evaluate this hypothesis, the following formula for the noise can be used:

$$S_{VG}L = \frac{q^2 D_{ot} kT}{4WC_{ox}^2 (2\pi f)^2 \tau} \qquad (1)$$

In equation (1), q is the electronic charge, D_{ot} is the oxide trap density (in $cm^{-2}eV^{-1}$), k is Boltzmann's constant, T the absolute temperature, C_{ox} is the oxide capacitance per cm^2 and τ the characteristic trap time constant. From the experimental lower frequency limit of $\leq$0.7 Hz, a maximum τ of $\geq$0.2 s can be derived. The corresponding oxide trap density is in the range of $\leq 2.4 \times 10^{12}$ $cm^{-2}eV^{-1}$. For the high frequency limit of 50 Hz, a 70 times lower trap density results, which supports the idea of a fairly steep trap density profile, over a short oxide depth.

The depth information (z) can be obtained by assuming that the trap time constant is due to tunneling, which results in an equation of the form [13]:

$$\tau = \tau_0 \exp(2\alpha z) \qquad (2)$$

with α a tunneling parameter in the range of 10^8 cm^{-1} and τ_0 the minimal trapping time through tunneling for traps close to the interface, in the range of 10^{-10} s. Based on the maximum τ value corresponding with a frequency of 0.7 Hz yields a depth z in the range of 53 nm from the $Si-SiO_2$ interface. This is much deeper than for typical border traps (1 to 2 nm), which dominate the $1/f$ noise in MOSFETs. In addition, it is derived that over a small distance, the underlying trap density reduces by about two decades, for increasing depth from the gate/oxide interface. The fact that the $1/f^{1.7}$ noise is absent in the back channel spectra and also in the noise of 3.5 nm gate oxide bulk MOSFETs, suggests that the traps are most likely associated with the polysilicon gate/oxide interface.

Another important conclusion is that – if this interpretation is right – the study of such a noise allows to gain information on the traps which are close to the gate interface. This feature is unique for thin-gates and should be observable in other devices (e.g. bulk transistors) as well. In this respect, it can be noted that in a recent paper, a technique based on the study of the gate current - gate voltage characteristics has been proposed for assessing the traps at the polysilicon gate-oxide interface in thin-oxide (e.g. 2.5-3.9 nm) MOS devices [14]. Typical detrapping time constants are in the range of a few seconds, which is in line with the range of time constants reported here. Furthermore, the de-trapping time reduces for thinner gate oxides. A possible origin may be processing induced damage [14].

5. Conclusion

In summary, a new type of LF noise has been observed in 2.5 nm NO gate PD SOI MOSFETs, which occurs in the 0.7-50 Hz frequency range and is characterised by a $1/f^{1.7}$ spectrum. It is proposed that the origin of this noise is related to carrier exchange between the channel and oxide traps, which are related to the polysilicon gate interface. The high frequency exponent can be explained by assuming that the traps show a rather steep concentration profile, which decays when moving away from the gate interface.

6. References

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