Simulation and Modeling of Nanocrystalline Silicon Thin Film Transistors

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Abstract

We study the behavior of nanocrystalline hydrogenated silicon (nc-Si:H) thin film transistors (TFTs), and we present a physically based analytical model for these devices suitable for implementation in circuit simulators such as SPICE. The model is based on existing models for amorphous silicon thin film transistors, which have been extended to account for observed physical phenomena in nc-Si:H TFTs. The proposed model shows good agreement with experimental data.

1. Introduction

Thin-film transistors are used as switching elements in large area electronics. Usually, amorphous hydrogenated (a-Si:H) or polycrystalline hydrogenated silicon (poly-Si:H) are used as channel materials. The advantage of the a-Si:H is the possibility for deposition over large surfaces at relatively low deposition temperatures (below 450°C). Nevertheless this material suffers degradation under illumination and under bias stress. The use of poly-Si:H solves this problem, but high temperatures are used for crystallization of the a-Si:H material and expensive substrates are required.

Nanocrystalline hydrogenated silicon have been proposed as promising alternatives to a-Si:H and poly-Si:H [1-3]. Their major advantage is the possibility to be deposited over large area at very low deposition temperature (120 °C). At the same time they present improved stability under illumination and bias stress compared to the a-Si:H [1, 4]. These qualities make nc-Si:H attractive for the fabrication of high quality inexpensive TFTs.

An accurate analytical model for these new transistors is a prerequisite for utilizing the devices in a circuit context. In this work, we present an analytical model for nc-Si:H suitable for implementation in SPICE [5]. The paper is organized as follows. First we present the nc-Si:H properties which are important for the operation of the TFTs. Then we compare our experimental characteristics to the existing model for a-Si:H TFTs. Afterwards, with the help of numerical simulations (using SILVACO Atlas), we analyze the physical phenomena responsible for the different operation regimes of the nc-Si:H TFTs, and we propose a new model related to this phenomena. Finally we demonstrate the agreement between our model and experimental data for nc-Si:H TFTs.

2. Nanocrystalline TFTs

The nc-Si:H materials are polycrystalline hydrogenated layers with grain sizes of a few nanometers [3]. The grain boundaries have amorphous-like structure and the high density of defect states (DOS) is responsible for the TFTs behavior. In this paper we analyze the characteristics of TFTs with the channel material consisting of hydrogenated silicon with grain size of 8 nm and deposited by the hot-wire chemical vapor deposition (HWCVD) technique [6,7]. Our TFTs have an inverted staggered structure with thermal grown SiO₂ for gate insulator and aspect ratio W/L = 2.5 [3].

3. Analytical Device Model

Recently, analytical models for both a-Si:H and poly-Si:H TFTs were developed [5] and implemented in several circuit simulators including Eldo, HSPICE and AIM-Spice [8]. We base our model on the a-Si:H TFT model presented in [5]. In Fig. 1-3, we have compared experimental curves of our device to this a-Si:H TFT model. As we note from Fig. 1-2, the modeled curve is in good agreement with the experimental for gate voltage VGS of about 17V. For VGS above this value there is a significant increase of the experimental drain current that is not reproduced by the model.

To achieve a better understanding of this effect, we studied the behavior of the TFT transconductance gm = dIdsg/dVGS. In Fig. 4 we compare the measured and modeled (using the model of [5]) transconductance. The measured transconductance is in good agreement with the modeled for VGS lower than 17V. Above VGS = 17V...
there is a dramatic increase of the transconductance. This phenomenon can not be explained by the a-Si:H TFT model [5], which describes the above threshold regime with the following equation:

\[ I_{av} = \mu_{eff} C \frac{W}{L} V_{DSE} (1 + \lambda V_{DS}) V_{GT} \]  

(1)

where \( \mu_{eff} \) is the carrier’s field effect mobility, \( C \) is the gate insulator capacitance, \( V_{DS} \) is the drain-source voltage, \( \lambda \) is a parameter describing the gate-length modulation effect, and \( V_{DSE} \) and \( V_{GT} \) are continuous functions giving, respectively, the effective drain-source voltage and the gate voltage overdrive.

**Field – Effect Mobility in nc-Si:H**

In a-Si:H TFTs the field effect mobility \( \mu_{eff} \) is dependent on the acceptor-like tail states in the a-Si band gap [9]:

\[ \mu_{eff} = \mu_n \frac{n_{free}}{n_{free} + n_{trapped}} \]  

(2)

where \( \mu_n \) is the band mobility, \( n_{free} \) is the concentration of the free induced electrons, \( n_{trapped} \) is the concentration of the trapped in defect states electrons. In a-Si material \( n_{free} < n_{trapped} \). Both \( n_{free} \) and \( n_{trapped} \) increase with increasing of the gate voltage, and the factor \( n_{free}/(n_{free}+n_{trapped}) \) is almost independent of the gate voltage. This is why for above threshold regime in the a-Si TFTs model, \( \mu_{eff} \) is defined as a weak function of the gate-source voltage [5].

For elevated gate voltages two new regimes were defined for a-Si TFTs: the transitional regime and the crystalline-like regime [9]. In the transitional regime the tail states at the a-Si:H/insulator interface are almost completely filled and the Fermi level touches the bottom of the conduction band. The fraction of \( n_{free} \) at first small, increases with the increase of \( V_{GS} \). At higher \( V_{GS} \) the traps are completely filled, \( n_{trapped} \) remains constant and \( n_{free} \) increases with increasing \( V_{GS} \). Similarily to crystalline MOSFET (“crystalline-like regime” [9]):

\[ n_{free} \propto \frac{C}{q} (V_{GS} - V_n) \]  

(3)

where \( V_n \) is the gate voltage in transitional regime which we call “transitional voltage” according to [9] and \( q \) is the electronic charge. In [9] the corresponding regime is called “crystalline-like regime”. According to eqs. (2) and (3) the field effect mobility becomes linearly dependent on the gate voltage:

\[ \mu_{eff} = \mu_n M (V_{GS} - V_n) \]  

(4)

where \( M \) is linear-dependence coefficient. The field-effect mobility \( \mu_{eff} \) will increase with increasing \( V_{GS} \) until \( n_{free}/(n_{free}+n_{trapped}) \) \( < 1 \). When \( n_{free} >> n_{trapped} \) the factor \( n_{free}/(n_{free}+n_{trapped}) \) \( \approx 1 \) and \( \mu_{eff} \approx \mu_n \).

Substituting eq. (4) in eq. (1) will lead to quadratic dependence of the drain – source current of \( V_{GS} \). For a-Si:H TFTs the latter regime is supposed to occur at very high gate voltages (about 100V). The transition to crystalline-like regime has not been taken into account in the SPICE model for a-Si:H TFTs because this transitional voltage is too high for all practical matters. However, lower density of the tail states should facilitate the transition to crystalline-like regime at lower gate voltages. In nc-Si:H the DOS is lower than in a-Si:H because of the higher internal atomic order. This is why, in nc-Si:H TFTs, we can expect that the transition to crystalline-like regime occurs at significantly lower gate voltages than in a-Si TFTs.

In order to confirm this hypothesis, we performed numerical simulations using SILVACO Atlas [10]. We simulated the behavior of nc-Si:H TFTs at different bias conditions and with several values of the characteristic decay energies, WTA (i.e., different densities of acceptor-like tail states). In Fig. 5, we show the evolution of the free and trapped carrier concentration with the gate voltage. The free electron concentration becomes relevant at values of \( V_{GS} \) much lower than in purely a-Si:H, and becomes higher than the trapped electron concentration at about \( V_{GS} = 31 \) V. Our numerical simulations showed that \( n_{free}/(n_{free}+n_{trapped}) = 0.6 \) at \( V_{GS} = 40 \) V. Replacing this value in (2), and using the extracted value of \( \mu_{eff} \), the estimated value of \( \mu_n \) is in order of \( 1 \) cm/Vs which is typical for a-Si:H material. This value confirms that grain boundaries are responsible for the material properties.

In Fig. 6 we show the simulated transconductance vs. \( V_{GS} \) of nc-Si:H TFTs for different values of WTA. The corresponding DOS shapes are shown in Fig. 7. For high values of WTA the shape of \( g_m \) approaches the typical behavior in a-Si:H TFTs. However, at lower WTA (i.e., lower density of tail states) we observe a large increase of \( g_m \) with \( V_{GS} \) after a regime of slow increase of \( g_m \) with \( V_{GS} \). This is actually the \( g_m \) behavior we found in our transistors. A lower density of tail states implies a higher grain size. We conclude that the nanometer grain size is the responsible for this unique behavior of nc-Si:H TFTs in the normal voltage range.

For materials with larger grain size the trap concentration is significantly lower and the increasing of \( \mu_{eff} \) with \( V_{GS} \) begins at much lower gate voltages and is much sharper. Actually, in Fig. 6, we do not observe any change of behavior in the above-threshold \( g_m \) at high values of the grain size. The behavior of \( g_m \) is similar to the observed one in poly-Si TFTs. The existing poly-Si TFT model [5] describes adequately this behavior.

**Drain Current Equations**

Our experimental characteristics show that at \( V_{GS} =17 \) V the channel current changes from linear to quadratic dependence of \( V_{GS} \). We conclude that in our device, \( V_n \) is 17 V. As expected this is considerably lower than for a-Si:H TFTs. For \( V_{GS} > V_n \), quadratic-dependent component of the current appears near the a-Si:H/insulator interface and adds to the linear-dependent current away from the surface as it was confirmed by our numerical simulation. We have consequently modified the existing a-Si:H TFT SPICE model to obtain an appropriate model for nc-Si:H. As the a-Si:H TFT model
is in good agreement for subthreshold regimes, our modifications affect only the equations for $I_{DS}$ above threshold. For gate voltage below $V_G$ the above threshold drain current in linear region is linearly dependent on $V_{GS}$. Using eqs. (1-4), we introduce new equations for describing the quadratic-dependent current component:

$$I_{tr} = \frac{1}{2} \mu_o C \frac{W}{L} V_{DS} \left(1 + \lambda V_{DS}\right) M \cdot V_{Gtre}^{2+D} \quad (5)$$

$$V_{Gtre} = V_{th} \left[1 + \frac{V_{Gtre}}{2V_{th}} \right]^2 + \frac{\left(V_{Gtre} - V_{th}\right)}{2V_{th}} \quad (6)$$

where $V_{Gtre}, V_{DS}, V_{th}$ is thermal voltage and $\delta$ is a transition width parameter which ensures the good behavior of $V_{Gtre}$. According to (6) $V_{Gtre} = V_{Gtre}$ when $V_{Gtre} \geq V_{tr}$, as it should, and if $V_{Gtre} < V_{tr}$, $V_{Gtre} = 2V_{th}$, making $I_{tr}$ negligible, as it should. Therefore, three new parameters are incorporated to the model: $V_{tr}, M,$ and $D$, which is a correction coefficient. Our new model permits simulating of purely amorphous Si TFTs, setting $M=0$.

We use the following unified expression of the channel current, which smoothly tends to the desired expression in each operating regime:

$$I_{DS} = I_{look} + \left(\frac{1}{I_{sub}} + \frac{1}{I_{sub} + I_{tr}}\right)^{-1} \quad (7)$$

where $I_{look}$ and $I_{sub}$ are, respectively the expressions of the leakage and subthreshold current given in [5], and $I_{sub}$ is the linear above threshold contribution given in (1). Therefore, according to (7), below threshold, $I_{DS} = I_{look} + I_{sub}$ and above threshold, $I_{DS} = I_{sub} + I_{tr}$. The channel current expression, (7), has an infinite order of continuity, which is very desirable in circuit simulation.

The modeled $I-V$ characteristics agree very well with the experimental data below and above threshold (Fig. 1, 2 and 3). In Fig. 4 we compare the experimental and the modeled transconductance. Again, we note that the experimental data is well described by our new model.

4. Conclusions

We have presented a new model for the promising nanocrystalline silicon TFTs, based on an existing model for amorphous silicon TFTs. By studying the physical properties of the new materials with the help of numerical simulations, we developed a new model that accurately reproduces experimental $I-V$ characteristics of nc-Si TFTs. The new introduced parameters allow the simulation of TFTs made by large variety of materials from amorphous to microcrystalline materials with small-grain size. Our new model will ease the introduction of nc-Si:H TFTs in industrial applications.

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6. References


Fig. 1. Experimental and modeled $I_{DS}$-$V_{GS}$ characteristics (in linear scale) using the a-Si:H model [11] and the proposed nc-Si:H model.
Fig. 2. Experimental and modeled $I_{DS}$-$V_{GS}$ characteristics (in logarithmic scale) using the a-Si:H model [11] and the proposed nc-Si:H model.

Fig. 3. Experimental and modeled $I_{DS}$-$V_{DS}$ characteristics using using the a-Si:H model [11] and the proposed nc-Si:H model.

Fig. 4. Experimental and modeled transconductance using the a-Si:H model [11] and the proposed nc-Si:H model.

Fig. 5. Simulated (with SILVACO Atlas) carrier concentrations using WTA=0.03 eV. $V_{DS} = 5$ V.

Fig. 6. Simulated (with SILVACO Atlas) transconductances using different values of WTA. $V_{DS} = 5$ V.

Fig. 7. Simulated (with SILVACO Atlas) DOS shape using different values of WTA. $V_{DS} = 5$ V.