Source/Drain Parasitic Resistance Role and Electrical Coupling Effect in sub 50nm MOSFET Design

Jun Yuan

Department of Electrical Engineering, University of California, Los Angeles, CA 90024, USA
Jun_yuan@ee.ucla.edu

*Peter M. Zeitzoff **

**SEMATECH, Austin, TX 78741, USA*
peter.zeitzoff@sematech.org

Jason C. S. Woo

Department of Electrical Engineering, University of California, Los Angeles, CA 90024, USA
woo@icsl.ucla.edu

Abstract

Source/Drain (S/D) parasitic resistance limitation and electrical coupling effect have been studied in sub 50nm MOSFET device. S/D extension region under sidewall spacer can be the main part of the total S/D series resistance, box-like junction application can eliminate the S/D-to-gate overlap, thus enhance planar device scaling into sub-50nm regime. DIBL is sensitive to S/D extension doping concentration, and it can be decoupled from deep S/D region with sidewall spacer design. Contact resistance plays an important role in device drive current capability. But contradictory to long contact limit case, we present for the first time that increased contact electrode depth in scaled S/D region reduces contact resistance.

1. Introduction

MOSFET device performance is mainly determined by carrier transportation in the channel, source/drain-to-gate electrical static coupling, and other parasitic effects. Scaling of MOSFET devices has been a key driving force in IC industry due to high speed and low power requirements [1], but the short channel effect (SCE) should be suppressed and drive current capability (I_{on}) should be enhanced together to exploit the full advantage of MOSFET scaling. Source/Drain (S/D) engineering gains attention for realization of high operating performance in deep sub-micron regime.

Source/Drain extension (SDE) to gate overlap effect has been studied comprehensively in ~ 100nm regime [2], and it is reported that ~ 20nm/side overlap is necessary prior to the onset of rapid I_{on} degradation for conventional implant devices (laterally graded doping in SDE), and it was concluded that down scaling limit for gate length is 60-70nm in planar MOSFET devices. However, we propose that I_{on} degradation with less gate overlap [2] mainly came from the SDE region under sidewall spacer due to its graded low doping. Box-like S/D junction application in our simulation shows that SDE-to-gate overlap can be totally eliminated without degradation of I_{on} with proper S/D design, thus enhancing conventional down scaling into sub-50 nm regime.

Contact resistance plays important role in limiting I_{on} when channel resistance is shrunk with scaling devices. Contact electrode depth effect in S/D region in long contact limit has been studied in [3], and it was shown that contact resistance increases with contact depth in deep S/D region. However, we demonstrate that it is different in fully scaled down devices.

In this context, S/D electric coupling effect has been concurrently studied by examining S/D doping and geometry effect on drain-induced-barrier-lowering (DIBL) in 45nm NMOS device. Our work provides guidelines for S/D engineering in sub 50nm planar MOSFET design, and optimized S/D structure is proposed based on this study.

2. Simulation structure and model

Fig.1 shows the two dimensional device structure used in our simulation. Gate length is 45nm (metallurgical channel length is 30nm), and equivalent gate oxide thickness is 8 A, junction depths for SDE (X_{je}) and deep S/D (X_{jc}) are 15 nm and 45 nm respectively with box-like profile, and gate and drain bias are 0.8 V [4].

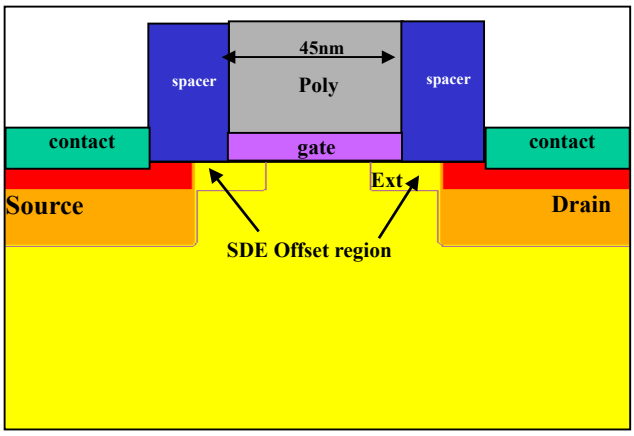

Fig.1 2-D view of MOSFET with an extension offset region (SDE junction: X_{je} =15nm, deep S/D junction: X_{jc}=45nm)

In this context, the S/D extension region underneath the sidewall spacer is defined as an offset region, its lateral dimension (L_{ext}) can be changed with different deep S/D region encroachment, as a result of spacer width variation (L_{ext} can be zero or negative if deep S/D region encroaches to the gate edge or channel region). For comparison of device performance, identical leakage current (10nA/μm) is kept for all of the simulated devices, which is achieved by changing substrate doping.

Device simulations are carried out using energy balance models with SILVACO tool [5].

3. Results and Discussions

(1). Source/Drain doping and geometry effect on I_{on} and DIBL

Fig.2 shows the relationship between I_{on} (solid symbol) and DIBL (hollow symbol) as a function of SDE doping concentration with two kinds of SDE offset length (L_{ext}) cases.

For nonzero L_{ext} device, I_{on} degrades considerably with reduced S/D extension doping concentration (N_{ext}). However, with zero L_{ext} design by aligning deep S/D with gate edge, I_{on} is almost independent of N_{ext} decrement. ***This clearly demonstrates the critical role of N_{ext} underneath the sidewall spacer in contributing high S/D series resistance***. Hence, the rapid I_{on} degradation with less gate overlap in [3] can be explained as the result of low N_{ext} under spacer due to its lateral doping gradient. For zero L_{ext} devices shown in Fig.2, the little dependence of I_{on} on N_{ext} is attributed to the trade-off between SDE accumulation resistance and threshold voltage, by changing substrate doping concentration to keep the identical leakage current.

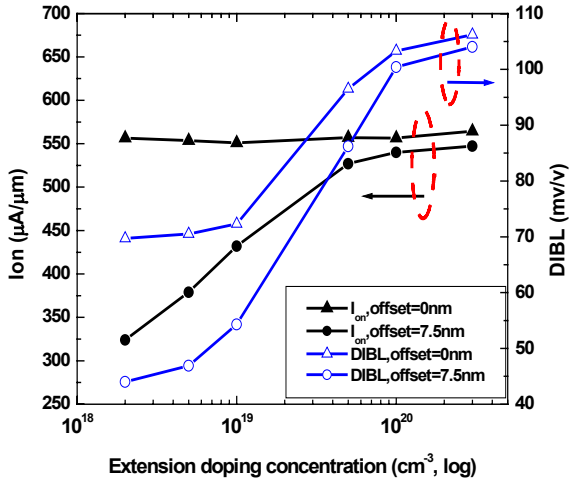

Fig. 2 Simulation data of I_{on} & DIBL vs. SDE doping concentration with zero and nonzero SDE offset region case (X_{je}=15nm, X_{jc}=45nm, deep S/D doping=3x10^{20}cm^{-3})

Fig.2 shows that DIBL increases substantially in a certain extension doping range, and this is the result of an increased depletion charge induced in the channel. But DIBL is almost insensitive to N_{ext} at high doping and low doping range respectively. When N_{ext} is very high, the depletion region induced in the channel no longer increases, thus resulting in saturated DIBL. On the other hand, at the low doping range, the depletion region extends laterally through the extension region and reaches deep S/D region, thus limiting further DIBL reduction with decreased N_{ext}. Similar trend of DIBL versus N_{ext} is obtained with both zero and nonzero L_{ext} devices, and DIBL difference at low doping range between them indicates deep S/D encroaching effect on DIBL.

But ***DIBL can be decoupled from deep S/D region***, shown in Fig.3. With the increment of L_{ext} by enlarging spacer width, DIBL becomes almost flat since it is mainly contributed by SDE region. However, I_{on} degrades continuously with increment of L_{ext}, especially for low N_{ext} case, this further confirms the role of SDE region under spacer in contributing to S/D series resistance.

Therefore, considering I_{on} and DIBL together, device can be designed with two kinds of approaches: low N_{ext} with minimum L_{ext} to reduce S/D resistance, or high N_{ext} with large L_{ext} to decouple DIBL. By comparing the results shown in Fig.3, it is shown that device design with low N_{ext} but zero L_{ext} can have both higher I_{on} and lower DIBL.

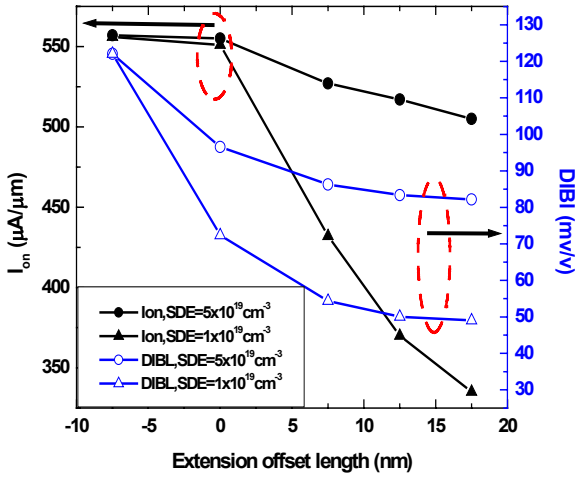

Fig. 3 Simulation data of Ion & DIBL vs. extension offset length with two different extension doping (X_{je}=15nm, X_{jc}=45nm, deep S/D doping=3x10^{20}cm^{-3})

With zero L_{ext} design, I_{on} and DIBL relationship as a function of SDE junction depth (x_{je}) under gate is shown in Fig.4. It is shown that x_{je} effect on DIBL is related with extension doping. At low N_{ext}, DIBL is not

sensitive to x_{je} since DIBL is mainly controlled by deep S/D region. At high N_{ext}, DIBL decreases with x_{je} because of reduced charge sharing with channel. But I_{on} is insensitive to the x_{je} scaling (even down to zero) in both cases, and it is due to trade-off between increased accumulation resistance and reduced threshold voltage to keep same leakage current. Therefore, ***SDE-to-gate overlap region can be totally eliminated without degradation of I_{on} with zero L_{ext} design***, even it has large metallurgical channel length. This non-overlap device also has low C_{gs} and C_{gd} benefit, which is favorable for high speed application.

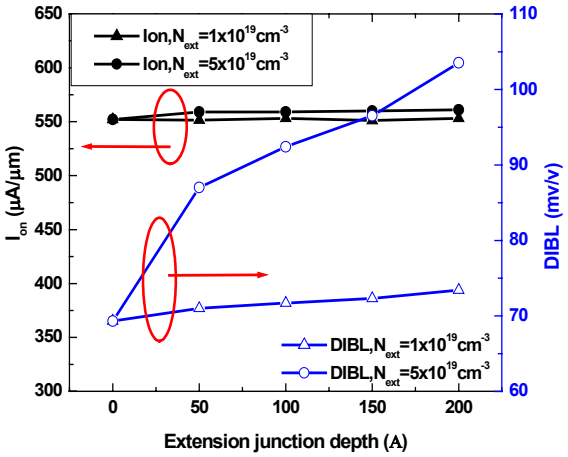

Fig.4 I_{on} & DIBL variation vs. X_{je} with two different SDE doping concentration (L_{ext} =0nm)

Fig. 5 illustrates that DIBL can be reduced with reduction of deep S/D junction depth (X_{jc}). However, I_{on} is almost not degraded due to its high doping concentration. Therefore, shallow S/D region application combined with zero gate overlap and L_{ext} design can further enhance the planar device scaling into 30 nm regime [6].

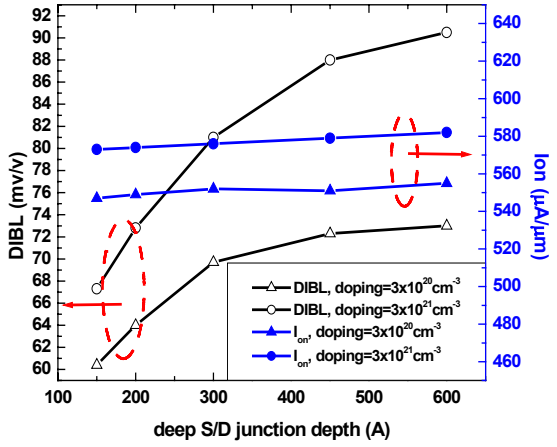

Fig.5 I_{on} & DIBL variation vs. deep S/D junction depth with two different deep S/D doping concentration (L_{ext} =0nm)

(2). Specific contact resistance and contact electrode depth effect

MOSFET channel resistance is reduced with scaled channel length, but on the other hand, the accordingly scaled contact area causes an increment in contact resistance if specific contact resistance is not scaled. Therefore, technology to reduce the specific contact resistance has a major impact on I_{on} in deep sub-micron MOSFET as shown in Fig.6.

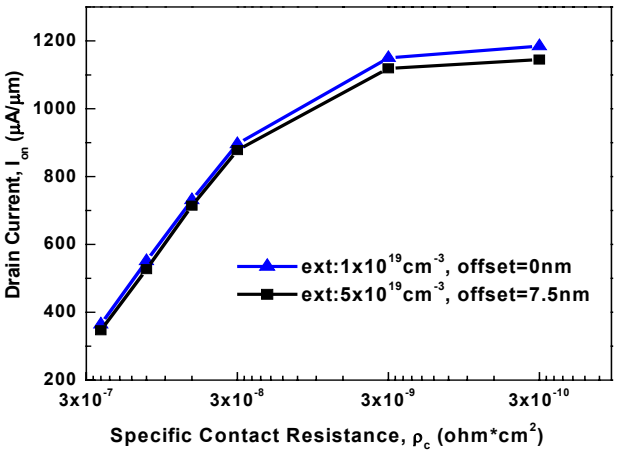

Fig.6 Relationship between I_{on} and specific contact resistance in 45nm NMOS device (contact area=0.045μm x 1μm)

Contact electrode depth effect on Device performance has been studied in long contact limit case [3]. It was reported that contact resistance increases with contact depth in deep S/D region due to the increased sheet resistance underneath the contact region. Our simulation also shows similar results in the long contact limit case. However, it is different in fully scaled devices.

The relationship between I_{on} and contact electrode depth in S/D region with short contact limit (0.045μmx1μm) is shown in Fig 8. It can be seen that

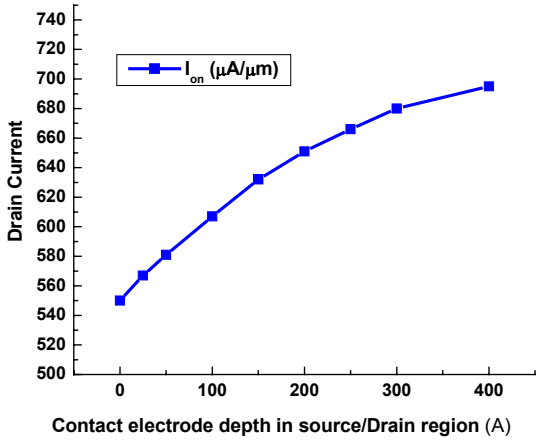

Fig.7 Ion improvement with contact depth in S/D region (ρ_c=1.2 x 10^{-7} ohm.cm^2, contact area is 0.045μmx1μm)

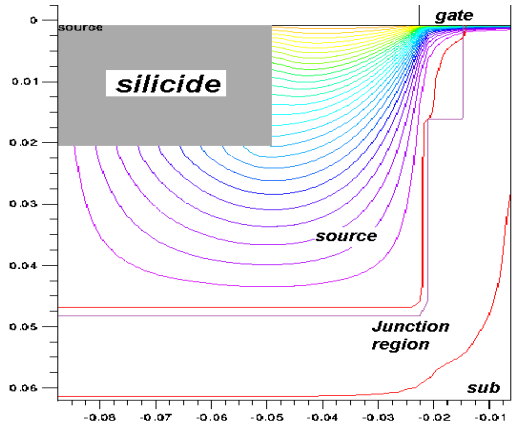

Fig.8 2-D view of current flow to contact electrode, it shows current flows to both side contact and planar contact

contact resistance is reduced with increased contact depth. The reason is that ***current flows to both side contact and planar contact region in fully scaled device***, as shown in Fig. 9 (but in long contact case, current mainly flows to planar contact region, not the side contact region). Thus, the resulting contact resistance can be considered as a sidewall contact resistance in parallel with a bottom contact resistance. And the side contact area increases with the increment of contact depth in S/D region, which results in a smaller contact resistance in scaled device design.

4. Optimized device with S/D engineering

Based on short contact limit analysis in Fig. 6 & 7, thick silicide technology is still needed in scaled device, not only for reduction of silicide sheet resistance, but also for deep contact depth in S/D region to reduce contact resistance. Hence, another heavily doped deep S/D region is needed for the contact region, but large sidewall spacer must be used to minimize its effect on DIBL, as analyzed in Fig.3.

Based on the analysis in this context, the S/D optimized device is shown in Fig.9: zero S/D overlap with gate, heavily doped shallow S/D under large sidewall spacer, and thick low-barrier silicide formation in deep S/D contact region.

The box-like junction profile can be obtained by laser annealing method [7,8], and low specific contact resistance can be achieved with dual low-barrier silicide material application (ErSi and PtSi) [9]. And this design can be extensively applied to 30 nm planar devices.

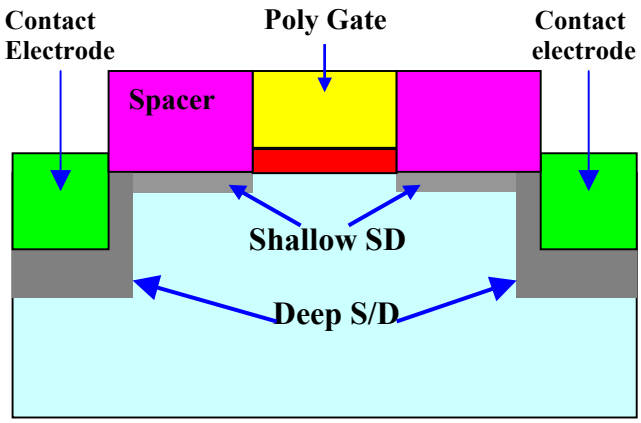

Fig.9 Two-Dim view of the proposed device structure with source/drain optimization

5. Conclusions

Source/Drain parasitic resistance limitation and electric coupling effect has been studied in sub 50nm device. It is shown that S/D extension region under sidewall spacer can be the main part of the total S/D series resistance, and box-like junction profile application can eliminate SDE-to-gate overlap, thus enhancing planar device scaling into sub-50nm regime. DIBL is sensitive to SDE doping concentration, but it can be decoupled from deep S/D with large sidewall spacer design. Contact resistance plays an important role in device current drive capability, and increased contact depth in S/D actually reduces contact resistance, which is contradictory to long contact limit case. The optimum S/D structure can be obtained with zero S/D overlap with gate, heavily doped shallow S/D junction under spacer, and thick low-barrier silicide in deep S/D contact region.

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