ZrO$_2$ gate dielectrics prepared by e-beam deposition of Zr and YSZ films and post annealing processes

M. Johansson, M. Y. A. Yousif, A. Sareen, P. Lundgren, S. Bengtsson
Solid State Electronics Laboratory, Department of Microelectronics and Microtechnology Centre at Chalmers (MC2), Chalmers University of Technology, S-412 96 Göteborg, Sweden
e-mail: yousif@ic.chalmers.se

U. Södervall
SIMS Laboratory, Department of Microelectronics and Nanosciences and Microtechnology Centre at Chalmers (MC2), Chalmers University of Technology, S-412 96 Göteborg, Sweden

Abstract

In this paper we present the electrical performance of MOS capacitors with ZrO$_2$ gate dielectric prepared by e-beam evaporation of Zirconium and Yttrium Stabilized Zirconia (YSZ) and subsequent thermal treatment. To this stage we have reached an equivalent oxide thickness (EOT) of 1.9 nm. The effect of post-oxidation annealing on Zr incorporation into the Si substrate is investigated. SIMS analysis showed no signs of Zr diffusion in the substrate at temperatures as high as 900°C and that significant diffusion occurs only at 1100°C.

1. Introduction

The relentless scaling of Si MOSFET devices, which has offered outstanding improvement in performance with SiO$_2$ as the gate dielectric, seems to have reached an end. For SiO$_2$ films thinner than 2 nm, the leakage current between the gate and the substrate becomes intolerable. To suppress this current, thicker oxides with higher dielectric constants may prove viable to replace SiO$_2$. In order to meet performance and leakage requirements, for low-power applications, high-k gate dielectrics are required by the year 2005 [1]. It is worth mentioning here that dielectrics with too high k values may not prove viable for devices below 100 nm because they will enhance short channel effects [2]. Certain criteria must be fulfilled before these high-k materials can be nominated as gate dielectric candidates for CMOS technology. These include, the energy bandgap, the conduction and valence bands offsets with Si, thermal and electrical stabilities on Si, process compatibility with CMOS technologies, etc. A recent review of high-k gate dielectrics can be found in [3].

Among the high-k dielectrics that are widely nominated to be rather stable on Si and promising candidates for SiO$_2$ replacement are ZrO$_2$ and HfO$_2$ [4, 5]. Here in this paper we investigate MOS devices and materials incorporating ZrO$_2$ and YSZ films deposited with e-beam technique and post-deposition annealing processes. This deposition method, in addition to its system simplicity, can offer films with better purity and less damage compared to CVD and sputtering methods [6].

2. Experiment

PMOS capacitors were fabricated on 1-20 Ωcm (100) n-type Si wafers. YSZ (ZrO$_2$ doped with 9 mole % of Y$_2$O$_3$) and Zr metal films were deposited by e-beam evaporation on the Si wafers. Before loading the wafer into the chamber, the standard cleaning processes SC1 and SC2 and a dip in 2% HF were carried out until the wafer’s surface becomes hydrophobic. The chamber pressure during deposition was about (7.5 to 75)x10$^{-8}$ Torr, and the films were deposited at room temperature with a deposition rate of 1-6 Å/min. The films were furnace annealed in N$_2$ ambient @ 500°C for 20-30 min and some in O$_2$ ambient for 1-5 min. Immediately after annealing, Al gate electrodes were deposited either as blankets or through a shadow mask. These films were characterized by ellipsometry, optical Tencor Spectramap, Atomic Force Microscopy (AFM), CV, IV, and secondary ion mass spectroscopy (SIMS) measurements. Some of the devices received a process of post-metallization anneal (PMA) in N$_2$ ambient @ 350°C for 20 minutes.

3. Results and Discussion

In figure 1, we show the high frequency (1 MHz) CV characteristics for a YSZ film (S0), which was e-beam deposited on an n-type 1-10 Ωcm Si substrate. From the maximum capacitance in accumulation an equivalent oxide thickness (EOT) of 8.6 nm was extracted. The film thickness was measured with the Tencor alpha-step profilometer to be about 35 ± 4 nm. A dielectric constant of 15.5 ± 1.5 was deduced from Fig. 1, assuming no interfacial layer is formed. The nonuniformity is believed to be partly due to a large tilt angle used for the substrate holder. Large hysteresis (~ 0.20 V) has also
been observed in all films. The total oxide charge density estimated from Fig. 1 to be $8 \times 10^{11}/\text{cm}^2$.

The films of S0 were further investigated for Zr interdiffusion using SIMS analysis after different furnace annealing temperatures in the range 500-1100 °C for 20 min (loading in and out times excluded). The Zr and oxygen ($O^{16}$) profiles are displayed in Fig.2a and 2b, respectively; the sputtering ion was $O^{16}$. As can be seen in Fig. 2a, for temperatures between 500-800 °C there is no sign of Zr incorporation into the Si substrate, within the SIMS resolution. This observation is in agreement with previous measurements, which were carried out up to 700 °C and for 5 minutes [4]. At 800 °C, however, we observed a depression in the Zr profile (not shown) at two different places on the sample and also a change in the O$^{16}$ profiles as shown in Fig. 2b. This could either be due to an onset of another phase of the film crystal structure, which would, in turn, lead to a rather different sputtering rate or it could be due to an inhomogeneity of Zr in the film caused at 800 °C. Although there is no sign of Zr incorporation into the Si substrate at this typical CMOS processing temperature, the undesirable low-k interfacial layer is most likely to widen.

As the annealing temperature is increased above 800 °C, the Zr profile slope starts to become more negative i.e. Zr diffuses in the Si substrate. It is worth to note that only at 1100 °C that a significant Zr interdiffusion can be observed as is clearly shown in Fig. 2a. It is needless to mention that the incorporation of Zr into the Si substrate has a great impact on the channel mobility.

In Fig. 3a and 3b, we show the hf-CV (1 MHz) and the current-voltage (IV) characteristics, respectively, for the thinnest YSZ film (S5) we have deposited using the e-beam evaporation method. An EOT of 1.92 nm is extracted from the CV measurement. Undesirable large hysteresis is clearly shown and also the flat band voltage is negatively shifted. The total oxide charge was extracted to be $7.8 \times 10^{12} / \text{cm}^2$ for the negative voltage sweep and $5.3 \times 10^{12} / \text{cm}^2$ for the positive sweep. Compared to SiO$_2$, the gate leakage current is reduced by about 3 orders of magnitude. In an attempt of reducing the leakage current further, a PMA process was performed in $N_2$ ambient @ 350 °C for 20 min. The leakage current was even higher after this step, which possibly could be attributed to some reaction between the Al electrode and the gate oxide.

We have also e-beam deposited thin Zr metal films on Si (S8), which were then furnace annealed in $N_2$ ambient @ 500 °C for 20-30 min and some in $O_2$ ambient for 1-5 min. In Fig. 4a and 4b, we show the hf-CV (1 MHz) and the current-voltage (IV) characteristics, respectively. An EOT of 2.0 nm is extracted from the CV measurement. The flat band voltage is shifted positively. The total oxide charge was extracted to be $6.7 \times 10^{12} / \text{cm}^2$. Since no stretch-out is observed at lower frequency (10 kHz), with only the effect of series resistance, most of the defects are due to fixed oxide and mobile charges. The gate leakage current is also reduced by about 3 orders of magnitude. These films deteriorated in the same manner as that of the YSZ films (S8) after PMA in $N_2$ ambient @ 350 °C for 20 min.

4. Conclusions

We have used e-beam evaporation and thermal treatment to deposit high-k ZrO$_2$ on Si from Zr metal and YSZ targets. SIMS, CV and IV measurements were performed to characterize and evaluate these films. The interdiffusion behavior of Zr (from a 35-nm YSZ film on Si substrate) into Si has been studied at different temperatures ranging from 500-1100 °C. At 800 °C, a change in the crystal structure is anticipated to have taken place and significant diffusion occurred only at 1100 °C. A dielectric constant of about 15.5 was extracted from the CV measurements and EOT of 1.9-2.0 nm have been achieved with this evaporation method. The films became more leaky after a PMA process in $N_2$ ambient at 350 °C for 20 min, which can be attributed to a possible reaction between the Al gate electrode and gate oxide.

Acknowledgement

This work was financed by the Swedish Strategic Research Foundation (SSF).

References

Fig. 1. High-frequency (hf) CV (1 MHz) for MOS capacitor with a YSZ gate dielectric, which was e-beam deposited. The average physical thickness is about 35 ± 4 nm.

Fig. 2a. SIMS depth profile of Zr for S0 after furnace annealing at different temperatures for 20 min each. O\textsuperscript{16} ion is the sputtering ion.

Fig. 2b. SIMS depth profile of O\textsuperscript{18} for S0 after furnace annealing at different temperatures for 20 min each (O\textsuperscript{16} ion is the sputtering ion).

Fig. 3a. hf-CV for a thin YSZ film. An EOT of 1.92 nm was achieved with this e-beam deposition method. The total oxide charge density $7.8 \times 10^{12}$/cm\textsuperscript{2} for the –ve to +ve sweep, and $5.3 \times 10^{12}$/cm\textsuperscript{2} for the +ve to –ve sweep.

Fig. 3b. IV characteristic @ RT for the thin YSZ film shown in Fig. 2a. The value of the current density is reduced by about 3 orders of magnitude compared to that of an SiO\textsubscript{2} of 1.9 nm.

Fig. 4. hf-CV (a) and IV (b) characteristics for ZrO\textsubscript{2} film. An EOT of 2.0 nm was extracted. The total oxide charge density $6.7 \times 10^{12}$/cm\textsuperscript{2}.