Gate length scaling in high f_{MAX} Si/SiGe n-MODFET

F.Aniel, M. Enciso-Aguilar
P. Crozat, R. Adde,
IEF, Paris-Sud University, F-91405 Orsay, France,
E-mail: frederic.aniel@ief.u-psud.fr

T. Hackbarth, U. Seiler.
H-J. Herzog, U. König
DaimlerChrysler Research Center, Wilhelm-Runge-Str. 11, D-89081 Ulm, Germany)

H.Von Känel
ETH Zürich, CH 8093 Zürich, Switzerland

Abstract

The performances of strained channel Si/$Si_{0.6}Ge_{0.4}$ n-MODFETs as a function of gatelength have been investigated experimentally at 300K . The direct-current, microwave and noise performances of devices with gatelengths ranging from 0.5 µm to 0.1 µm are presented. Maximum oscillation frequency f_{MAX} of 158 GHz is obtained for a 0.1 X 100 µm with f_T = 42 GHz and a minimum noise figure NF_{min} = 0.5 dB at 2.5 GHz showing the potential of SiGe technology. The dependence of small signal, and noise parameters on gatelength and biases has been analyzed to assess the impact of non stationary transport and of short channel effects on the device behavior.

1. Introduction

The exploitation of the band-gap engineering concept in silicon technology enables the design of devices for applications which were previously reserved to other materials, such as III-V semiconductor compounds. In a Si/SiGe n-MODFET, the tensile strain of the Si channel on SiGe splits the heavy and light hole valence bands, and shifts strongly downwards the two-fold anisotropic Δ valley normal to the interface. The energy discontinuity Δ_{2-4} has been estimated to be 6 meV [1] per germanium percent in the relaxed SiGe buffer. It gives superior transport properties to a Si strained undoped layer compared to an undoped bulk Si layer if an electric field is applied in the tensile plane. Several experimental and theoretical investigations have pointed out the strain-induced increase of electron transport properties in tensile strained Si layers grown on a relaxed SiGe substrate [2, 3]. Most electrons have a lower in-plane effective mass, and intervalley scattering rates are reduced. High electron mobilities up to 2900 cm^2/Vs at room temperature have been found even for high sheet carrier concentrations of 2-5 10^{12} cm^{-2} [3].

The rise of performances of SiGe technology continues with the scaling down of the transistor dimensions towards deep sub-micrometer gate lengths where non stationary transport becomes significant. Non stationary dynamics leads to electron velocity overshoot, short channel effects. In this work, SiGe MODFET's with gate length between 0.5 µm and 0.1 µm have been investigated. An experimental investigation to asses the impact of non stationary transport and short channel effects on the overall device performances is presented. Devices with a room temperature f_{MAX} up to 158 GHz, but with a f_T up to 42 GHz and a minimum noise figure NF_{min} = 0.5 dB at 2.5GHz have been studied.

2. Device structure and experimental setup

The active layer stack is grown by solid source molecular beam epitaxy (MBE) on a compositionally graded Si/$Si_{0.6}Ge_{0.40}$ virtual substrate which is grown by low energy plasma enhanced chemical vapor deposition (LEPECVD) on a high resistivity 1000 Ω cm p-type Si substrate. The modulation-doped structure consists of, from bottom to top, a 5 nm Sb doped $Si_{0.6}Ge_{0.4}$ supply layer with a doping density of $2x10^{18}$ cm^{-3}, a 3 nm undoped $Si_{0.6}Ge_{0.4}$ spacer, followed by a 9 nm biaxially strained undoped Si channel, a 4.5 nm undoped $Si_{0.6}Ge_{0.4}$ spacer, a 5 nm Sb doped $Si_{0.6}Ge_{0.4}$ supply layer with a doping density of $1x10^{19}$ cm^{-3}. Finally the structure is capped with a 4 nm Si cap layer. The mushroom Ti/Pt/Au Schottky gate is patterned by e-beam lithography. In the gatelength scaling study, the gate is 100 µm wide with lengths L_G of 0.1, 0.15, 0.25, 0.5 µm and is centered within the source-drain distance L_{SD} of 2 µm. In the n-MODFET's with best frequency performances the gate is 0.1 µm long and 30 µm wide, and is placed asymmetrically nearer to the source (L_{SG} =0.5µm) within the source-drain space (L_{SD} = 1.5 µm).

A HP8510C vector network analyzer is used to perform HF measurements between 50 MHz and 50 GHz.The noise parameters are measured from 2 to 18 GHz with a noise test set designed around a Cascade on-wafer prober, a HP8510C vector network analyzer and a HP8563E spectrum analyzer. Their determination exploits the information contained in the noise figure variation versus frequency for only two impedance sources, a 50 Ω and a shorted delay line presented at the transistor input [4].

3. Experimental results and discussion

The static characteristics of the n-MODFET are presented in Figs. 1-2. The drain current increases steadily when the gatelength decreases while the threshold voltage V_{TH} shifts from –0.38 V down to –0.62 V. Neither thermal effect nor impact ionization signatures are observed in the I-V characteristics. Concerning the "on state " breakdown voltage, measurements at drain voltage up to 3.5 V have been performed on a l_G = 0.1 µm transistor without any observation of impact ionization. This point is under deeper investigation.

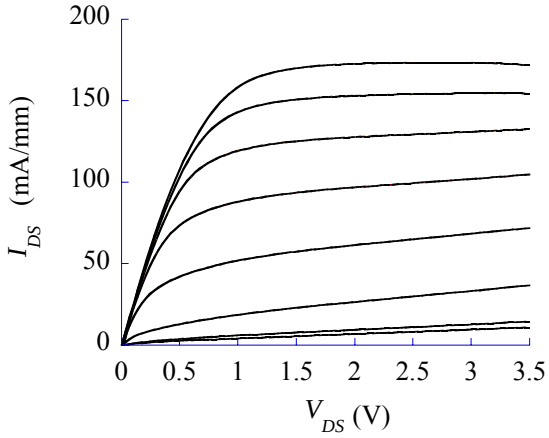

Figure 1. I-V characteristics of a 0.1 x 100 µm^2 n-MODFET at room temperature

The gate current versus gate voltage and gatelength is presented in Fig. 3. The gate leakage current increases at reduced gate length but it remains small due to a moderate doping level and a large gate to channel distance

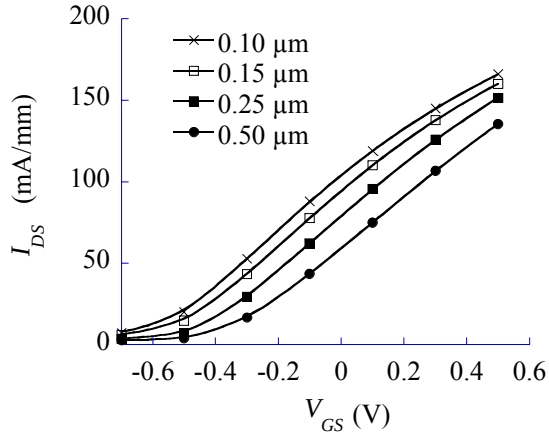

Figure 2. I_D-V_G at V_{DS} = 1.5 V for 0.1, 0.15, 0.25 and 0.5 µm gatelengths n-MODFET's

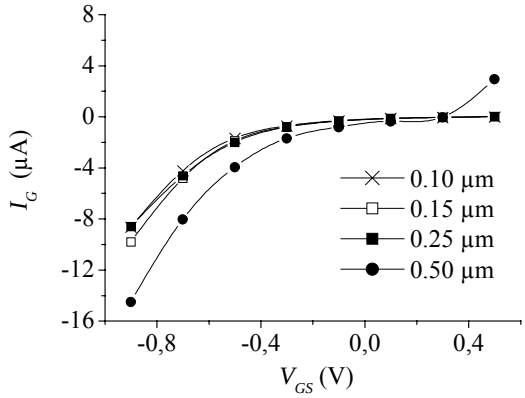

Figure 3. MODFET gate current versus gate voltage for several gate lengths at V_{DS} = 1.5 V

We now turn to microwave performances. The de-embedding step, performed to remove the contribution of line accesses and pads, reveals low losses in the virtual substrate which is a good point for future high frequency circuit realization. This low substrate leakage is responsible of only small differences between the raw measurements of the maximum frequency of oscillation frequency f_{MAX} and the de-embedded data presented here.

After the first reported RF data on Si/SiGe MODFETs in 1994, the frequency performances have grown step by step to f_T = 46 GHz and f_{MAX} = 92 GHz [5]. More recently, f_T = 62 GHz for a 0.18 µm gatelength [6] and f_T = 74 GHz for a 0.1 µm device [8] have been obtained. f_{MAX} as high as 120 GHz [7], and minimum noise figure, NF_{min} as low as 0.3 dB at 2.5 GHz with equivalent noise resistance R_n of 46 Ω [9] have been reported. Some demonstrator circuits based on n-MODFETs already exist. Inverters [10] and transimpedance amplifiers [11] open the road to more complex circuits, and the forthcoming integration of n-type and p-type HFETs offers a new generation of circuits based on a new complementary transistor technology. Cryogenic behavior investigations of n-MODFETs are presented in [7], [12] and [9] showing f_{MAX} as high as 195 GHz [7], f_T of 107 GHz [8] at 50K. The forthcoming HF and noise results are well representative of the steady improvement of material, of technology and of device performances.

Figure 4 illustrates the dependence on $1/L_G$ at room temperature of extrinsic f_T and intrinsic f_{Ti} cut-off frequencies. The latter is calculated by $f_{Ti} = g_m/(2\pi(C_{GS} + C_{GD})$. The maximum oscillation frequency f_{MAX} (Mason's gain) is also shown. As expected, both f_T and f_{MAX} increase as the gate length is reduced. The appearing stronger increase of f_T and f_{Ti} at large $1/L_G$ values might be regarded as the influence of velocity overshoot. f_T and f_{MAX} values are displayed in Table 1 at the four gate lengths. The total microwave delay is divided by less than 5 between the 0.5 and the 0.1 µm gatelength due to the detrimental role played by the feed back capacitance C_{GD} and the output conductance g_d in the shortest device.

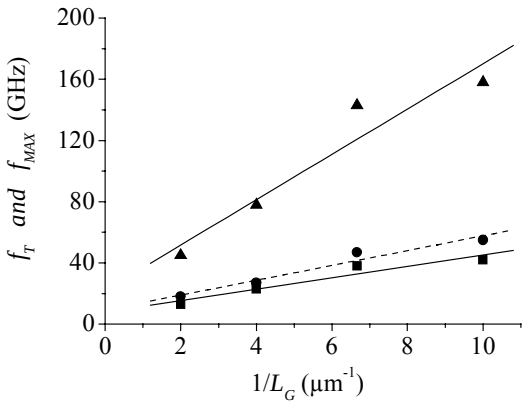

Figure 4. f_{Ti} (dashed line, solid circles), f_T (solid line, squares) and f_{MAX} (solid line, triangles) of a n-MODFET as a function of $1/L_G$ (V_{DS} = 1.5 V)

Excellent f_{MAX} value as high as 158 GHz have been reached for the 0.1 x 100 μm^2 device, corresponding to the state of the art of SiGe HeteroFET technology. The f_{MAX} value is proportional to f_{Ti} , to the C_{GS}/C_{GD} ratio and inversely proportional to the product (g_d .(R_S + R_G+ R_i)) where g_d is the intrinsic output conductance, R_S the source resistance, R_G the gate resistance and R_i the channel charging resistance. At smaller gatelength f_{Ti} rises due to the increase of non stationary transport while all other contributions to f_{MAX} decrease. But the T shape of the gate and the smaller aspect ratio limit strongly these reductions. In conclusion the f_{MAX} increases dramatically when the gate length is reduced down to 100 nm. A record data of f_{MAX} =183 GHz has been observed for an asymmetrically patterned device with L_G=0.1μm, L_{SG} = 0.5 μm, , L_{SD} = 1.5 μm, w = 30 μm [13], but with the same technology, which illustrates the improvement of f_{MAX} owing to a further reduction of R_S and R_G

Table1.f_T, f_{MAX} *and total microwave delay*

L_G (μm)	f_T (GHz)	f_{MAX} (GHz)	$1/(2\pi f_{Ti})$ (psec)
0.10	42	158	2.89
0.15	38	143	3.38
0.25	23	78	5.89
0.50	13	45	8.84

Figure 5 which shows the voltage gain g_m/g_d , reveals the influence of short channel effects as the gatelength becomes smaller. Although the transconductance still continues to increase at smaller gatelengths, the output intrinsic conductance rises when L_G diminishes**,** for three reasons**:** 1) the improvement of carrier velocity in the channel because the physical mechanism insuring the drain current saturation is not able to screen efficiently the drain bias modulation, 2) carrier transfer from the channel towards the substrate buffer and to the upper layers where transport properties are lower than in the channel, and 3) strong reduction of the aspect ratio at short gatelengths

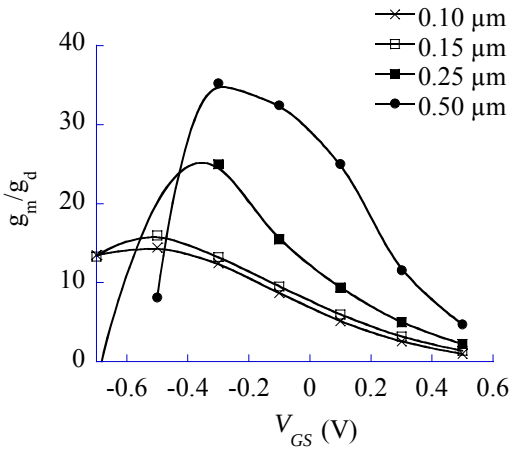

Figure 5. Intrinsic voltage gain g_m/g_d of n-MODFET versus V_{GS} with L_G as a parameter (V_{DS} = 1.5 V)

On the other hand, both intrinsic capacitance C_{GS} and C_{GD} are proportional to the gate length. However the reduction of the measured C_{GS}/C_{GD} ratio represented in Fig. 6 can be mainly attributed to the smaller aspect ratio at short L_G. The detrimental effects such as short channel and aspect ratio degradation can be further reduced owing to a proper scaling of device dimensions

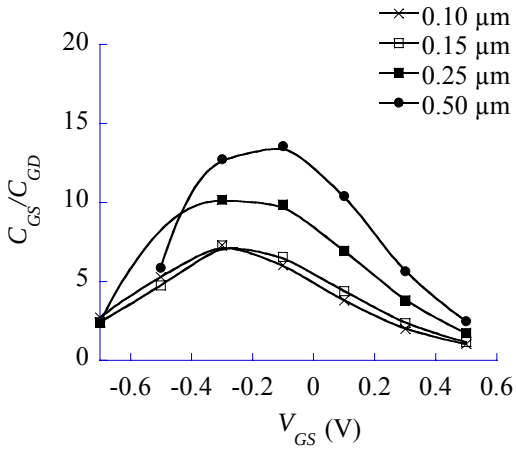

Figure 6. C_{GS}/C_{GD} ratio of n-MODFET's versus V_{GS} with L_G as a parameter (V_{DS} = 1.5 V)

Figure 7 shows the minimum noise figure NF_{min} versus $1/L_G$ at 2.5 GHz and 16 GHz. The relatively low resistivity of the Si substrate and of the $Si_{1-x}Ge_x$ graded buffer is responsible for a noise contribution of the device access lines and pads to the measured results. We have developed device access noise de-embedding using a full on-wafer characterization and modeling of open and short structures. The noise contribution of device accesses to NF_{min} is 0.3 dB, while its contribution to R_n is negligible. The accuracy of de-embedded NF_{min} is ±0.2 dB and of R_n is ±5%.

For the two frequencies presented in Fig. 7, NF_{min} decreases at reduced gatelength. The reduction of NF_{min} versus L_G at low frequency (2.5 GHz) is small while it is

much larger at high frequencies (16 GHz), due to the large increase of f_{Ti} versus $1/L_G$.

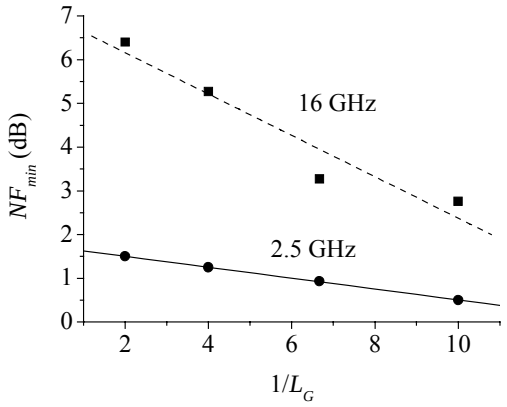

Figure 7. NF_{min} of n-MODFET's versus $1/L_G$ at 2.5 GHz and at 16 GHz (V_{DS} = 1.0 V)..

Figure 8 displays the equivalent noise resistance R_n versus $1/L_G$ at 2.5 and 16 GHz. R_n also decreases with L_G but increases only slightly versus frequency.

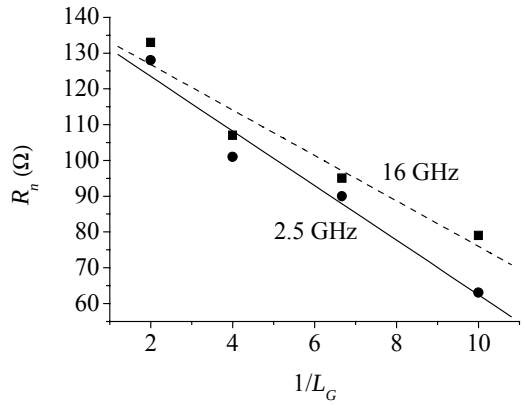

Figure 8 : R_n of n-MODFET's versus $1/L_G$ at 2.5 GHz and at 16 GHz (V_{DS} = 1.0 V)

The reduction of the NF_{min} and of R_n at small gate length can easily be explained by the corresponding enhancement of transconductance as a consequence of the increase of carrier velocity. NF_{min} and R_n measured optimum values are 0.5 dB, 63 Ω at 2.5 GHz , and 2.7 dB, 79 Ω at 16 GHz, respectively. The noise performances presented here are at the state of the art [9]. The very low *Rn* for this Si/SiGe n-FET technology due to a very low R_G and a high g_m. are comparable to values for SiGe HBT's and better than for CMOS technology.

6. Conclusion

The performance dependence of Si/SiGe n-MODFETs on gatelength has been examined. It shows that high frequency operation with low noise and high voltage breakdown of good reliability can now be offered for SiGe circuits with 0.1µm gatelength devices. HF and noise results represent the steady improvement of materials, of technology and of device performances. A f_{MAX} = 158 GHz for a symmetrical device is obtained. Further optimization of velocity overshoot effects in 70 nm gatelength devices with restrained short channel effects and reduced device parasitic will bring new progress.

Acknowledgements: The financial support of the EC in the frame of IST-1999-SIGMUND project, and of the German BMBF project ALCANT-SATCOM are gratefully acknowledged.

7. References

[1] M. Rieger, and P. Vogl, "Electronic-Band parameters in Strained $Si_{1-x}Ge_x$ substrates," *Phys. Rev. B*, vol. 48, no. 19, pp. 14276-14287, 1993.

[2] T. P. Pearsall, J. C. Bean, R. People, and A. T. Fiory, "Ge_xSi_{1-x} modulation-doped p-channel field-effect transistors," in *Proc. Int. Symp. Si-MBE*, 1985, pp. 400-405.

[3] S. F. Nelson, K. Ismail, J. O. Chu, and B. S. Meyerson, "Room-temperature electron mobility in strained Si/SiGe heterostructures," *Appl. Phys. Lett.*, vol. 63, no. 3, pp. 367-369, 1993.

[4]V. Danelon, P.Crozat, F. Aniel, G. Vernet, "A 4 noise parameters determination method for transistors based on the frequency dependence of the noise figure", *Electron. Lett.*, vol. 34, pp. 1612-1613, 1998.

[5]M. Glück, T. Hackbart, U. König, M. Birk, A. Haas, and E. Kohn, *Proc. MSS 8*, July 1997, St. Barbara.

[6] S. J. Koester, J. O. Chu, and R. A. Groves, "High-f_T n-MODFETs fabricated on Si/SiGe heterostructures grown by UHV-CVD," *Electron. Lett.*, vol. 35, no. 1, pp. 86-87, 1999

[7] F.Aniel, N. Zerounian, R. Adde, M. Zeuner, T. Hacbarth, U. König., "Low temperature analysis of 0.25 µm SiGe n-MODFET", *IEEE Trans. on Electron Dev.,* 2000, 47, pp. 1447-1453.

[8]F. Aniel, M. Enciso-Aguilar, T. Mack, U. Seiler, Th. Hackbarth; L. Giguerre; P. Crozat; R. Adde; B. Raynor. " High performance 100 nm T-gate strained $Si/Si_{0.6}Ge_{0.4}$ n-MODFET", Semiconductor Device Research Symposium, 2001 International , 2001, pp. 482 -485

[9] M. Enciso, F.Aniel, P. Crozat, R. Adde, M. Zeuner, T. Fox, T. Hackbarth." 0.3 dB minimum noise figure of 0.13 µm gate-length strained $Si/Si_{0.58}Ge_{0.42}$ n-MODFETS "Elect. Letters, vol. 37, issue 17, pp 1089-1090, Aug. 2001.

[10] T. Ostermann, M. Glück, R. Hagelauer et al., in *Proc. Int. Semicond. Device Research Symposium*, Dec. 1997.

[11] M. Saxarra, M. Glück, J. N. Albers, D. Behammer, U. Langmann, and U. König, "Transimpedance amplifiers based on Si/SiGe MODFETs," *Electron. Lett.*, vol. 34, no. 5, pp. 499-500, 1998.

[12] M.J. Rack, T.J. Thornton, D.K. Ferry, J. Robrts, R.C. Westhoff, M. Robinson,"Cryogenic field effect transistor using in Si:SiGe heterostructure grown by APCVD", Materials Science and Engineering B87 (2001) 277-281

[13] M. Enciso, F.Aniel, P. Crozat, R. Adde, M U. Seiler.

H-J. Herzog, U. König, *H.Von Känel* "DC and High Frequency performance of a 0.1 µm $Si/Si_{0.6}Ge_{0.4}$ n-type MODFET with a 183 GHz f_{MAX}"., private communication.