Abstract

An experimental and numerical study of the static and dynamic RF behaviour of 0.25 µm gate-length FDSOI MOSFETs is presented. For the numerical analysis, we used a 2D ensemble Monte Carlo simulator, in which real effects such as surface charges, contact resistances or experimental parasitic capacitances were considered. Results show an excellent agreement between the experimental data and the Monte Carlo simulation. In the static characteristics, short channel effects such as velocity overshoot or the presence of hot carriers are observed. Furthermore, important AC parameters (small-signal equivalent circuit capacitances, transconductance or cut-off frequency) are analysed.

1. Introduction

Fully-depleted (FD) silicon-on-insulator (SOI) technology is attracting an extraordinary interest in recent years. Many reasons exist for this concern: FDSOI MOSFETs offer important advantages over traditional bulk devices, such as a higher transconductance, reduced parasitic capacitances, etc., thus providing an exceptional high-frequency performance, together with a lower threshold voltage and absence of latch-up [1]. Due to these properties, FDSOI devices are being confirmed as an appropriate alternative for the realization of low-cost analog circuits operating at microwave frequencies with low power consumption.

In order to speed up the development of the technology and its applications, a complete and accurate characterization of the high frequency performance of the devices is needed. Computer simulation plays a very important role for this purpose. The traditional basic simulation methods, such as drift-diffusion or hydrodynamic models, show important limitations when applied to the study of MOSFETs with small dimensions. The reduction of the gate length towards deeply sub-micrometric dimensions involves the appearance of short-channel effects (velocity overshoot, hot carriers, etc.) for the study of which a microscopic approach is the best solution. In this framework, the ensemble Monte Carlo (EMC) method [2] appears as the most adequate simulation technique to deal with this problem, since it includes in a natural way all these phenomena. But to turn the Monte Carlo method into a reliable simulation tool, it is necessary to check the validity of the simulator with experimental measurements.

The aim of this work is to study the static and dynamic characteristics of n-channel 0.25 µm gate length FDSOI MOSFETs by means of experimental measurements and EMC simulations. We focused in the saturation regime, the main operation region of interest for these devices in analog applications. In the simulations, important effects appearing in real devices, such as surface charges, contact resistances, or extrinsic experimental capacitances were taken into account. For the static behaviour, the EMC method is able to supply many important quantities of interest, i.e. drift velocity, energy, and concentration of carriers, electric field inside the devices, etc. In the dynamic response, it allows not only to study the bias dependence of small-signal equivalent circuit (SSEC) parameters, but also to analyse the effect of different factors such as surface charges, overlap length variation, gate length reduction, oxide thickness, etc. on those parameters. In this way, the EMC method can be of great help in answering many questions stressed by the experimental results.

2. Structure under analysis

FDSOI MOSFETs were fabricated with a CMOS-compatible process on UNIBOND® wafers. The gate length was 0.25 µm with eight gate fingers in parallel, each having a finger width of 12.5 µm. The buried oxide thickness is 0.4 µm and the silicon thin film thickness was 30 nm. A titanium salicide process was used to lower the contact resistances. More details about the device geometry and the fabrication process can be found in Ref. [3].

The simulation was performed by means of a 2D semiclassical bipolar EMC simulator self-consistently coupled with a Poisson solver. Our model has been successfully employed for the study of different devices, like HBTs and BJTs [4] or MOSFETs [5]. The main
features of the simulator have been presented in Ref. [5]. Both electron and holes were simulated as particles, which allows to evaluate properly the influence of each type of carrier. The size of the meshes ranges from 10 to 250 Å in order to solve accurately the Poisson equation. The time step is 1 fs. Our MC simulator allows to take into account the effect of series resistances in the drain and source contacts by considering self-consistently the voltage drop due to these resistances for each time step. Real effects appearing in fabricated devices, such as surface charges [6] or impact ionisation have been taken into account.

The MC structure simulated (Fig. 1) attempts to reproduce the experimental geometry, taking into consideration the real values of important parameters, such as overlap length ($L_{ov}$), spacer oxide length ($L_{sp}$), oxide thickness ($t_{ox}$), doping profiles, etc. The device is considered to operate in common-source configuration, with source and substrate contacts short-circuited.

3. Static characteristics

Fig. 2 shows the output characteristics of the simulated devices (symbols) together with the experimental measurements (dashed lines). The inset shows the transfer characteristic for a drain voltage ($V_{DS}$) of 1.0 V. We found that the surface charge in the overlap and spacer regions is a key factor in achieving an accurate fit of the simulation results to the experimental transconductance. In general, MC output characteristics show a very good agreement with the experimental ones. Furthermore, the value of the threshold potential (around 0.25 V) is quite well reproduced. Impact ionisation processes were not observed in the $V_{DS}$ range considered. From now on, results are shown for $V_{DS} = 1.0$ V, corresponding to the saturation regime.

Figure 3 shows the ratio between extrinsic transconductance ($g_m$) and drain current ($I_D$) as a function of $I_D$. In Fig. 3 the ratio between extrinsic transconductance ($g_m$) and drain current ($I_D$) is shown. This is an important relationship, since high values of this ratio are indicative of a good performance in terms of voltage gain [1]. As it can be seen in Fig. 3, an excellent agreement is obtained between the MC results and the experimental data.

Figure 4 shows the electron concentration [Fig. 4 (a)], the electron velocity along the x direction [Fig. 4 (b)] and the electron energy [Fig 4 (c)] under the gate oxide for different $V_{GS}$ ranging from 0.25 to 1.25 V. Concern-
ing the electron concentration, it is remarkable the high carrier density present in the source overlap, whereas in the drain side it is practically null (as corresponds to a MOSFET device in the pinch off region) except for the case of the highest $V_{GS}$, which indicates that the device begins to leave the saturation region at the higher gate voltages. Electron velocity shows the appearance of an overshoot region, which is a well-known short-channel effect in MOSFETs [7].

The maximum value of this overshoot region, which is a well-known short-channel voltages. Electron velocity shows the appearance of an begins to leave the saturation region at the higher gate

4. Dynamic response

The MC method allows to calculate the intrinsic four complex admittance ($Y$) parameters that describe the AC behaviour of a two-port device [8]. Nevertheless, in analog circuitry design, it is very helpful to evaluate the dynamic behaviour of the device in terms of the frequency-independent SSEC parameters. This allows to address the importance of different magnitudes and geometry parameters (i.e. oxide thickness or reduction of the gate length) in the dynamic response. Furthermore, it is an important step in the calculation of noise parameters. The elements of the SSEC can be calculated from the $Y$ parameters [9].

In this work, we considered the SSEC of Fig. 5. The dotted box encloses the “intrinsic” equivalent circuit from the point of view of experimental measurements, in which the effect of contact resistances, capacitances and inductances was subtracted [10]. Nevertheless, it includes the effect of some parasitic capacitances that appear due to the device topology (represented by $C_{gd}$, $C_{gs}$, and $C_{ds}$). These capacitances are associated to the device geometry, and they can be evaluated from their zero current values (we considered them to be bias-independent). For the device under analysis, these values are $C_{gs}^{ext} = 214$ fF/mm, $C_{gd}^{ext} = 126$ fF/mm, and $C_{ds}^{ext} = 0$ fF/mm. Since these parasitic effects can not be included in a 2D model, we must add these capacitances to our MC results (corresponding to the shaded area in Fig. 5) in a post-processing stage [6] in order to perform a direct comparison between MC and experimental data. Therefore, the $Y$ parameters obtained by the MC method are recalculated by means of the following relationships [6]:

$$Y_{11} = Y_{11}^\prime + j\omega (C_{gs}^{ext} + C_{gd}^{ext})$$
$$Y_{12} = Y_{12}^\prime - j\omega C_{gd}^{ext}$$
$$Y_{21} = Y_{21}^\prime - j\omega C_{gd}^{ext}$$
$$Y_{22} = Y_{22}^\prime + j\omega (C_{ds}^{ext} + C_{gd}^{ext})$$

(1)

In this way, we obtain MC parameters that can be directly compared to the “intrinsic” experimental data.

Figure 6 shows the experimental data (lines) and the MC results (symbols) for the SSEC capacitances as a function of $V_{GS}$. The inset shows the $C_{gs}/C_{gd}$ ratio.

![Figure 6. SSEC intrinsic capacitances. The inset shows the $C_{gs}/C_{gd}$ ratio.](image)

First of all, it must be remarked that the MC results agree very accurately to the experimental data for the three capacitances. Furthermore, the dependence with the biasing is very well reproduced. As it can be observed in Fig. 6, $C_{gs}$ has the highest values for the gate voltages considered. For the lowest $V_{GS}$, the device operates in the depletion regime or in the weak inversion regime, and the capacitance corresponds in its main part to the depletion capacitance. As the gate voltage increases, the inversion layer appears [Figure 4 (a)] and the number of carriers under the gate at the source end of the channel increases, thus increasing the $C_{gs}$ capacitance. Nevertheless, from a $V_{GS}$ of around 0.75 V $C_{gs}$ reaches a saturation value due to the practically constant increase of charge with the gate voltage. Furthermore, the high values of charge in the overlap region indicate a strong influence of the overlap capacitance on the total $C_{gs}$ in this range.

$C_{gs}$ maintains a quite constant value, except for the highest $V_{GS}$ (from 1.0 V), for which it tends to increase slightly. This is due to the appearance of a small concentration of electrons in the depletion region at the drain.
side of the channel, when the device begins to leave the saturation regime [Fig. 4 (a)].

Concerning the values of $C_{ds}$, it must be remarked that whereas in a bulk MOSFET this capacitance can show significant values [5], for the FDSOI device it has very low values as compared to the other capacitances. This indicates a reduced influence of the substrate coupling (due to the presence of the buried oxide) which is of great importance in high frequency applications.

The $C_{gd}/C_{gs}$ ratio is a magnitude of interest in the study of a SOI MOSFET. As it can be seen in the inset, our MC simulator successfully predicts this ratio for the gate voltages studied. The maximum value (3.5 aprox.) is reached for $V_{gs} = 0.625$ V.

Figure 7 shows the values of the intrinsic transconductance, $g_{mi}$ and the intrinsic output conductance, $g_{di}$ [Fig. 7 (a)] together with the cut-off frequency, $f_T$ [Fig. 7 (b)] as a function of $V_{gs}$ for $V_{ds} = 1.0$ V. Lines represent the experimental data, whereas symbols represent the MC results. The values for $f_T$ were obtained by means of the following relationship [11]:

$$ f_T = \frac{g_{mi}}{2\pi(C_{gs} + C_{gd})} \quad (2) $$

As it can be seen in Fig. 7 (a), $g_{mi}$ reaches a maximum value around 475 S/m for $V_{gs} = 1.0$. With regard to $f_T$, it shows its maximum value (around 48 GHz) for $V_{gs} = 0.8$ V. Our MC simulator reproduces perfectly the dependence of these experimental parameters with the biasing, although in this case it slightly underestimates $g_{mi}$ for high $V_{gs}$ and the values of $g_{di}$ in general (due to the relatively flat MC output characteristics). Because of the slight underestimation of $g_{mi}$, $f_T$ is also a bit lower in the case of MC results as compared to the experimental data.

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References