An Ultra-Thin Polycrystalline-Silicon Thin-Film Transistor with SiGe Raised Source/Drain

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Introduction

- To integrate driving circuits in AMLCD, poly-Si TFTs need:
  - Large drive current
  - Higher breakdown voltage
- The use of thin channel TFTs ($\leq 50$nm) is beneficial for higher current drive.
Introduction

- However, disadvantages of thin channel include
  - poor S/D contact
  - Large series resistance
  - Smaller horizontal breakdown voltage

- An ideal TFT device structure should therefore consist of a thin active channel region, while maintaining a thick S/D region
Proposed Structure

- Thin channel (20 nm) and thick S/D (120nm)
- Oxide spacer is used to isolate S/D from poly-Gate
- SiGe is selectively grown by UHVCVD
Advantages of proposed structure – thin channel and thick S/D
- Reduced S/D resistance
- Higher turn-on current
- Breakdown voltage, $V_{BD}$ increases
- Lower leakage current (trap state in bulk decreases)
- Self-aligned in nature
- No additional masks are required
Results and discussions

- TEM photo
  - Thickness of poly-SiGe was about 100 nm grown by UHVCVD
  - Growth condition
    - SiH$_4$ = 20 sccm
    - GeH$_4$ = 5 sccm
    - Pressure < 1 mTorr
    - Temp = 550 °C
    - Time = 4 hours
Results and discussions

- Transfer and output characteristics
Rs Effects

- The total resistance \( R_{\text{total}} \) from drain to source is a composition of source/drain \( R_{\text{S/D}} \) and channel \( R_{\text{channel}} \):
  \[ R_{\text{total}} = 2R_{\text{S/D}} + R_{\text{channel}} \]

- The measured resistivity \( \rho \) for S/D regions:
  - Channel thickness = 20 nm (activation, RTA 850 °C for 20 sec)
  - \( \rho \approx 7 \ \Omega\text{-cm} \) for conventional TFTs
  - \( \rho \approx 3.0 \times 10^{-3} \ \Omega\text{-cm} \) for SiGe RSD TFTs
Results and discussions

- Dimensional effects

\begin{align*}
\text{Conventional} \\
W=10\mu m \\
V_g (V) &-5 &0 &5 &10 &15 &20 &25 &30 \\
I_d (A) &10^{-12} &10^{-11} &10^{-10} &10^{-9} &10^{-8} &10^{-7} &10^{-6} \\
L=10\mu m &
L=8\mu m &
L=5\mu m &
L=3\mu m &
L=1\mu m \\
\text{SiGe RSD} \\
W=10\mu m \\
V_g (V) &-5 &0 &5 &10 &15 &20 &25 &30 \\
I_d (A) &10^{-12} &10^{-11} &10^{-10} &10^{-9} &10^{-8} &10^{-7} &10^{-6} \\
L=10\mu m &
L=8\mu m &
L=5\mu m &
L=3\mu m &
L=1\mu m \\
\end{align*}
Results and discussions

- **Drain breakdown voltage, \( V_{BD} \)**
  - The scaling of channel dimensions in poly-Si TFTs is critical to realize high density AM-LCD. To this end, the drain breakdown voltage requirement must be satisfied.
  - \( V_{BD} \) is defined as the drain voltage when drain current \( I_d = 2\, \text{nA} \) @ \( V_g = 5\, \text{V} \).
**Results and discussions**

- **Breakdown voltage**
  - $V_{BD}$ is higher for SiGe RSD TFTs due to smaller drain horizontal electric field.
  - Larger degradation of $V_{BD}$ was observed for conventional TFTs as channel length decreases.
Conclusions

- The proposed novel SiGe Raised S/D TFTs feature high turn-on current and on/off current ratio, compared to conventional TFTs.

- Moreover, the drain breakdown voltage for the proposed TFTs is significantly improved.

- The new structure is self-aligned in nature and no additional masks are needed and is ideally suitable for high-density and high-performance driver circuits for AMLCD applications.