Controlling STI-related parasitic conduction in 90 nm CMOS and below

E. Augendre, R. Rooyackers, D. Shamiryan, C. Ravit*, M. Jurczak, G. Badenes+

IMEC, Leuven
*Philips Research, Leuven
+Institut de Ciències Fotòniques, Barcelona
From the isolation point of view
Scaling goes with…

limiting parasitic conduction

Poly Si

STI Si

0.25µm CMOS 90 nm CMOS
Controlling STI-related parasitic conduction in 90 nm CMOS

Origin of the parasitic lateral conduction

Two routes to reduce it

Implementation in a 0.18 µm CMOS flow

Application down to 90 nm CMOS
Parasitic conduction & electric field crowding

Field crowding causes local Vth lowering
- Subthreshold hump
- Enhanced Vth(W) roll-off

→ Increase corner radius (sidewall reoxidation)

→ Reduce gate wrap-around
Against gate wrap around: T-shape STI

- Straight profile STI
- Nitride etch
- +polymerisation
- T-shape STI
- Gate wrap-around is minimized
Against gate wrap around: limited HF time

Gate wrap-around is minimized

(pre-gate oxide)
Comparison T-shape / reduced HF

- 150 nm nitride
  - 15 nm pad oxide
    - 400 nm trench
      - Straight profile
        - Long HF
        - Short HF
    - T-shape
      - Short HF
        - Long HF
        - Short HF
    - 325 nm trench
      - Straight profile
        - Short HF
    - 250 nm trench
      - Straight profile
        - Short HF

Rest of the processing: 0.18 μm CMOS flow
Active area width

Offset in active area width relative to mask dimension

- Straight profile: -19 nm (σ = 5 nm)
- T-shape: +15 nm (σ = 9 nm)

}  

Lines are 34 nm larger per side with T-shape
Oxide recess depth estimate (from silicided line resistance)

STI oxide thickness

- 400 nm trench
  - Straight profile: 364 nm, 26 nm, 26 nm
  - T-shape: 380 nm, 13 nm, 9 nm
- 325 nm trench
  - Straight profile: 377 nm, 12 nm, 12 nm
- 250 nm trench
  - Straight profile: 322 nm, 12 nm, 12 nm

© imec 2002
Morphology summary

Oxide recess
- Decreases significantly with reduced HF
- Is yet more reduced with T-shape STI

Trench filling
- 400 nm trenches were filled slightly below target
- 325 and 250 nm trenches were filled on target

Active area width
- Active area lines are ~34*2 nm wider with T-shape STI
- Width control is degraded by the polymerization step
Short HF does not degrade GOI

Pre-gate oxide influences gate oxide integrity (GOI)

Time-dependent dielectric breakdown on overlapping capacitors

- Charge to breakdown independent of perimeter
- No extrinsic failures
Short HF suppresses subthreshold hump

Subthreshold hump is visible with long HF

Disappears with short HF

→ Hump attributed to gate wrap-around

→ Wrap-around reduced enough with short HF
Short HF improves Vth(W) roll-off

Strong roll-off caused by:
- gate wrap around
- incomplete oxide filling

→ T-shape STI more resistant towards incomplete STI filling

→ Equal control with properly filled straight profile

→ Uniformity better with straight profile
Application of short HF down to 90 nm CMOS

- 15 nm oxide
- 150 nm nitride

- 0.18 µm CMOS
  - 400 nm STI straight profile reduced HF
  - tox = 3.5 nm furnace oxynitride
  - soak RTA 1070°C

- 0.13 µm CMOS
  - 350 nm STI straight profile reduced HF
  - tox = 2.0 nm furnace oxynitride
  - soak RTA 1050°C

- 90 nm CMOS
  - 250 nm STI straight profile reduced HF
  - tox = 1.5 nm RPN nitridation
  - spike RTA 1100°C
Total hump suppression

Short HF suppresses subthreshold hump for all technologies

0.18 µm process could be most sensitive to biased-body hump appearance (higher body factor)
Well controlled narrow channel effects

The same isolation architecture fits down to 90 nm technology

Scaling improves narrow channel effects.

This might be explained by reduced B redistribution.
Conclusions

Implanting well through reoxidised pad-oxide is effective reducing gate wrap-around.

It preserves oxide integrity.

With well controlled trench filling, it is equivalent to T-shape STI, with improved uniformity.

When implemented in a 90 nm CMOS flow, it enables reducing Vth roll-off to 40 mV (between W=10 µm and W=0.11 µm).

Promising approach for coming technology nodes.
www.imec.be
Worldwide collaboration with more than 450 companies and institutes.
Appendix

Recess evaluation from salicided line (300 μm) resistance

- Si dimension known from SEM
- CoSi$_2$ sheet resistance known from Van der Pauw measurement
- Oxide recess assuming constant sheet resistance on the edge