UIS - Failure of DMOS Power Transistors

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Outline

• Unclamped Inductive Switching (UIS) - some facts

• Analytical Modelling Approach

• Numerical Device Simulation

• Conclusions & Outlook
Unclamped Inductive Switching (UIS): typical example

\[ i(t) = I_0 - \frac{V_{BR}}{L} \cdot t \]

**T on:** current \( i \) flows in channel of \( T \)

**T off:** avalanche \( \rightarrow \) heat is dissipated in \( T \) at rate \( V_{BR} \cdot i \)
Unclamped Inductive Switching: measuring the failure level

- Gate is turned off
- Current continues to flow
- Sudden drop in $V_{Drain}$ indicates device failure

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Unclamped Inductive Switching: measuring the failure level

Only a limited amount of heat can be dissipated without device damage.

- The maximum tolerable UIS-current is determined by the value of inductance $L$.

Measurement Setup

Limiting curve for safe UIS

\[
\log(I_{\text{Max}}) = -\log(L)
\]
Analytical Modelling Approach: From cell array to single cell

- Device consists of integrated cell array
- Experiment shows: failure occurs randomly somewhere inside the array
- Cells at the border are immune to UIS failure
  - Cells may be considered as equivalent
  - UIS-failure analysis restricted to one single cell in parallel with the rest of the array
Analytical Modelling Approach: Collective behavior of cell array

$I / n$ \[ I_{\text{cell1}} \] \[ \frac{\partial I}{\partial T} \] \[ T \] \[ I_{\text{cell1}} \]

$I / n$ \[ I_{\text{cell2}} \] \[ \frac{\partial I}{\partial T} \] \[ T \] \[ I_{\text{cell2}} \]

...\[ I / n \]

$I / n$ \[ I_{\text{cell}_n} \] \[ \frac{\partial I}{\partial T} \] \[ T \] \[ I_{\text{cell}_n} \]

\[ \frac{\partial I}{\partial T} < 0 \]
\[ \Rightarrow \text{stable operation} \]

\[ \frac{\partial I}{\partial T} > 0 \]
\[ \Rightarrow \text{unstable operation} \]

**ETM**: electrothermal model of device cell

**n-1 equivalent cells**

**1 different cell**

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Analytical Modelling Approach:
• Single Cell Model

• Electrothermal transport equations
• Reflecting boundary conditions at the side borders
• For downward heat transport, the cell is a semi-infinite, 1D solid
• Heat transport equation is linear
• Carrier recombination + generation are instantaneous compared to temperature evolution
• In the stable regime, only the avalanche current $j_{pav}$ is taken into account
• Electrical and thermal currents are 1D
Analytical Modelling Approach:
  • UIS stress without failure

UIS stress below instability limit:
  • Body diode is reverse biased
  • Avalanche breakdown occurs
  • Cells in parallel: $V_1=V_2=...=V_n$
  • For perfectly equivalent cells, also $I_1=I_2=...=I_n$
  • Actually, cells differ slightly from each other

• But, avalanche-induced current is temperature-stable in each individual cell: $\frac{\partial I_{av}}{\partial T} < 0$

→ total current uniformly distributed among all cells
Analytical Modelling Approach:
• UIS stress causing failure (qualitative)

UIS stress reaches instability limit:
• Heat is generated at spot A
• Temperature rises at A
• Device voltage rises
• Thermal diffusion
  → temperature also rises at B
  → $j_{n\text{Diff}}$ is enhanced
• Multiplication rate $M_{nB}$
  at spot B increases
  → further rise of $j_{n\text{Diff}}*M_{nB}$
• If $j_{n\text{Diff}}$ is the dominant contribution to I:

$$\frac{\partial I}{\partial T} > 0 \Rightarrow \text{unstable behavior, current filament}$$
$$\Rightarrow \text{device failure}$$
Analytical Modelling Approach

- UIS stress causing failure (quantitative)

\[
\begin{align*}
    j_{pav} &= j_{pDrain} \cdot M_p A(T_A, V_{SCR}) \\
    j_{nDiff} &= \frac{kT \cdot \mu_e(T)}{W_{av}} \cdot \left[ n_i^2(T) / N_{\text{base}} \cdot \exp\left( \frac{q(\Phi_{\text{sub}} - \Phi_{\text{ext}})}{kT} \right) \right] \\
    \Phi_{pBE} &\approx j_{pav} \cdot \frac{W}{q \mu_e(T) \cdot N_{\text{base}}} ; \quad \Phi_{nBE} \approx V_{Source} = 0
\end{align*}
\]

\[
I_{cell} = I_0 - \frac{V_{BR}}{L} \cdot t \\
\approx j_{nDiff} \cdot A_{Diff} \cdot M_n B(T_B, V_{SCR}) + j_{pav} \cdot A_{av}
\]

After heat at \( B \) has become significant:

\[
T_{B2} = c_V^{-1} \cdot V_{DS} \cdot j_{nDiff} \cdot A_{Diff} \cdot t + T_f
\]

since

\[
\frac{dj_{\text{avg}}}{dt} = \frac{\partial j_{\text{avg}}}{\partial T} \cdot \frac{\partial T}{\partial t} = \frac{\partial j_{\text{avg}}}{\partial T} \cdot c_V^{-1} \cdot V_{DS} \cdot j_{nDiff} \cdot A_{Diff}
\]

\{ \[ j_{nDiff} \gg j_{pav}, \frac{\partial j_{\text{avg}}}{\partial T} > 0 \} \Rightarrow \frac{\partial I}{\partial T} > 0
\]

\Rightarrow \text{unstable solution}
Numerical Device Simulation: constant current pulses

Motivation: Validation of the analytical model
Only one cell is simulated

Kink in temperature ➔ relocation of the hot spot!

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Numerical Device Simulation: constant current pulses

electron current density - formation of filament

temperature levels - relocation of the ‘hot spot’

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Numerical Device Simulation: constant current pulses

- Electron current from source-contact rises rapidly after relocation of hot spot
  \(\Rightarrow\) temperature ‘kink’ indicates onset of current instability

Maximum device temperature, currents at source-contact vs. time (I=1mA)
Numerical Device Simulation: constant current pulses

- Hole quasiFermi potential biasing emitter-base junction reaches only 0.2 V

Temperature and quasiFermi potentials at emitter-base junction vs. time (I=1mA)

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Numerical Device Simulation: constant current pulses - discussion

Analysis of electron diffusion current:

\[
\mathit{j_{nDiff}} = \frac{D_n(T)}{W_{Base}} \cdot \left[ \frac{n_i^2(T)}{N_{\text{base}}} \cdot \exp\left(\frac{q\Phi_{\text{pBE}} - \Phi_{\text{at}},n}{kT}\right) \right]
\]

• Emitter- base junction is forward-biased with \(0.2\,V\) \(\Phi_{\text{pBE}}\) only

• Diffusion coefficient decreases with temperature: \(D_n(T) = kT \cdot \mu_n(T) \propto T^{-0.5}\)

• But: Intrinsic density rises: \(n_i^2(T) \propto T^3 \cdot \exp(-E_i/kT)\)

\(\Rightarrow n_i(T)\) is dominating factor for the increase of \(j_{nDiff}\)

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Numerical Device Simulation: UIS stress

current + voltage transients with and without UIS-failure

electron, hole current + voltage transients with and without UIS-failure

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Conclusions

• Analytical modelling approach for the failure of DMOS Power Transistors under UIS stress conditions has been proposed

• Electrothermal device simulation of a single transistor cell demonstrates the appearance of a current filament due to UIS stress

• From the analytical model it can be deduced that filament formation implies unstable current crowding in one cell, leading eventually to device failure and damage

• $n_i(T)$ is the decisive factor for filament formation
Outlook

• Experimental corroboration of the model is still missing
• Accurate high-temperature physical models are still to be implemented in the simulation in order to quantitatively predict UIS-failure levels
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Failure Current square Pulse

\[ y = 60.792x^{0.584} \quad R^2 = 0.9993 \]

\[ y = 30.535x^{0.4828} \quad R^2 = 0.9976 \]