Tunnel barrier properties in polycrystalline-Si single electron transistors

Y. Furuta¹,⁴ H. Mizuta¹,⁴ T. Kamiya²,⁴ K. Nakazato¹,⁴
Y. T. Tan²,⁴ Z.A.K Durrani²,⁴ and K. Taniguchi³

¹)Hitachi Cambridge Laboratory, Hitachi Europe Ltd.
²)Microelectronics Research Centre, University of Cambridge
³)Osaka University
⁴)CREST, JST (Japan Science and Technology)
Coulomb blockade in nanostructures

Electron transfer from conductor to a microscopic island and then on to another conductor.

Charging energy for one electron

\[ E_C = \frac{e^2}{2 C_\Sigma} \]

\((C_\Sigma\) : island capacitance)
Background and motivation

Poly-Si ~Naturally formed multiple-electron island~

Grain = Electron islands

Grain boundary (GB) = Tunnel junctions

Poly-Si film

Characterization of tunnel barrier at GB to establish “GB engineering technique”
Preparation of poly-Si film

Secco-etched poly-Si film used

Grain: 20 nm ~ 150 nm

Thermally grown 40 nm SiO₂

a-Si deposition: 50 nm at 550 °C

Phosphorus implantation

P: 20keV 3x10¹⁴ cm⁻²

Solid-phase crystallization

Annealing at 850 °C 30 min in Ar
Poly-Si point contact transistor (PC-Tr)

PC-Tr structure
width : 30 - 50 (nm)
length : 30 - 50 (nm)

Thermally grown 40 nm SiO₂

a-Si deposition: 50 nm at 550 °C

Phosphorus implantation
P : 20keV 3x10¹⁴ cm⁻²

Solid-phase crystallization
Annealing at 850 °C 30 min in Ar

E-beam lithography

Electrical isolation by RIE
(SiCl₄/CF₄ 20 sccm each)

Oxidation
1000 °C 15 min in dry O₂

As-prepared PC-Tr Oxidized PC-Tr
Electrical characteristics of as-prepared PC-Trs

NO Coulomb blockade (CB) effect observed (> 4.2K)
Electrical characteristics of oxidized PC-Trs

Type A ($V_T \leq 5$ meV)  Type B ($V_T > 5$ meV)

Oscillation period  Similar  Distributed

P/V current ratio  Small  Large
## As-prepared vs oxidized PC-Trs

<table>
<thead>
<tr>
<th></th>
<th>As-prepared PC-Tr</th>
<th>Oxidized PC-Tr</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>XTEM</strong></td>
<td><img src="image1" alt="As-prepared XTEM" /></td>
<td><img src="image2" alt="Oxidized XTEM" /></td>
</tr>
<tr>
<td>Poly-Si BOX</td>
<td>40 nm</td>
<td>40 nm</td>
</tr>
<tr>
<td>As-prepared PC-Tr</td>
<td>50 nm</td>
<td>Poly-Si BOX</td>
</tr>
<tr>
<td>Oxidized PC-Tr</td>
<td>18 nm</td>
<td></td>
</tr>
<tr>
<td><strong>I-V characteristics</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grain</td>
<td>20 nm ~ 150 nm</td>
<td></td>
</tr>
<tr>
<td>Tunnel capacitance</td>
<td>~ 80 aF</td>
<td>Tunnel capacitance</td>
</tr>
<tr>
<td>No CB effect</td>
<td></td>
<td>CB effect up to</td>
</tr>
</tbody>
</table>

- **As-prepared:**
  - Poly-Si BOX: 50 nm
  - Tunnel capacitance: ~ 80 aF
  - No CB effect

- **Oxidized:**
  - Poly-Si BOX: 18 nm
  - Tunnel capacitance: ~ 5 aF
  - CB effect up to ~ 40K
Temperature dependence of resistances
Characterization of GB barrier height

As-prepared PC-Tr

Oxidized PC-Tr

The mean potential barrier slightly increases after oxidation

The potential barrier distribution

As-prepared PC-Trs:
- Linear I-V PC-Trs
- Nonlinear I-V PC-Trs

Oxidized PC-Trs:
- Type A ($V_T \leq 5$ meV)
- Type B ($V_T > 5$ meV)
Evaluation of electron island size

2D capacitance calculator

Gate

S

Gate

D

Calculated capacitance

\[ \Delta V_G = \frac{e}{C_G} \quad V_T = \frac{e}{C_{\Sigma}} \]

Experimental data

Type A (\( V_T \leq 5 \text{ meV} \))

Type B (\( V_T > 5 \text{ meV} \))
Evaluation of electron island size

<table>
<thead>
<tr>
<th></th>
<th>Island size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device A</td>
<td>~ 40 nm</td>
</tr>
<tr>
<td>Device B</td>
<td>~ 3 nm</td>
</tr>
</tbody>
</table>

Type A ($V_T \leq 5$ meV)
- Similar to channel length

Type B ($V_T > 5$ meV)
- Largely distributed

2D capacitance calculator

Calculated capacitance

Experimental data

\[ \Delta V_G = \frac{e}{C_G} \quad V_T = \frac{e}{C_\Sigma} \]
Channel length dependence of island size

Oxidized PC-Trs : Type A ($V_T \leq 5$ meV)

- $T = 4.2K$
- $W = 50$ nm

Pattern-dependent oxidation (PADOX)*

Evaluation of tunnel barrier thickness

Numerical calculation
Transfer matrix method

Tunnel resistance $R_T$
Barrier height $qV_B$

Oxidized PC-Trs : Type B ($V_T > 5$ meV)
Tunnel barrier thickness $d : 3 \sim 4$ nm
High resolution XTEM image of poly-Si film

Before oxidation

After oxidation

SiO_x > ~ 2 nm

Oxidized PC-Trs : Type B (V_T > 5 meV)

Selective oxidation along GB
P/V ratio & barrier height vs. Tunnel resistance

- Good P/V current ratio
  - Tunnel resistance > 1MΩ
    - Thicker tunnel barrier
    - Small tunnel capacitance
  - Large coulomb gap
Further improvement of tunnel barriers

Higher $qV_B$ at GB

Multi-step oxidation

Dry oxidation at 650°C/750°C, 30min
Annealed at 1000°C in Ar ambient

Small tunnel capacitance

- Smaller grain
- Thicker barrier

nc-Si film

$V_B \sim 170$ meV

RT conductance oscillation

Summary

As-prepared PC-Trs
Nonlinear I-V characteristics due to discrete GB
No CB effect > 4.2K

Oxidized PC-Trs
CB effect < ~40K
Formation of thick SiO\textsubscript{x} tunnel barriers In channel
Reduction of tunnel capacitance

Tunnel barrier
- Selective oxidation along GB
- PADOX-mode oxidation

Tunnel barrier optimization needed for further improvement