The Four-Gate Transistor

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The Four-Gate Transistor

- Introduction
- G⁴-FET structure
- Measured characteristics
- Depletion regime simulations
- Conclusion
Introduction

• From Double-Gate to Multiple Gates: 4-Gates is a maximum
• The G⁴-FET is a new 4-Gate transistor
• A 4-Gate transistor without specialized processing
• New opportunities (logic functions, RF, analog circuit mixed-voltage/mixed-signal)
• Provide new physical concept opportunities
The G⁴-FET Structure

- MOS Source/Drain → Lateral junctions
- MOS Body contacts → Source/Drain
- MOS length → G⁴-FET width
- MOS width → G⁴-FET length

Regular Partially-Depleted (PD) MOSFET with body contacts

Aerial View
The G₄-FET Structure

- Accumulation mode transistor
- Regular PD process

Current flow perpendicular to cross section

Cross-section View

Aerial View
Measured I-V Characteristics

N-channel MOS-JFET \((L = 1.5\,\mu\text{m}, W = 0.35\,\mu\text{m})\) with \(V_{\text{SUBSTRATE}} = 0\,\text{V}\)

- \(V_{\text{PG}} = \) poly-gate voltage
- \(V_{\text{JG}} = \) junction-gate voltage

- \(V_{\text{PG}} = 3\,\text{V}, V_{\text{JG}} = 0\,\text{V}\)
- \(V_{\text{PG}} = 2\,\text{V}, V_{\text{JG}} = 0\,\text{V}\)
- \(V_{\text{PG}} = 1\,\text{V}, V_{\text{JG}} = 0\,\text{V}\)
- \(V_{\text{PG}} = 0\,\text{V}, V_{\text{JG}} = -1\,\text{V}\)
- \(V_{\text{PG}} = 0\,\text{V}, V_{\text{JG}} = -2\,\text{V}\)

0.35um PDSOI
Measured I-V Characteristics
Junction-Gate Controls Device Cutoff

- Junction-gate can achieve device cutoff as top-gate is swept from depletion to accumulation
- Top-gate accumulation enhances conductivity

![Graph showing measured I-V characteristics with linear and semilog scales.](image)

**Linear Scale**

- $V_{SUBSTRATE} = 0V$
- $V_{DS} = 100mV$
- $V_{PG} = +1V$
- $V_{PG} = +1V$

**Semilog Scale**

- $V_{SUBSTRATE} = 0V$
- $V_{DS} = 100mV$
- $V_{PG} = +1V$
- $V_{PG} = -2V$
- $V_{PG} = -1V$
Measured I-V Characteristics
Top-Gate Cutoff Control

- Device cutoff achieved with top-gate depletion if junction-gate is also depleted
Measured I-V & gm Characteristics

Back-Gate Depletion

- Back-gate depletion enables full depletion (device completely switched off)
- Exotic transconductance characteristics

**Semilog Scale**

- $V_{SUBSTRATE} = -20V$
- $V_{DS} = 100mV$
- $V_{PG} = +1V$
- $V_{PG} = 0V$
- $V_{PG} = -1V$
- $V_{PG} = -2V$

**Linear Scale (g_m vs. V_JG)**

- $V_{SUBSTRATE} = -20V$
- $V_{DS} = 100mV$
- $V_{PG} = 0V$
- $V_{PG} = +1V$
- $V_{PG} = -1V$
- $V_{PG} = -2V$

**0.35um PDSOI**
Measured I-V Characteristics
Back-Gate Accumulation

- Back-gate accumulation prevents device cutoff
- Large currents are possible
- Junction-gate maintains current magnitude control but cannot force cutoff

**0.35um PDSOI**
2-D Simulations – Wide Channel

\[ W = 10 \, \mu m; \quad N_A = 2.10^{20} \, cm^{-3}; \quad N_D = 5.10^{17} \, cm^{-3} \]

\[ V_{G1} = -1 \, V \]

\[ V_{G2} = 0 \, V \]

Front channel depletion

Front & back channel depletion

- Conductive plate with adjustable thickness
- Negligible junction effect (mainly MOS operation without JFET effect)

Color Legend:
- Green ⇒ not depleted
- Pink ⇒ totally depleted
- Yellow ⇒ accumulated
2-D Simulations – Narrow Channel
Top-Gate Influence

- $V_G2 = 0$ V
- $V_G1 = +0.5$ V
- $V_J = 0$ V
- $W = 0.3 \mu m$; $N_A = 2.1 \times 10^{20}$ cm$^{-3}$; $N_D = 2.1 \times 10^{17}$ cm$^{-3}$

- $V_J$ and $V_G1$ grounded: no full depletion
- $V_G1$ in accumulation: conduction in the whole film
- $V_G1$ in depletion: narrow conductive wire

Color Legend:
- Green ⇒ not depleted
- Pink ⇒ totally depleted
- Yellow ⇒ accumulated

Narrow Conducting Wire
2-D Simulations – Narrow Channel
Depleted Back-Gate

- Full depletion is easily achieved
- Front-gate accumulation maintains the channel

Color Legend:
Green ⇒ not depleted
Pink ⇒ totally depleted
Yellow ⇒ accumulated
2-D Simulations – Narrow Channel
Accumulated Back-Gate

- Front-gate accumulated
  ⇒ high current (2 channels + volume)
- Front-gate depleted: possible current modulation by $V_J$

Color Legend:
Green ⇒ not depleted
Pink ⇒ totally depleted
Yellow ⇒ accumulated
2-D Simulations – Narrow Channel
Junction-Gate Bias Influence

More negative $V_J$:
very narrow conductive path
$\Rightarrow$ full depletion
$\Rightarrow$ off-state regime

Color Legend:
Green $\Rightarrow$ not depleted
Pink $\Rightarrow$ totally depleted
Yellow $\Rightarrow$ accumulated
2-D Simulations – Narrow Channel
4-Gate Modulation of the Conductive Path

\[ V_{G1} = -2 \text{ V} \]
\[ V_{G2} = -25 \text{ V} \]
\[ V_J = -1.75 \text{ V} \]

- W = 0.3 µm; \( N_A = 2.10^{20} \text{ cm}^{-3}; \]
  \( N_D = 5.10^{17} \text{ cm}^{-3} \)

All gates in depletion:
- variable size of the wire
- variable position of the wire

• Conduction away from all interfaces
  ⇒ Anticipate very low flicker-noise
  ⇒ Extreme immunity to radiation?
  ⇒ Is this a quantum wire?

Color Legend:
Green ⇒ not depleted
Pink ⇒ totally depleted
Yellow ⇒ accumulated
G4-FET: Conclusion

• Novel device from a known technology.

• Takes advantage of SOI flexibility and isolation capabilities.

• Accumulation mode transistor enabling complete turn off and conduction path size control.

• High as well as low currents modulation.

• Electrically (not lithography) controlled Quantum wire.

• High breakdown voltage, low noise.

• Opens various application possibilities: 4-level logic, analog RF; mixed-voltage…