Future Trends in Intelligent Interface Technologies for 42V Battery Automotive Applications


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Overview

- Towards the 42V powernet
- Technology description
- Device performance
  - Vertical nDMOS
  - HV ESD protection structures
  - Flash EEPROM
- Ongoing development
- Conclusions
Towards the 42 V powernet

- No Charge Pump

- With 12V Charge Pump

42 V 50 V 58 V 68 V 70 V 80 V

Nominal Operating voltage

Maximum Operating voltage full lifetime (25y)

Maximum dynamic overvoltage (<1h)

ESD
Towards the 42V powernet

- Gate count increase from 5K to 30K
- OTP for calibration
- Flash EEPROM (32K to 256Kbytes)
- Robustness (T, HC, C/UIS, …)
- Increased ESD levels: min 4 kV HBM
- …
Focus on DMOS
I3T80 Technology

Basic I3T80

Optional Modules

- p-substrate

- HV Buried Layer Module
  - 2 masks: BLN-BLP

- n-epi

- Sinker module:
  - 2 masks: Nsink-Psink

- Pdrift module:
  - 1 mask

- CO35D-QLM: 18 litho steps + Analogue options

- Nresurf Layer
  - 1 mask

- Flash EEPROM

- Pbod module:
  - 1 mask

- Power metal
Vertical nDMOS

Graph showing the relationship between the number of gates and $R_{dsonA}$ (mΩ mm$^2$), with different dose levels indicated by different symbols.

- Dose 1x
- Dose 2x
- Dose 3x
- Dose 4x
- Dose 5x
- Dose 2x Opt
DMOS Benchmarking

Ron (mOhm*mm²) vs. Vbd (V)

- l3t80, Vgmax=3.3V
- ref [3], Vgmax=3.3V
- ref [4], Vgmax=9.0V
- ref [5], Vgmax=12.0V
ESD protection structures

I3T80 - automotive

- Operating Voltage Range
- Overvoltage range
- Breakdown

Current

Voltage

Supply
IO

Charge pump

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ESD protection structures

• Experimental TLP results on HV protection structures

<table>
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<tr>
<th>Applic</th>
<th>Vleak (V)</th>
<th>Vtrig (V)</th>
<th>It1 (µA/µm)</th>
<th>It2 (mA/µm)</th>
<th>Vhold (V)</th>
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<td>70</td>
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<td>22</td>
<td>~46</td>
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</table>

• In addition, ESD protection structures for LV CMOS, OTP and Flash EEPROM drivers (~15V) are available.
ESD protection structures

![Graph showing ESD protection structures](image-url)
Flash EEPROM

- Embedded Flash based on the HIMOS® cell. Cell area of 3.8 \( \mu m^2 \). Only 3 (!) additional masks are needed.
  - Programming: Source side hot electron injection: 10 \( \mu s \)
  - Erase: Fowler-Nordheim injection into the drain: 0.5 s
  - Reading: 30 ns

![Flash EEPROM Diagram]
On-going developments

- Adding more devices to the library
  - Optimised NPN
  - Optimisation of Pbody module (±10% reduction in Ron).
  - Optimised 40-50-60V DMOS devices
    - nDMOS : Ron < 75 mΩ*mm²
    - pDMOS : Ron < 160 mΩ*mm²
  - 20-30V n/pDMOS transistors for 12/42V dual battery
  - 80V resurf nDMOS for LS applications : Ron < 80 mΩ*mm²

- Development of a new spin-off I3T technology dedicated for peripherals : I3T50
Conclusions

- I3T80: third generation Intelligent Interface Technology for future 42V battery automotive applications
  - Cheap and flexible (min. 5 add. masks, modular approach)
  - Floating logic (up to 80V)
  - Competitive DMOS up to 80V, using only the 7 nm gateox.
  - Bipolar devices, HV floating diode, Si bulk Zener diodes, …
  - A broad array of passive components
  - A wide variation of HV ESD protection structures
  - OTP at no extra cost
  - Flash EEPROM at the expense of only three extra masks