Through-Wafer Copper Electroplating for RF Silicon Technology

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Introduction

Through-wafer vertical vias are essential for:

- Advanced Si-RF devices
- 3-D integrated circuits
- 3-D sensor packaging
Novel via formation technology

a. Membrane and via formation
b. Cu evaporation
c. Backside lithography & plating
d. Bottom-up Cu electroplating
e. Frontside Cu evap. & plating
f. Cu wet etching
Via blocking effect

Cu evaporation

Cu source

10^{-6} mbar

T^0

Cu

Cu sputtering

Si

10^{-2} mbar

Cu target

Cu

Ar
Via formation technology

SEM image of a via bottom after copper evaporation

SEM image of a via bottom after the first copper electroplating.

SEM image of a 20µm x 20µm via after the bottom-up copper electroplating
Results – dry etching

Membrane: 25 – 150 µm thick
Vias: circles & squares (5 – 50 µm)
Results – via formation

SEM image of a 5 µm slit (wafer front side) after bottom-up copper plating.

SEM image of randomly (left) and regularly (right) distributed 20x20 µm² vias (wafer front side) after bottom-up copper plating.
Results – device formation

SEM image of a Cu inductor at the wafer backside

Optical image of a cross-talk isolation test structure (wafer front side) after final Cu etching step.
Results – resistance measurements

\[ \rho = 2.5 \times 10^{-5} \, \Omega \text{cm} \]

\[ R_{\text{total}} = 2R + 2R_1 + R_2 \]

(L varies)

SEM image of test structures for electrical characterization of through-wafer Cu plugs (wafer front side)
Conclusions

- New through-wafer Cu electroplating technique developed
- IC compatible post-process approach developed
- Through-wafer Cu plugs and novel RF devices realized successfully
- Via resistivity is very low
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