Impact of Deep N-well Implantation on Substrate Noise Coupling and RF Transistor Performance for Systems-on-a-Chip Integration

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1. Introduction
2. Deep Nwell Process Overview
3. Substrate Coupling Test Structures
4. S21 Isolation
5. Effect on RF Transistor Performance
6. Conclusions
Introduction

Deep N-well Process Overview

- STI formation
- Deep n-well implant
- N-well formation
- P-well formation
- Channel implants
- Gate insulator and gate electrode
- Pocket I/I + LDD I/I
- Sidewall spacer and S/D I/I
- Co salicidation
- BEOL
Deep N-well Process Overview

Deep N-well and P-well SIMS Profiles

Doping concentration (cm\(^{-3}\))

Depth (um)
CMOS with Deep N-well Technology

Transistor Cross-Sectional View
Deep N-well RF Isolation Test Structures

(a) Typical Layout*

(b) More Complex Layout*

* The authors would like to acknowledge Institute of Microelectronics (Singapore) VLSI department for the test structure layouts.
Diode-Type Substrate Coupling Structure in Deep N-well
Effect of Different Body Biasing Techniques on RF Isolation for P+ Noise Generators

S21 Isolation (dB)

Frequency (GHz)

G to S spacing: 280 µm
DNW Implant: P1E13/900KeV

- Background noise
- without DNW
- with DNW + unbiased P and N + no GR
- with DNW + unbiased P and N + grounded GR
- with DNW + unbiased P + grounded N and GR
- with DNW + unbiased P + grounded N + no GR
Effect of Different Body Biasing Techniques on RF Isolation for N⁺ Noise Generators

- S21 Isolation (dB)

Frequency (GHz)

- with DNW + P and N tied to Vdd + grounded GR
- with DNW + grounded P + N tied to Vdd + no GR
- with DNW + grounded P + unbiased N + grounded GR

G to S spacing : 280 µm
DNW Implant : P1E13/900KeV
Effect of Different Body Biasing Techniques on RF Isolation for N⁺ Noise Generators

-90  -80  -70  -60  -50  -40  -30  -20  -10  0  1  10

S21 Isolation (dB)

-90  -80  -70  -60  -50  -40  -30  -20  -10  0  1  10

Frequency (GHz)

G to S spacing : 50 \( \mu \)m
DNW Implant : P2E13/900KeV

- without DNW (P+ to P+)
- without DNW (N+ to P+)
- with DNW + unbiased P and N + no GR
- with DNW + unbiased P + N tied to Vdd + no GR
- with DNW + unbiased P and N + grounded GR
- with DNW + unbiased P + N tied to Vdd + grounded GR

- without DNW (P+ to P+)
- without DNW (N+ to P+)
- with DNW + unbiased P and N + no GR
- with DNW + unbiased P + N tied to Vdd + no GR
- with DNW + unbiased P and N + grounded GR
- with DNW + unbiased P + N tied to Vdd + grounded GR
Effect of Deep Nwell Dosage on RF Isolation for \( P^+ \) Noise Generators

**Graph Details:**
- **S21 Isolation (dB)**
- **Frequency (GHz)**

The graph shows the S21 isolation in decibels (dB) against frequency in gigahertz (GHz). The S21 isolation is measured with different dosages of Deep Nwell (DNW) and is compared to the isolation without DNW.

Key findings:
- The isolation without DNW is the poorest among the options.

**Additional Information:**
- **G to S spacing:** 280 µm
Thin-Gate Oxide MOSFETs in Deep N-well DC Characteristics

The diagram shows the DC characteristics of different types of MOSFETs, including:

- N-std
- N-DW
- P-std
- P-DW

The graphs display the relationship between the gate voltage (Vg) and the drain current (Ids) for various voltage levels (Vds) and well depths (Vtd).
Thick-Gate Oxide MOSFETs in Deep N-well DC Characteristics
Effect of Deep Nwell on the RF Transistor AC Characteristics Extracted from S-parameters

Capacitances (pF) vs. Frequency (GHz)

- NMOSFET
- \( L_{\text{gate}} = 0.25 \ \mu \text{m} \)
- \( W_{\text{finger}} = 9.58 \ \mu \text{m} \)
- \( N_{\text{finger}} = 8 \)
- \( V_{\text{ds}} = 2.5 \text{V} \)
- \( V_{\text{gs}} = 1.0 \text{V} \)

- \( C_{gd} \)
- \( C_{gb} \)
- \( C_{gg} \)

- w/o DNW
- w DNW
Effect of Deep Nwell on the RF Transistor AC Characteristics Extracted from CV Measurements

**Results:**

- **N+/P-well Junction Capacitance**
  - **Area:** 225 µm²
  - **Perimeter:** 60 µm
  - **Frequency:** 100 KHz
  - **Dot:** with Deep Nwell
  - **Line:** without Deep Nwell

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**Graphs:**

- **NPW1_40.CV**
  - **P/A=6.00E-05/2.25E-10**
  - **T=40.0°C**
  - **Max Err% = 0.73**
  - **Rms Err% = 0.42**

- **NPW1_25.CV**
  - **P/A=6.00E-05/2.25E-10**
  - **T=25.0°C**
  - **Max Err% = 1.24**
  - **Rms Err% = 0.91**

- **NPW1_125.CV**
  - **P/A=6.00E-05/2.25E-10**
  - **T=125.0°C**
  - **Max Err% = 1.17**
  - **Rms Err% = 0.9**

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Chartered semiconductor manufacturing
Comparison of RF Transistor High Frequency Characteristics with and without Deep N-well

Red : without Deep N-well
Blue : with Deep N-well

S11

S12

S21

S22

freq

freq

freq

freq

H21

REAL [E-3]

Unilateral Gain
Effect of Deep N-well on RF Transistor Figures-of-Merit

- NMOSFET
  - $L_{\text{gate}} = 0.25 \ \mu\text{m}$
  - $W_{\text{finger}} = 9.58 \ \mu\text{m}$
  - $N_{\text{finger}} = 8$
  - $V_{\text{ds}} = 2.5V$

- $f_{\text{max}}$
- $f_{\text{t}}$

- $I_{\text{ds}}$ per unit width (mA/$\mu$m)

- Frequency (GHz)

- w/o DNW
- w DNW
Comparison of RF Transistor HF Noise Characteristics with and without Deep N-well

Red : without Deep N-well

Blue : with Deep N-well

Triode

Frequency (GHz)

NFmin (dB)

Saturation

Frequency (GHz)

NFmin (dB)

NMOS Transistor
Lf=0.18\,\mu m
Wf=5\,\mu m
Nf=16
Vgs=1.2V
Vds=0.6V

NMOS Transistor
Lf=0.18\,\mu m
Wf=5\,\mu m
Nf=16
Vgs=1.8V
Vds=1.8V

w/o DNW
+ w DNW

w/o DNW
+ w DNW
Comparison of RF Transistor 1/f Noise Characteristics with and without Deep N-well

- **NMOS Transistors**
  - \( L_{\text{gate}} = 0.18 \mu m \)
  - \( N_{\text{finger}} = 16 \)
  - \( L_{\text{finger}} = 5 \mu m \)
  - \( V_{ds} = 0.7V \)
  - \( V_{gs} = 1.8V \)

**Triode**

**Saturation**

\( S_{id} (A^2/Hz) \)

- **with DNW**
- **w/o DNW**
Vertical NPN Bipolar from the 0.18 µm Deep N-well Technology

- $V_A = 22V$
- $BV_{CEO} = 6V$
- $BV_{CBO} = 17V$

$A_E : 5X5 \, \mu m^2$
1. Deep n-well is effective in isolating substrate coupling for NMOSFET

2. Maximum of 35 dB isolation at 100 MHz obtained with deep n-well plus grounded nwell and p+ guard ring, using deep n-well dose and implant energy of P1E13 @ 900 KeV

3. Deep n-well process with optimum dosage and energy will not impact the dc, ac, rf, and noise performance

4. Vertical NPN bipolar with beta of 14 can be obtained from the deep n-well technology