Impact of Deep N-well Implantation on Substrate Noise Coupling and RF Transistor Performance for Systems-on-a-Chip Integration

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Presented by K. W. Chew

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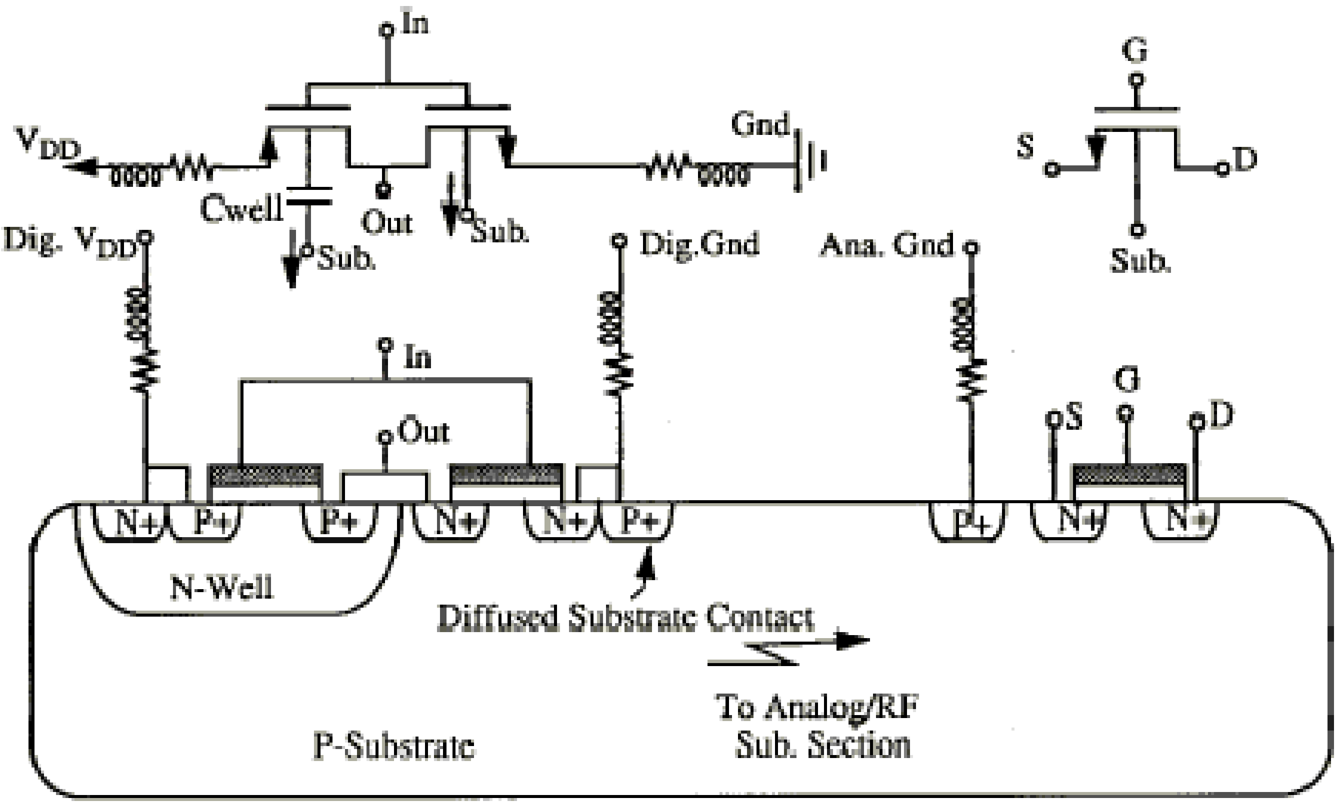
Outline

1. Introduction
2. Deep Nwell Process Overview
3. Substrate Coupling Test Structures
4. S21 Isolation
5. Effect on RF Transistor Performance
6. Conclusions

Introduction

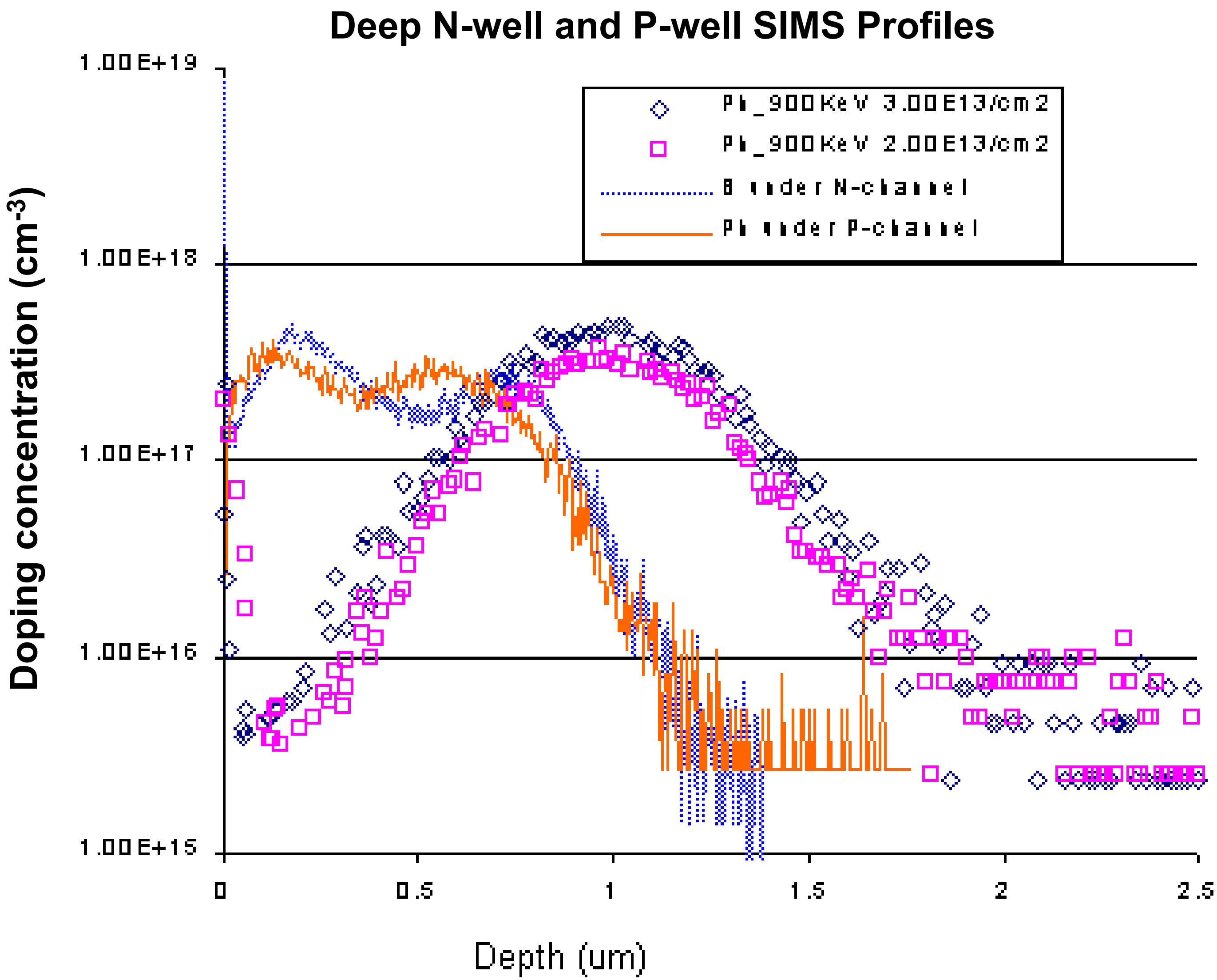


Source : IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, pp. 314-323, Mar. 1998

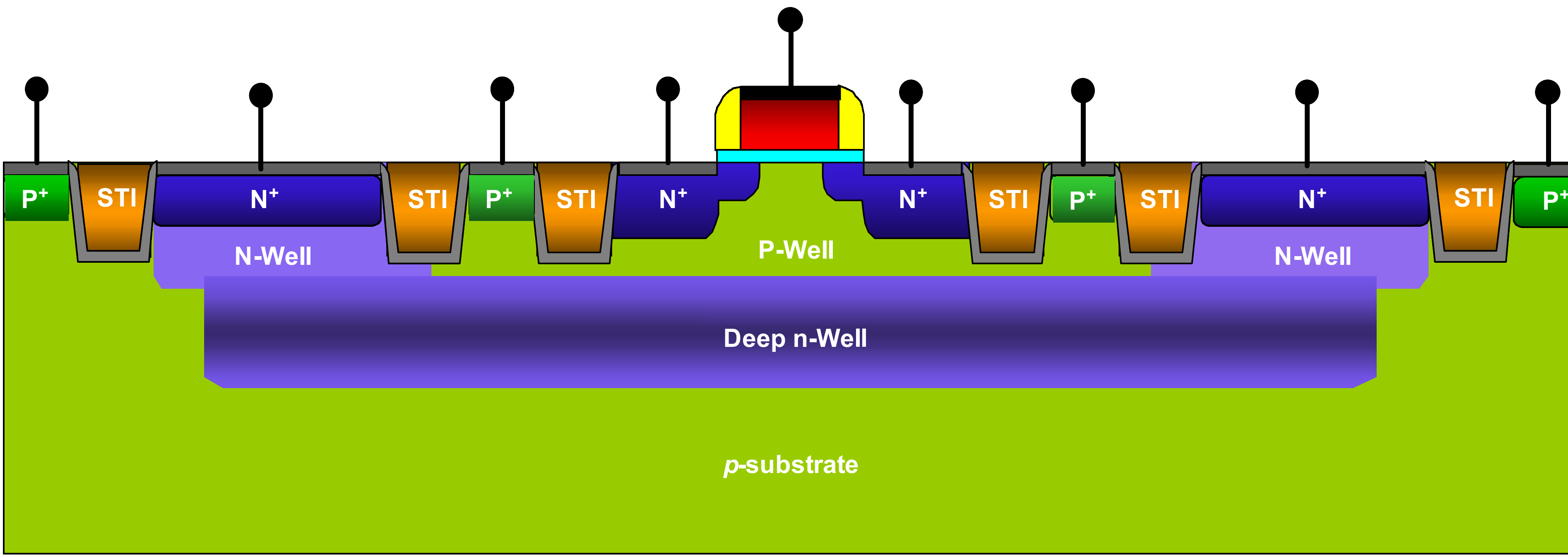
Deep N-well Process Overview

- STI formation
- **Deep n-well implant**
- N-well formation
- P-well formation
- Channel implants
- Gate insulator and gate electrode
- Pocket I/I + LDD I/I
- Sidewall spacer and S/D I/I
- Co salicidation
- BEOL

Deep N-well Process Overview



CMOS with Deep N-well Technology



Transistor Cross-Sectional View

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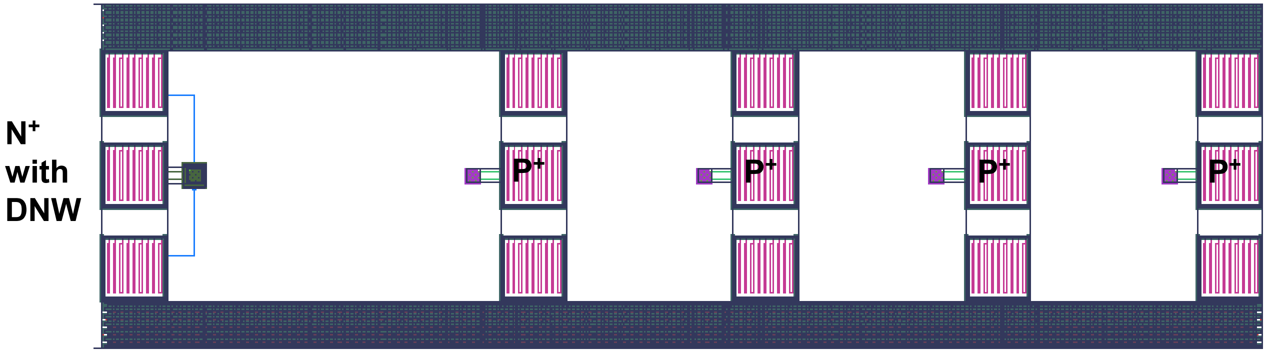
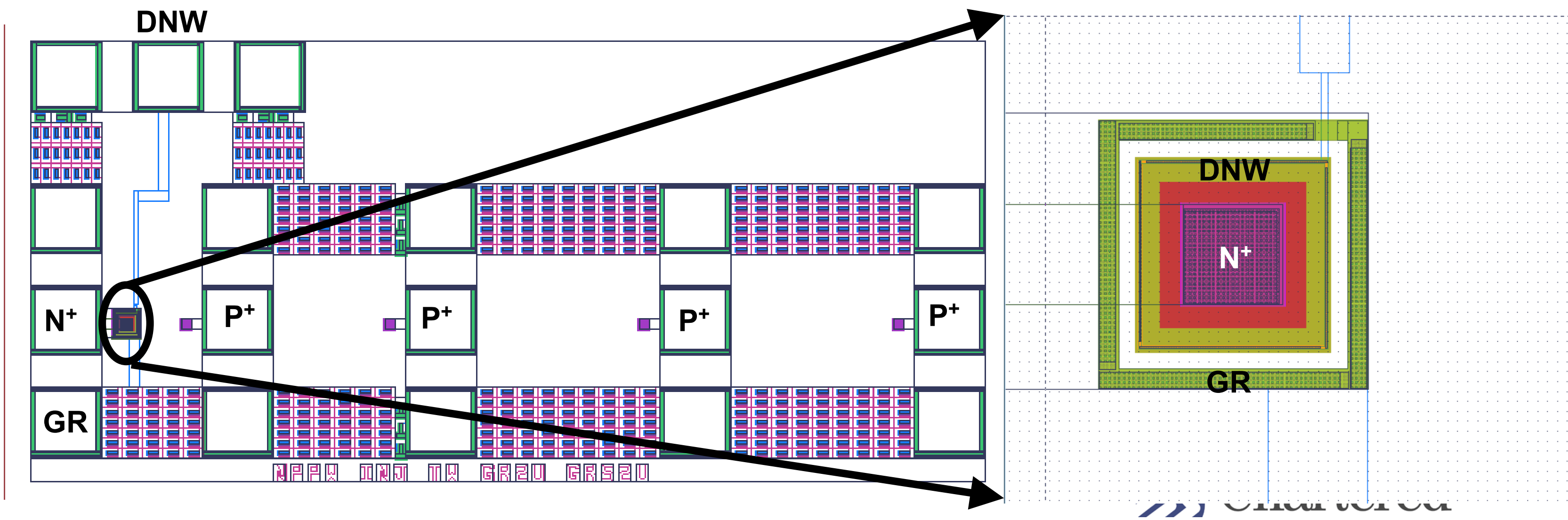
Deep N-well RF Isolation Test Structures

(a) Typical Layout*

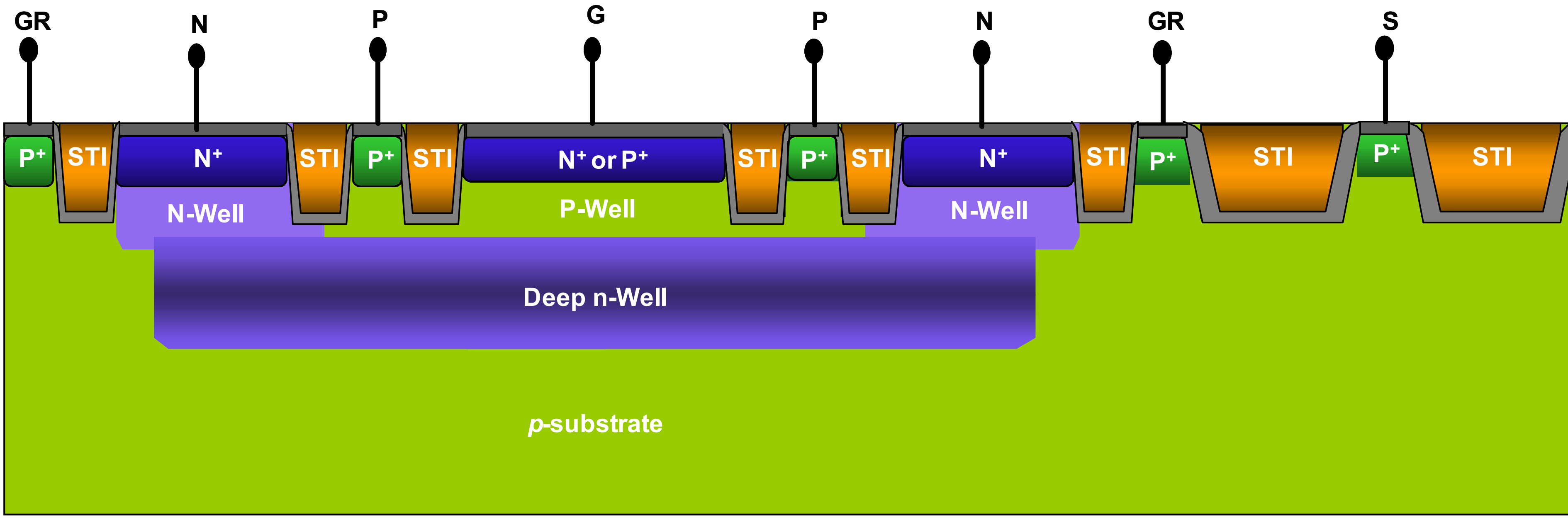


(b) More Complex Layout*

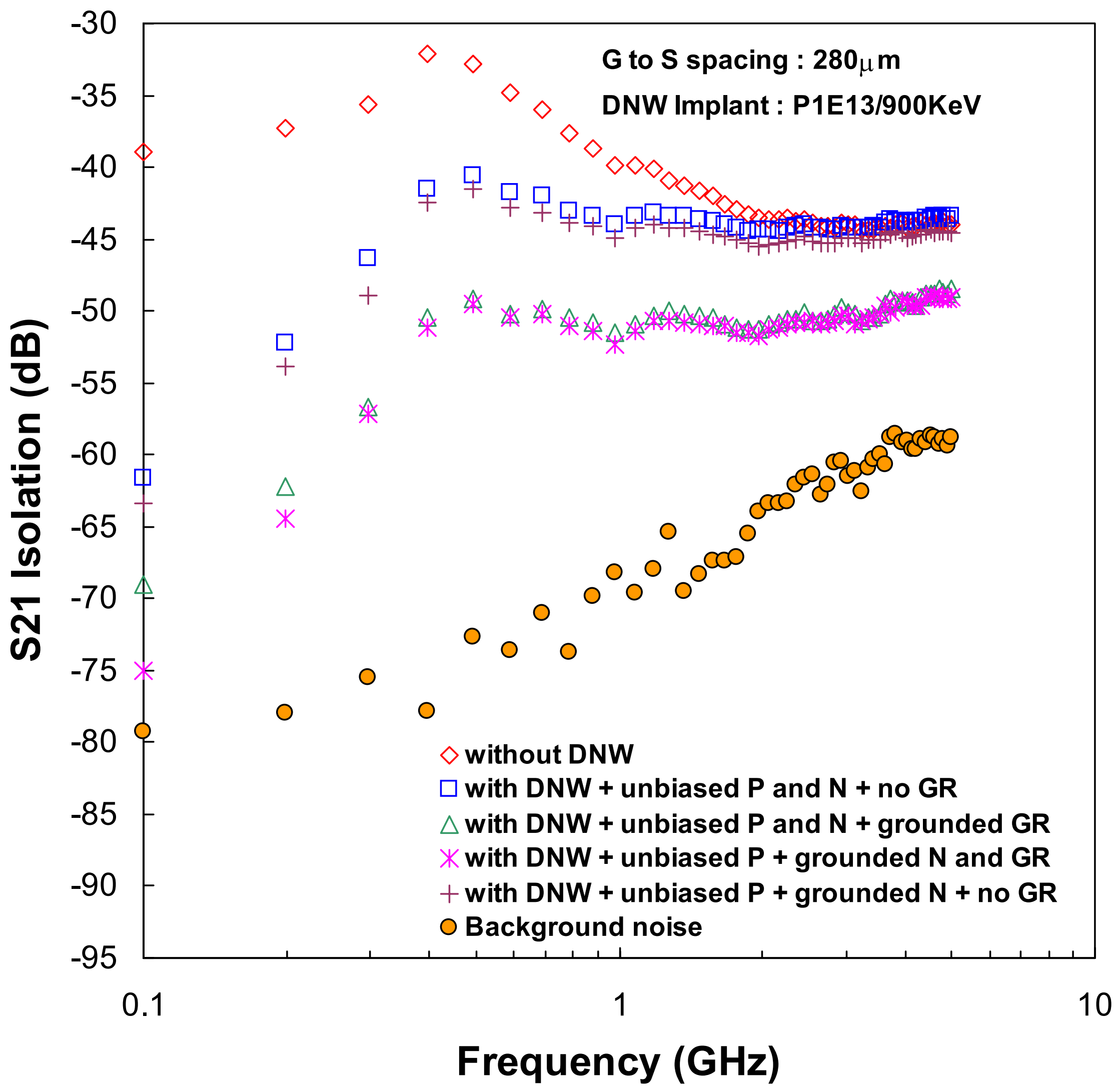


* The authors would like to acknowledge Institute of Microelectronics (Singapore) VLSI department for the test structure layouts

Diode-Type Substrate Coupling Structure in Deep N-well



Effect of Different Body Biasing Techniques on RF Isolation for P+ Noise Generators



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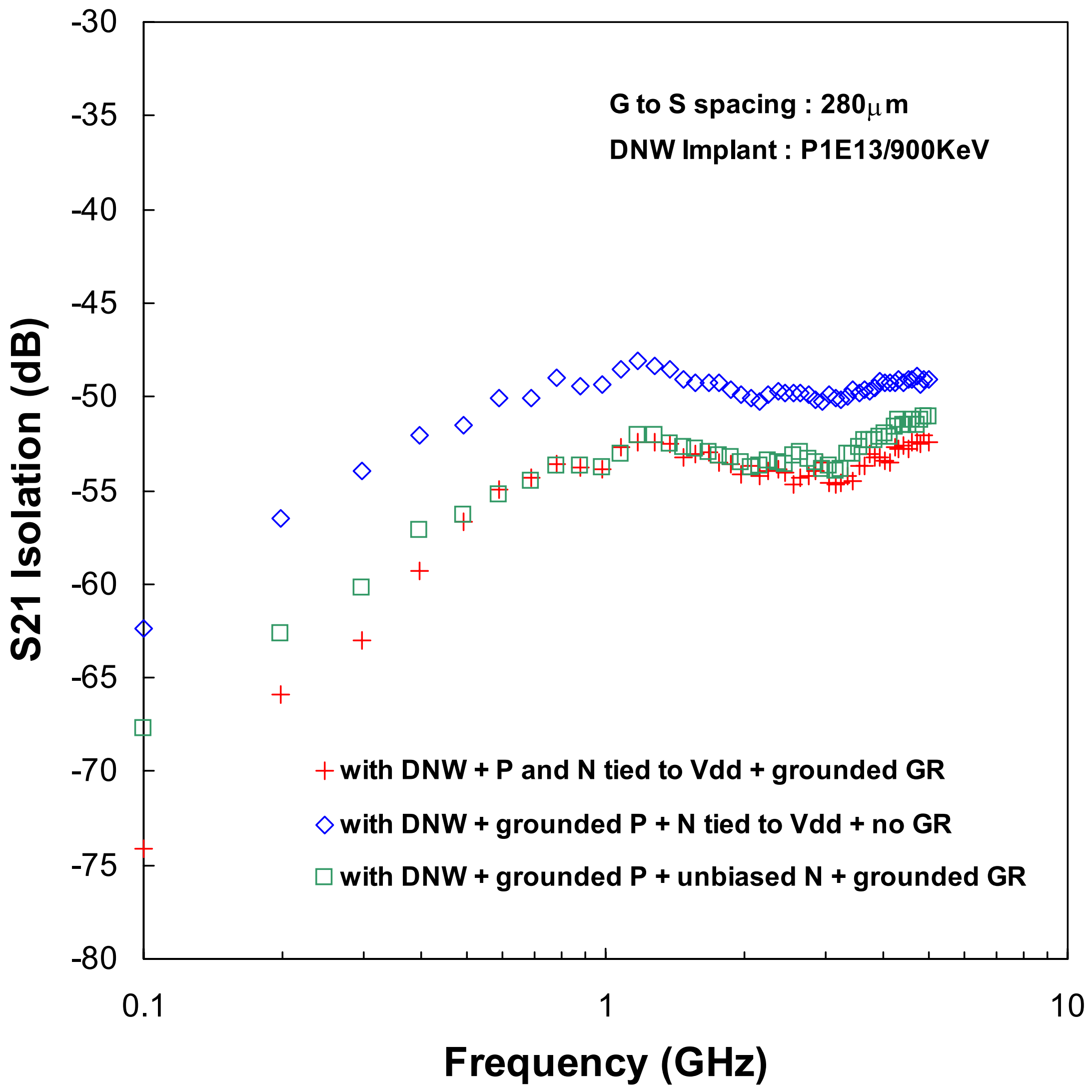
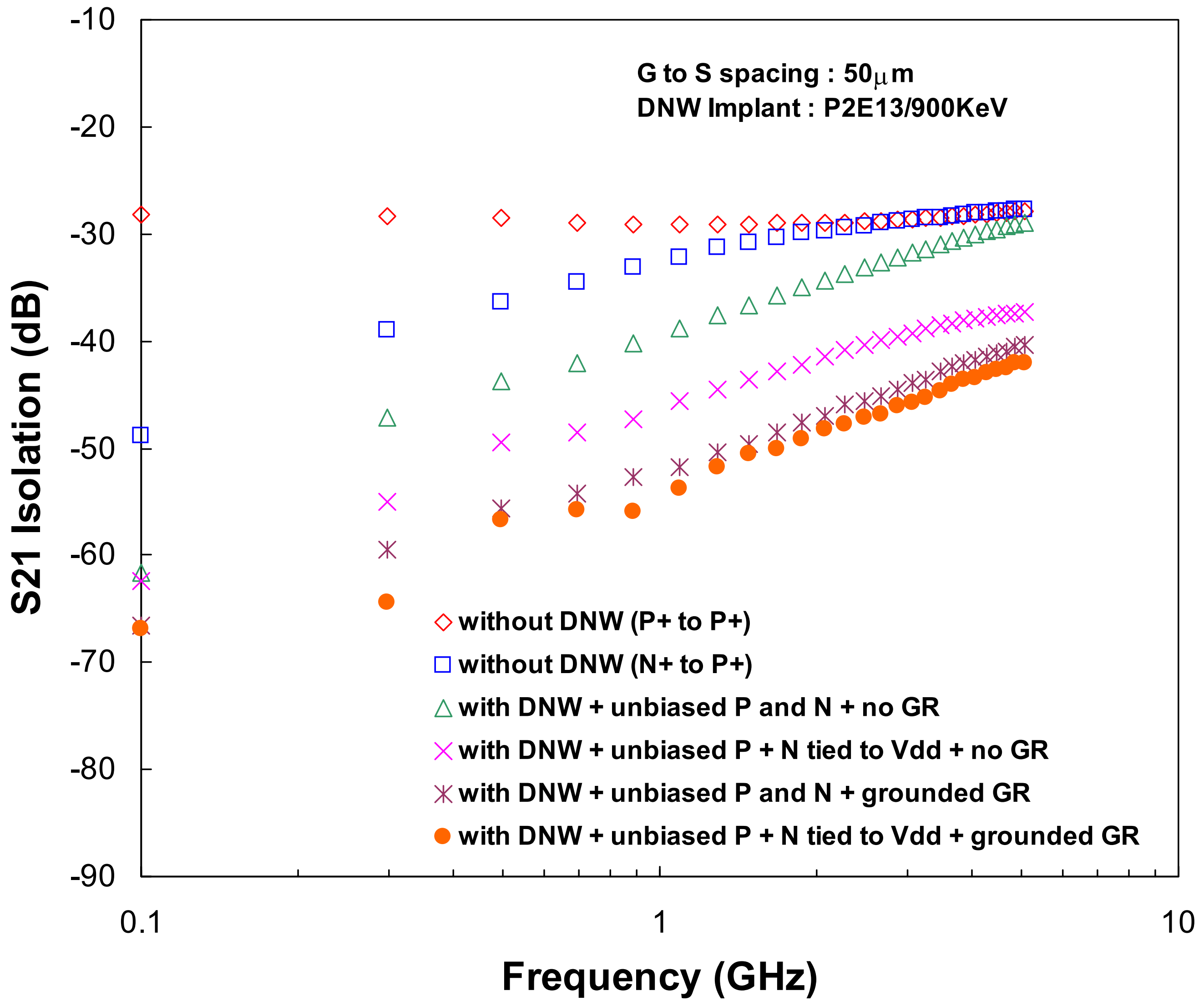
Effect of Different Body Biasing Techniques on RF Isolation for N^+ Noise Generators



Effect of Different Body Biasing Techniques on RF Isolation for N^+ Noise Generators



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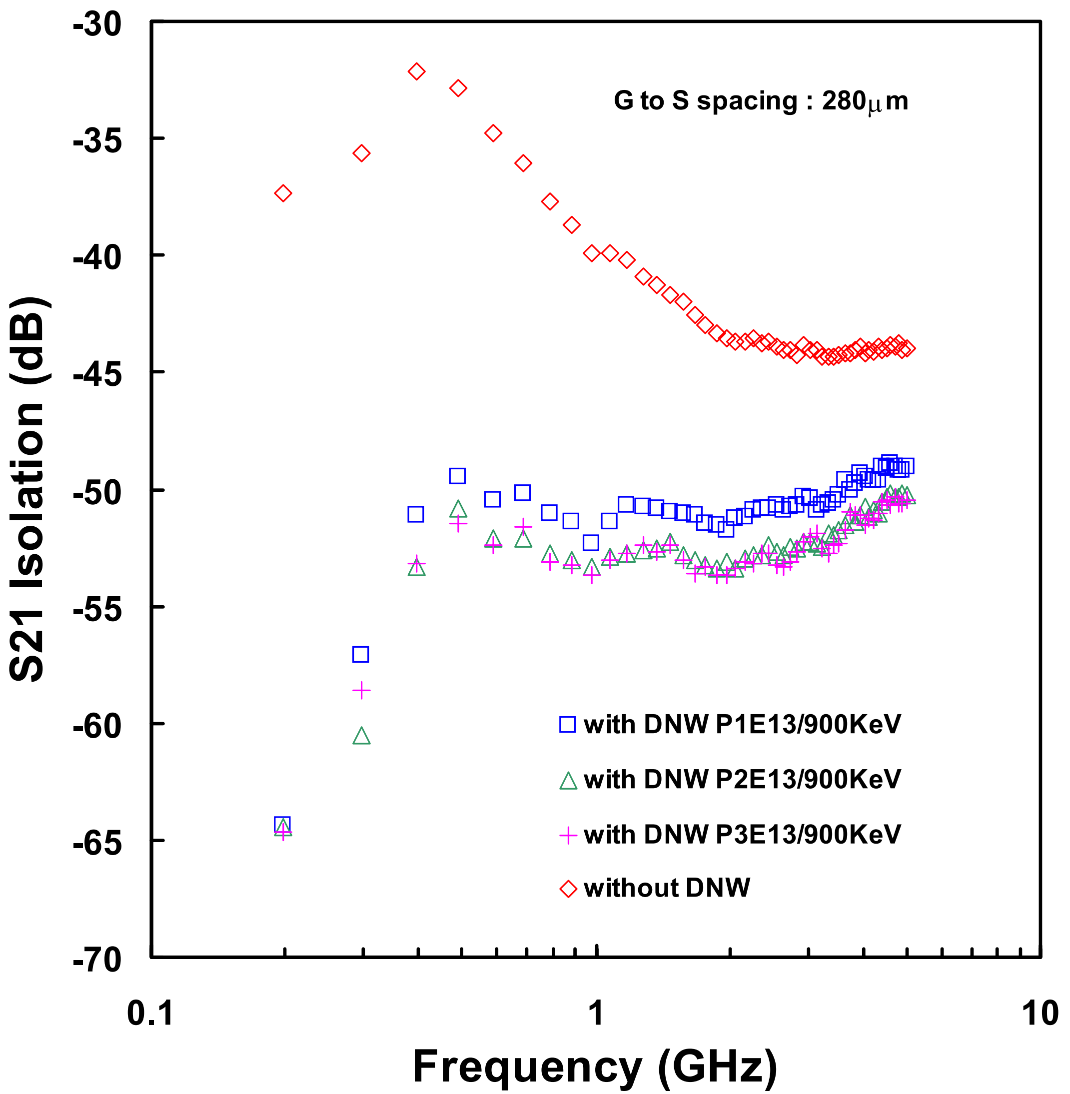
Effect of Deep Nwell Dosage on RF Isolation for P+ Noise Generators



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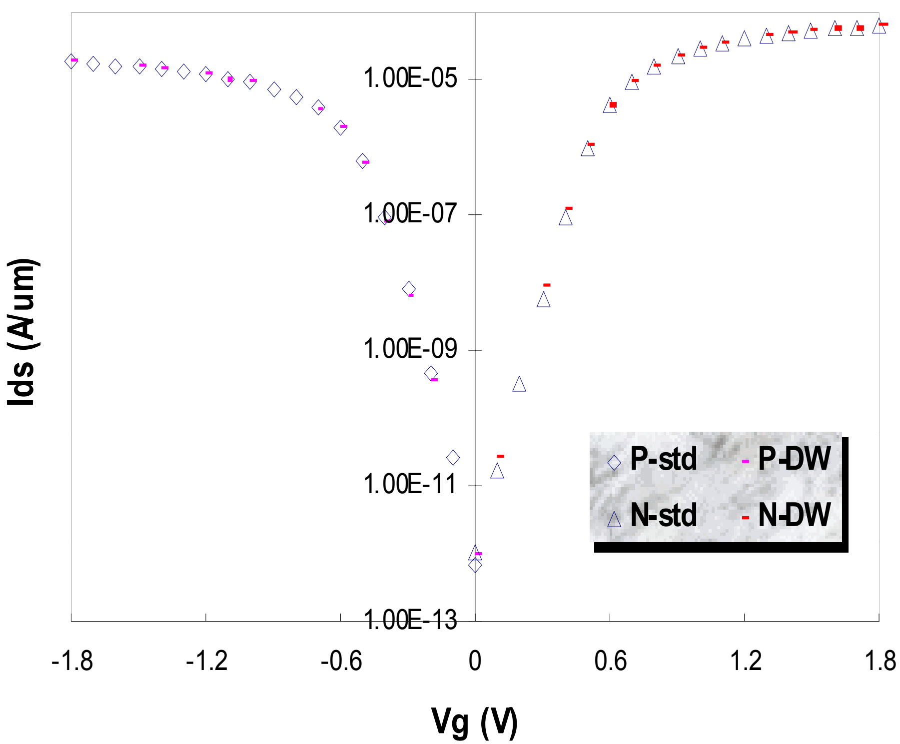
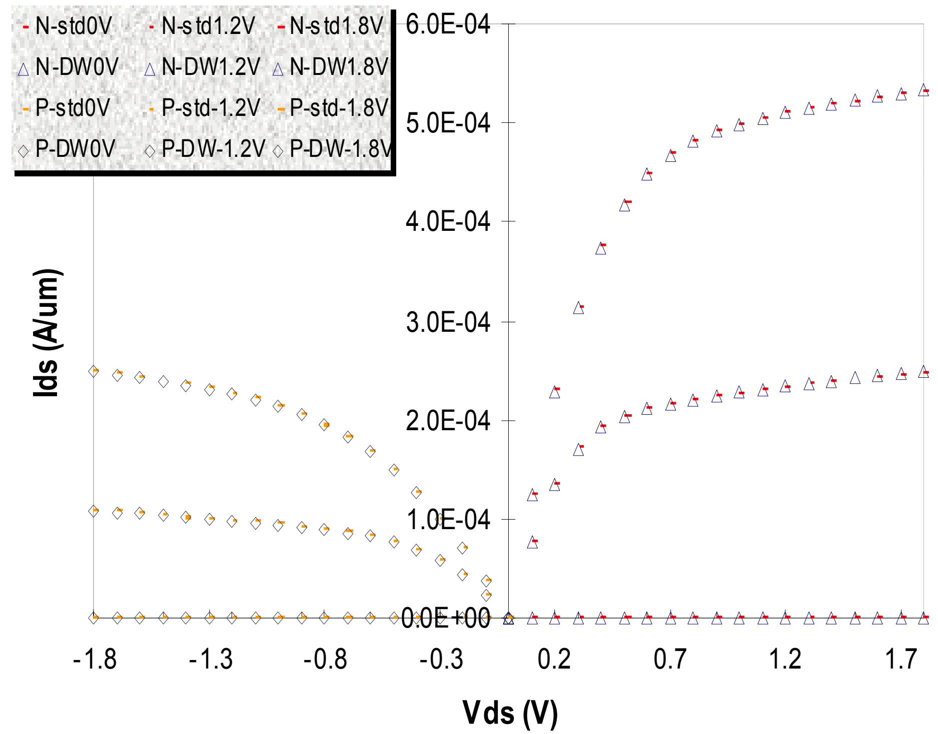
Thin-Gate Oxide MOSFETs in Deep N-well DC Characteristics





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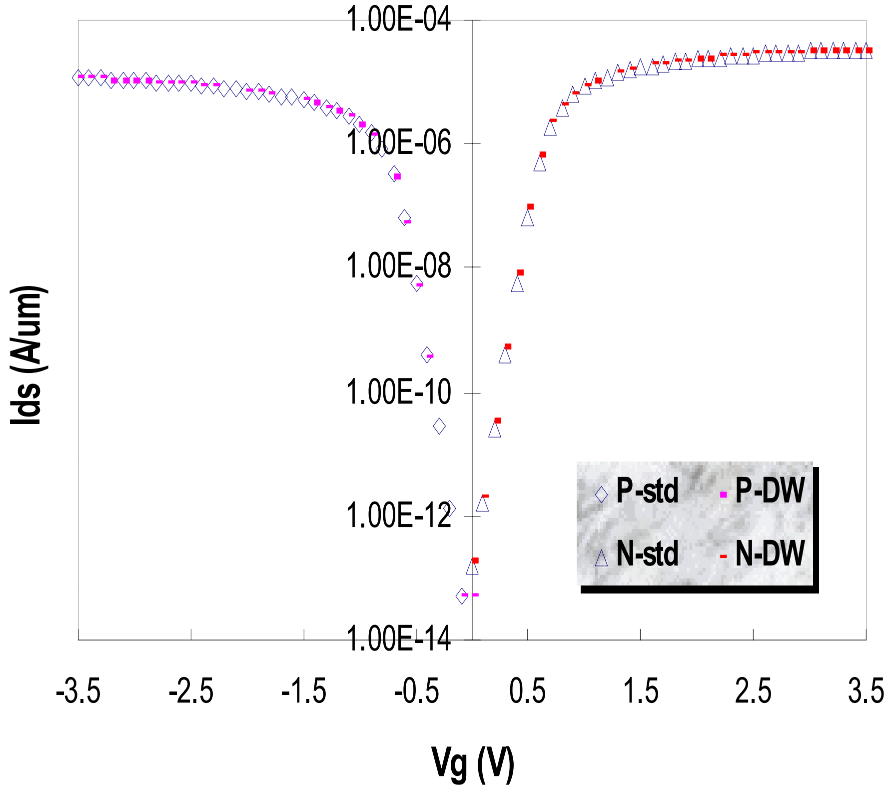
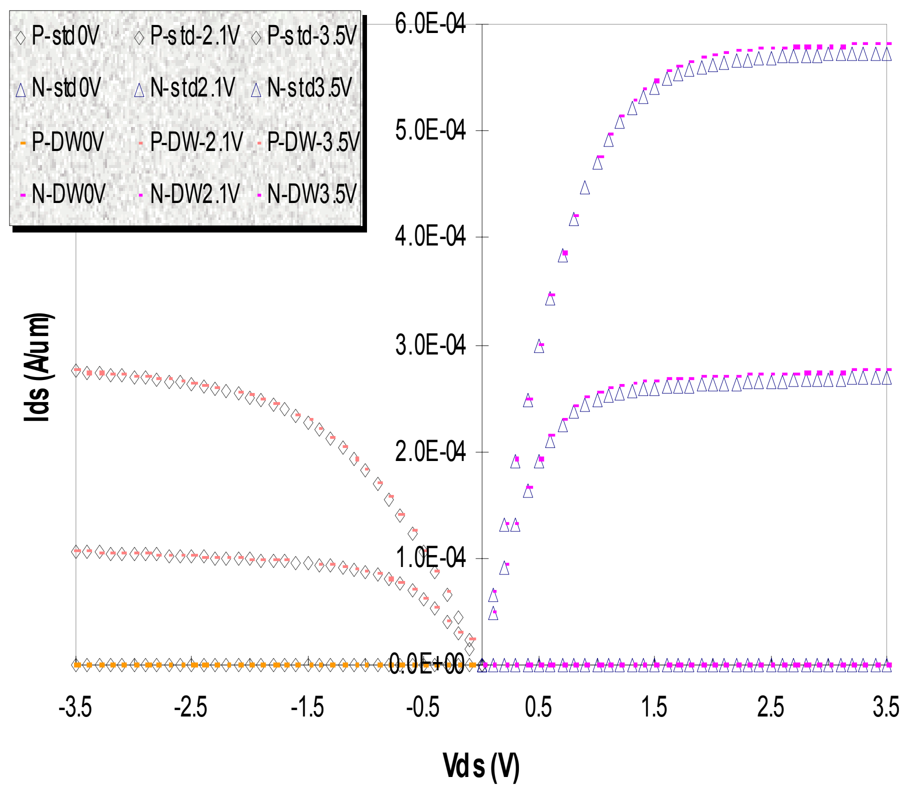
Thick-Gate Oxide MOSFETs in Deep N-well DC Characteristics





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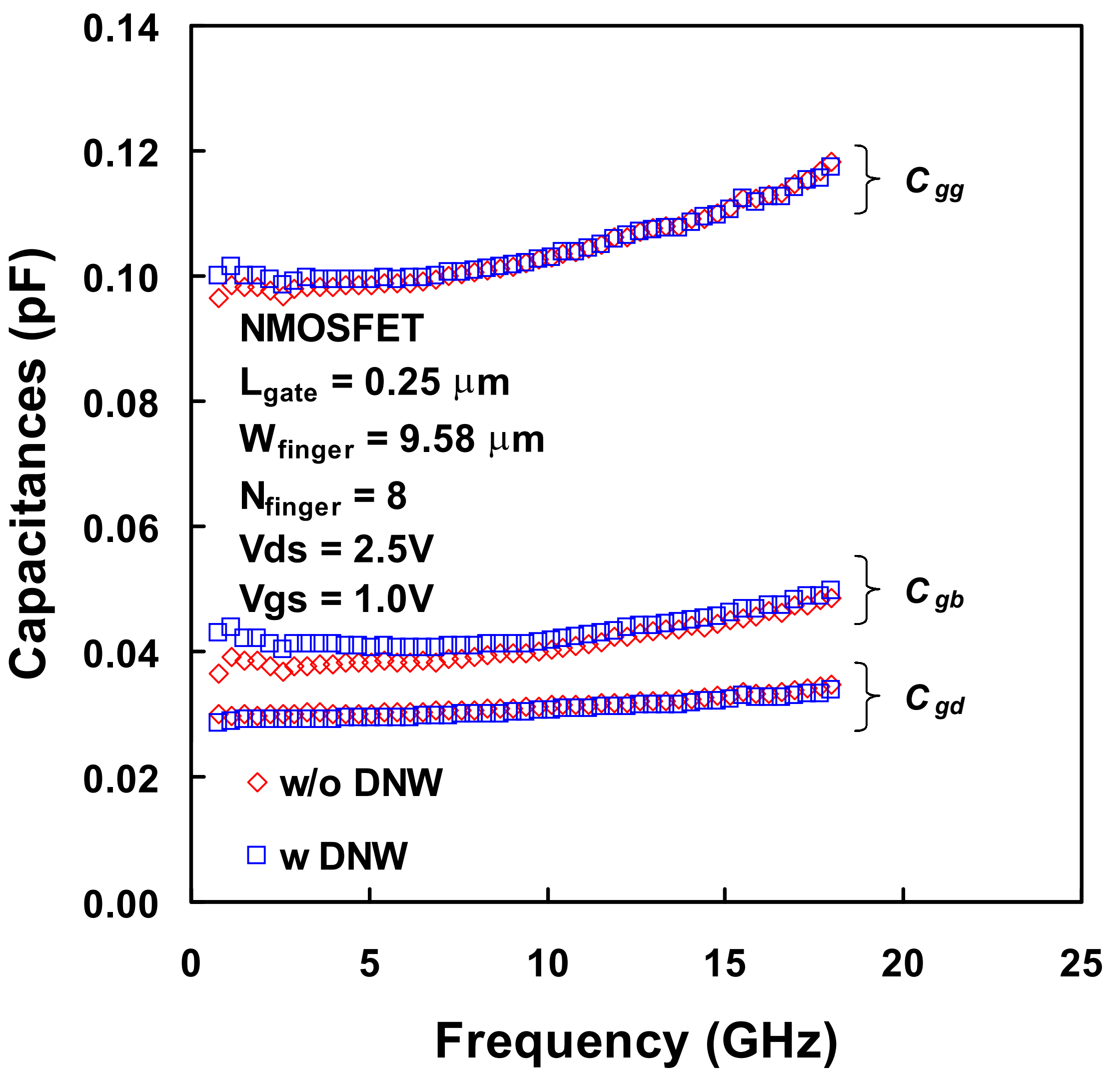
Effect of Deep Nwell on the RF Transistor AC Characteristics Extracted from S-parameters



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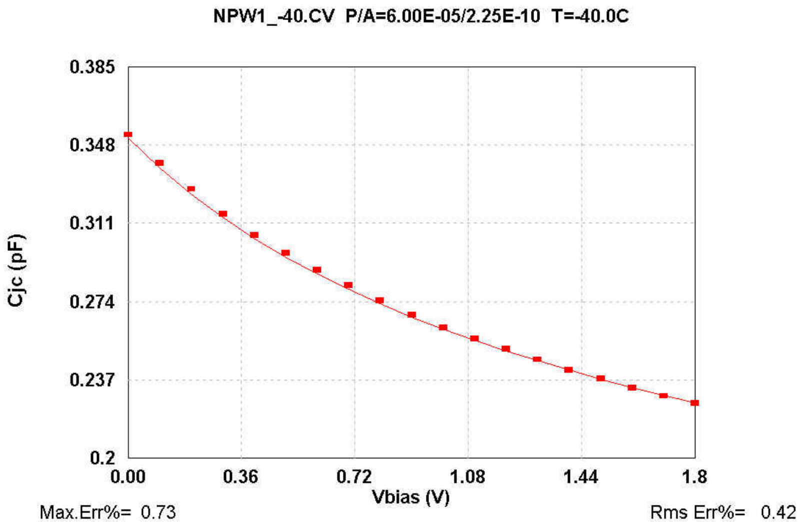
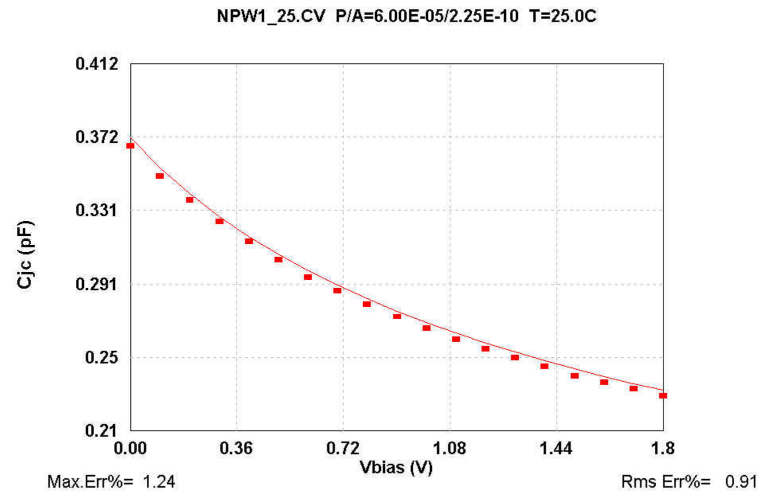
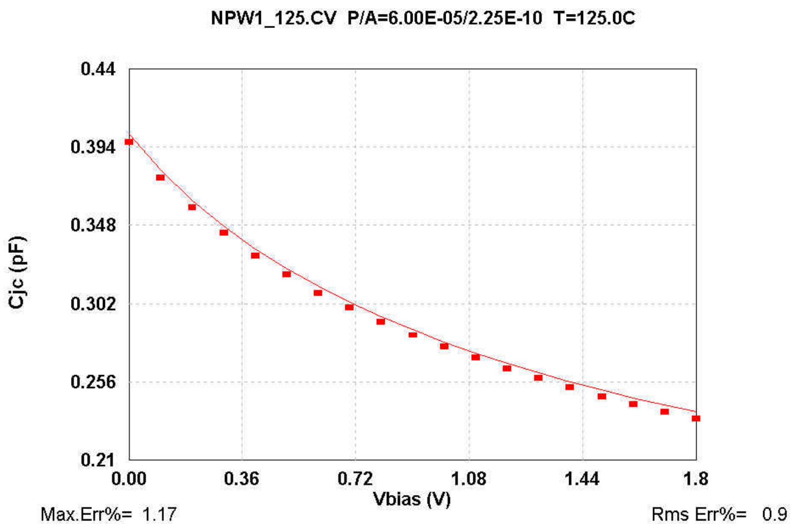
Effect of Deep Nwell on the RF Transistor AC Characteristics Extracted from CV Measurements







N^+/P-well Junction Capacitance
Area : 225 μm^2
Perimeter : 60 μm
Frequency : 100 KHz
Dot: with Deep Nwell
Line: without Deep Nwell

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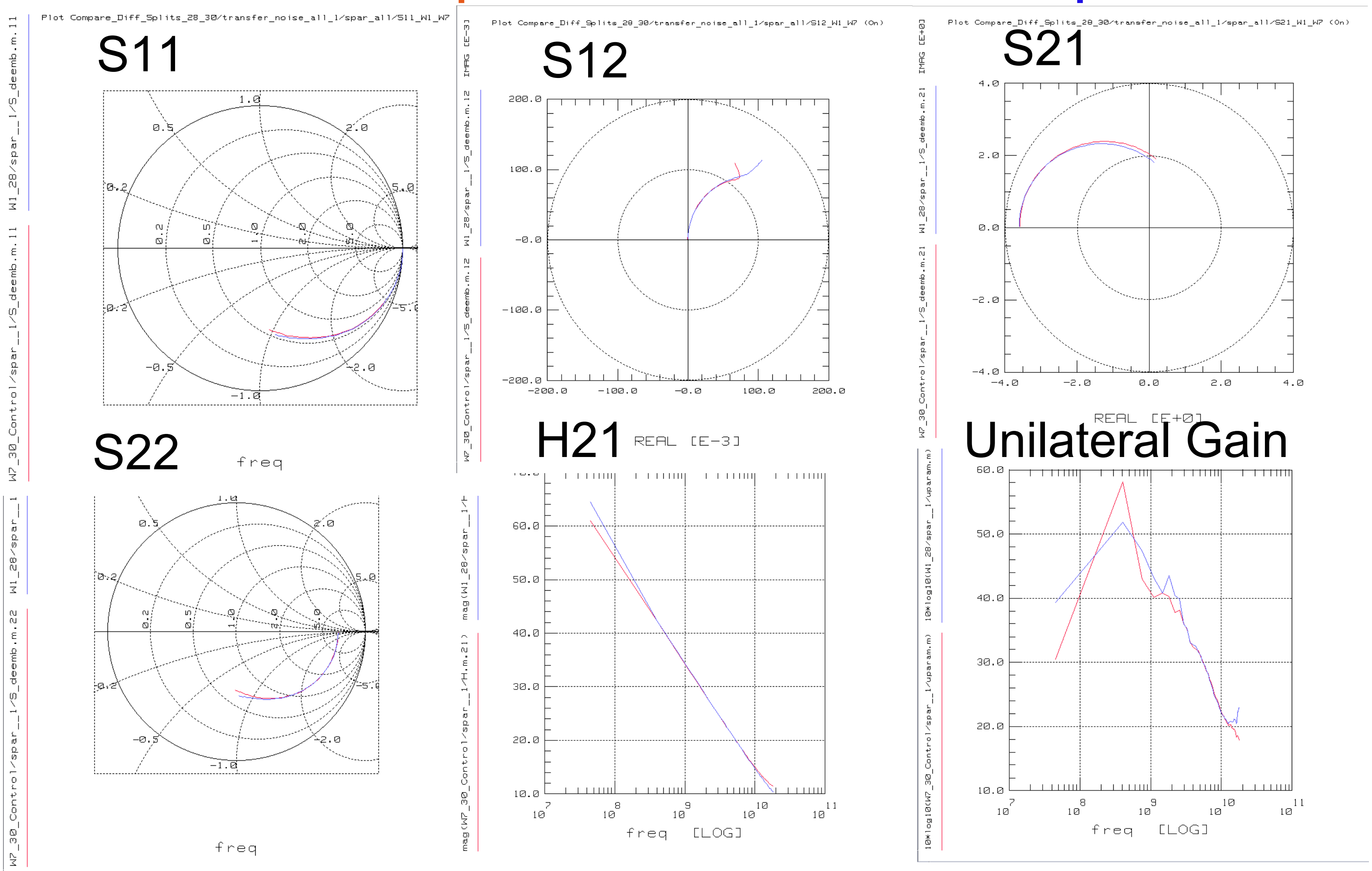
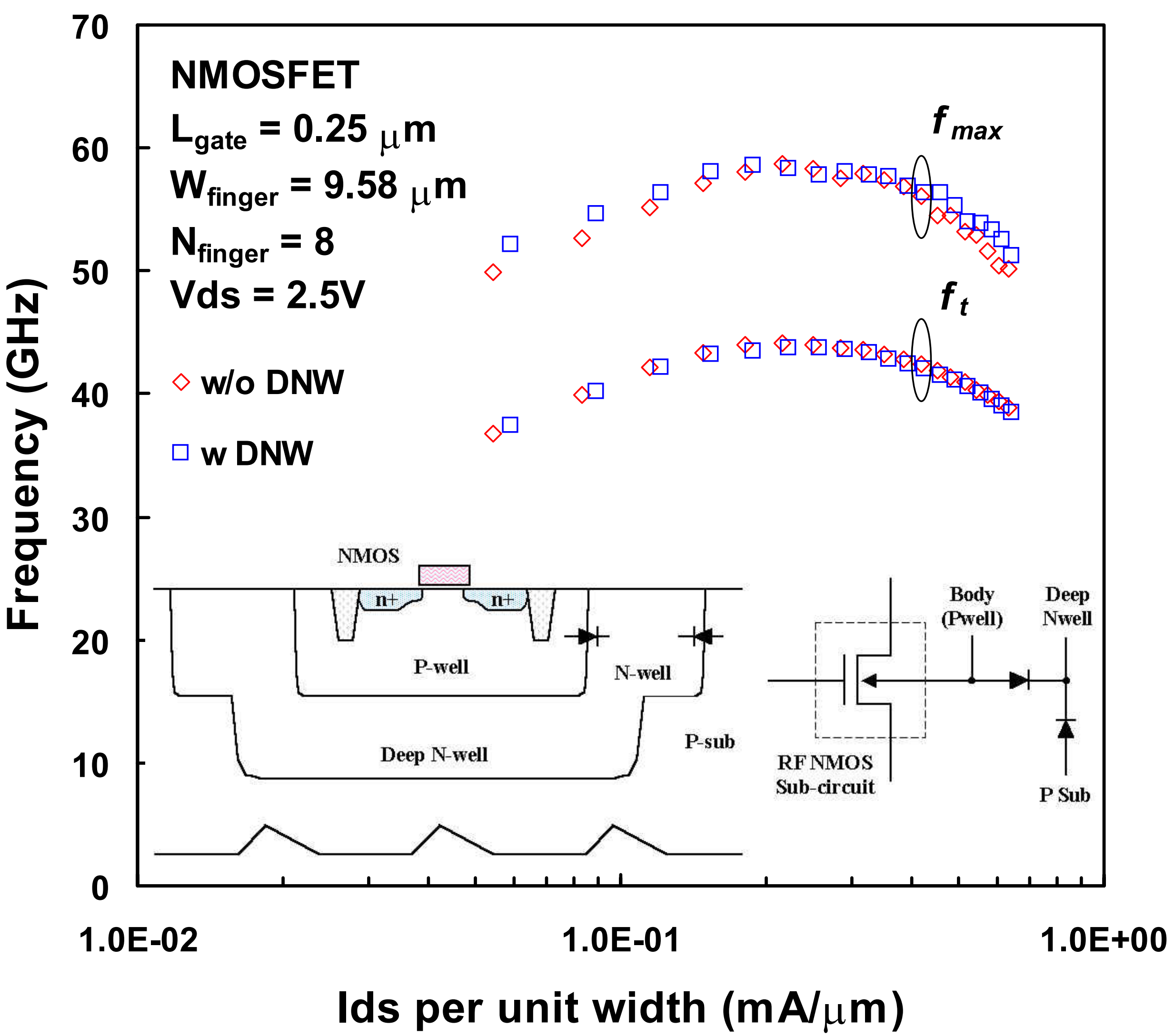
Comparison of RF Transistor High Frequency Characteristics with and without Deep N-well

Red : without Deep N-well **Blue : with Deep N-well**

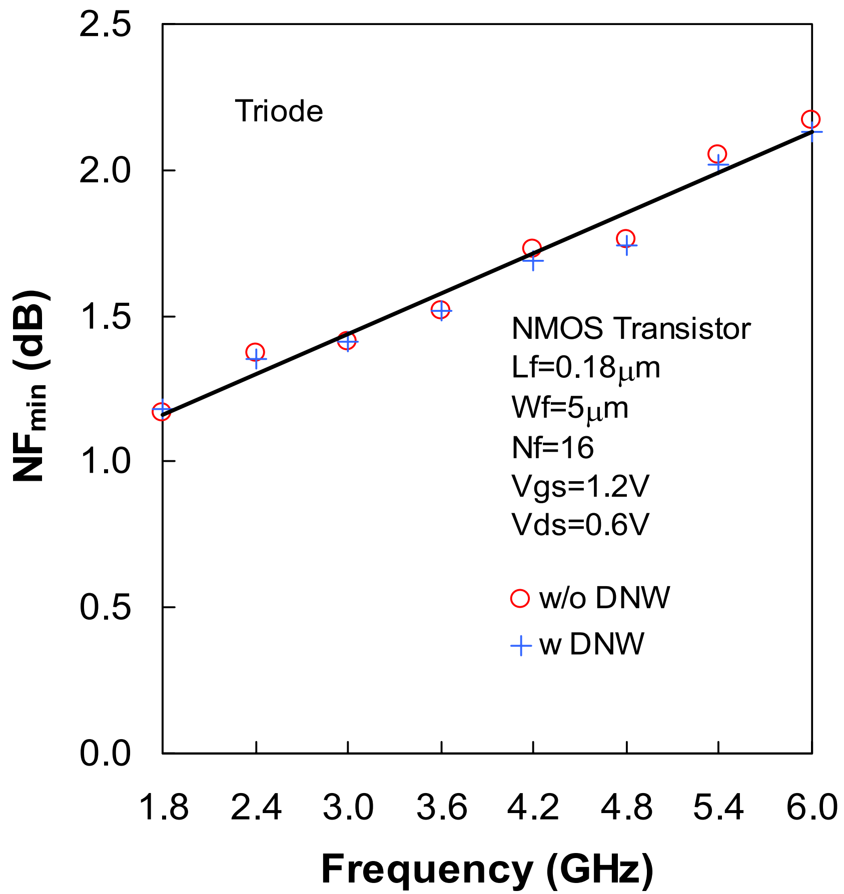


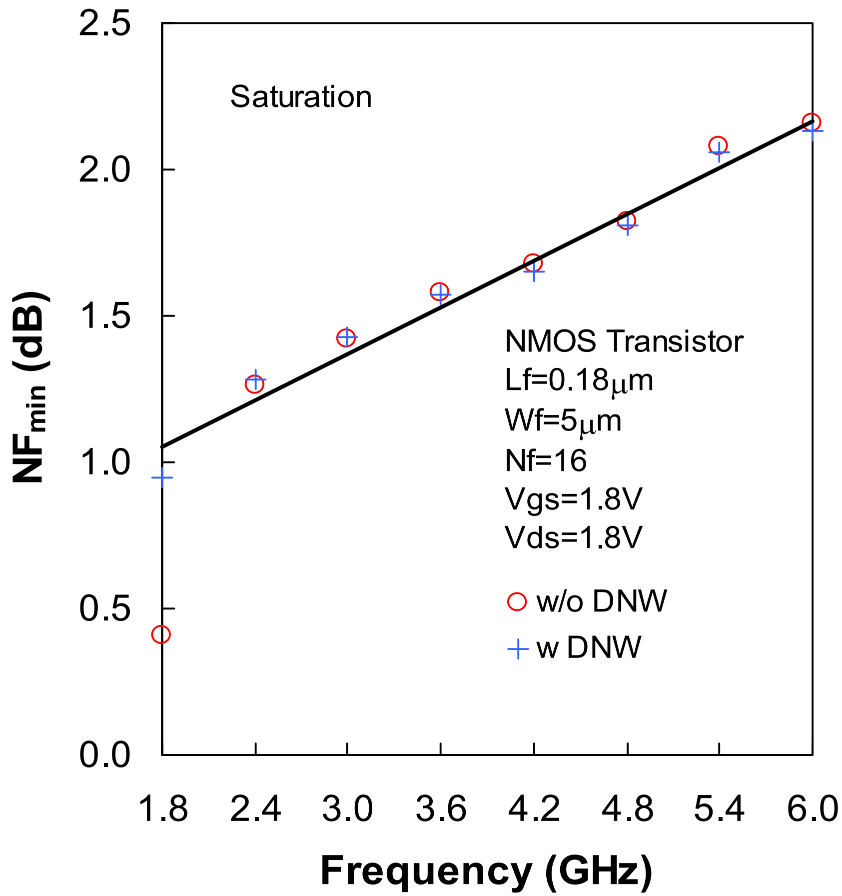
Effect of Deep N-well on RF Transistor Figures-of-Merit



Comparison of RF Transistor HF Noise Characteristics with and without Deep N-well

Red : without Deep N-well **Blue : with Deep N-well**





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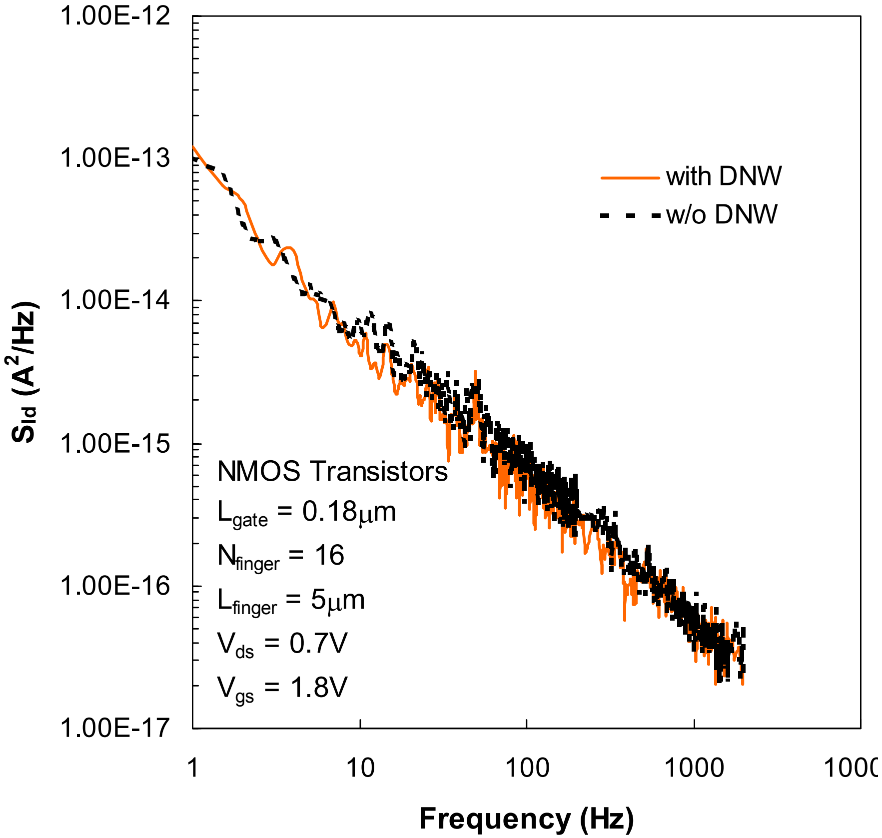
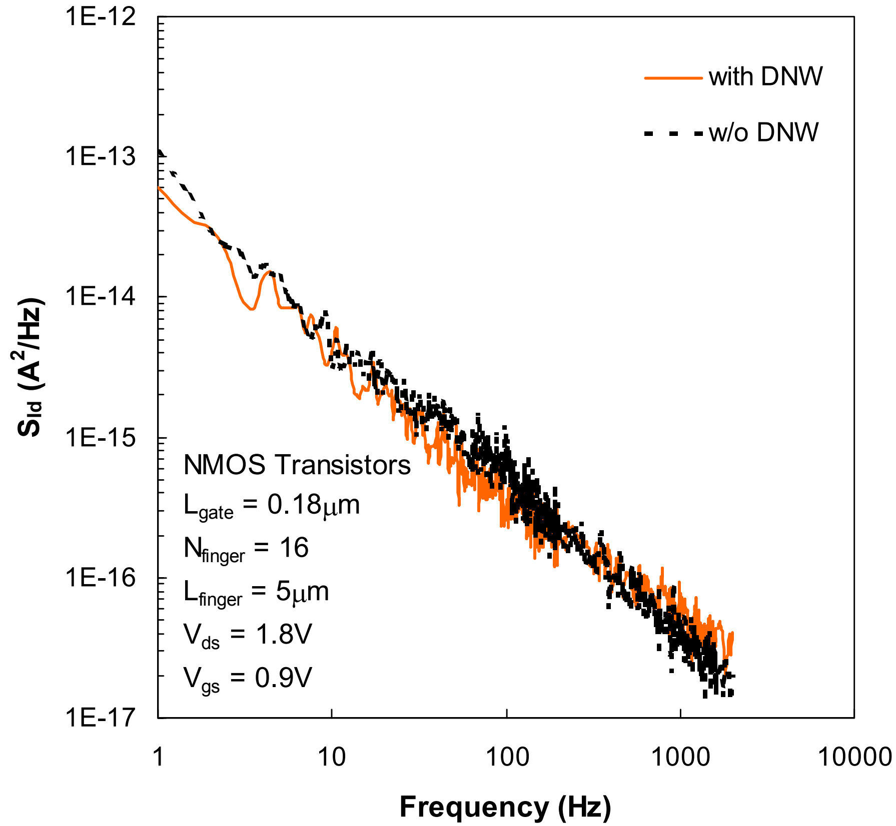
Comparison of RF Transistor 1/*f* Noise Characteristics with and without Deep N-well



Triode



Saturation

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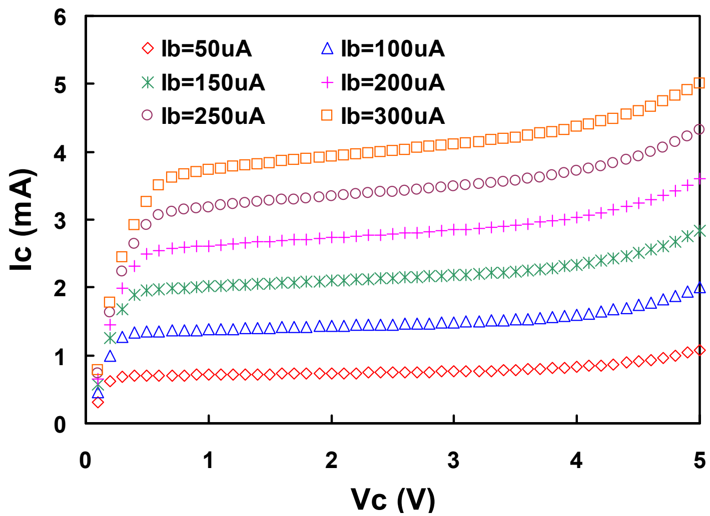
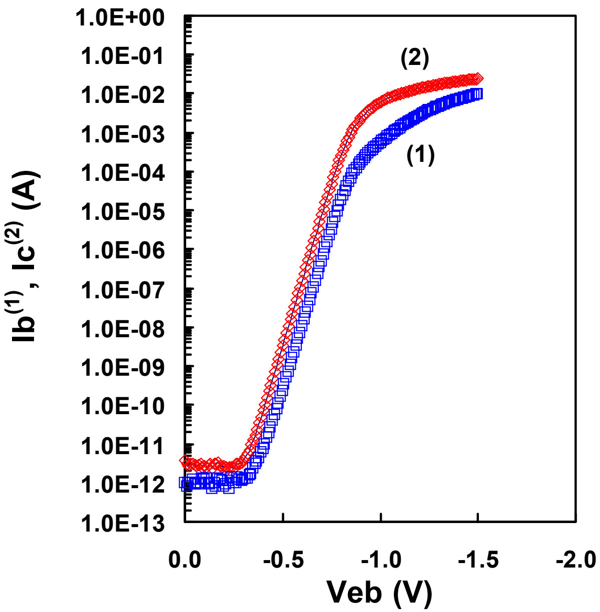
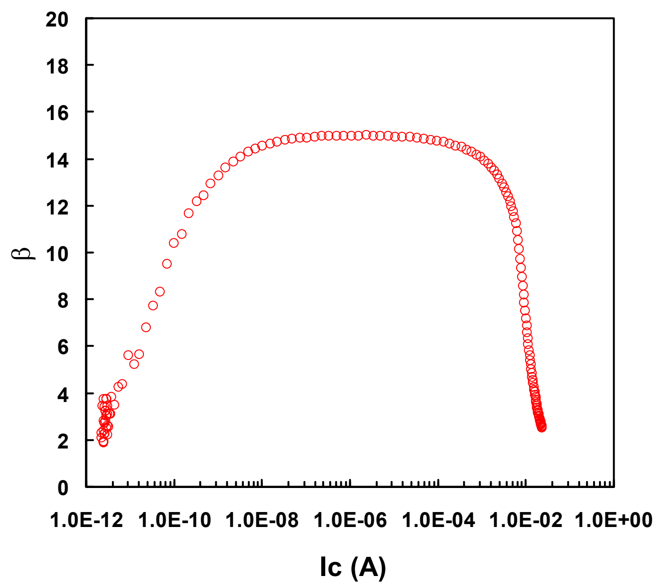
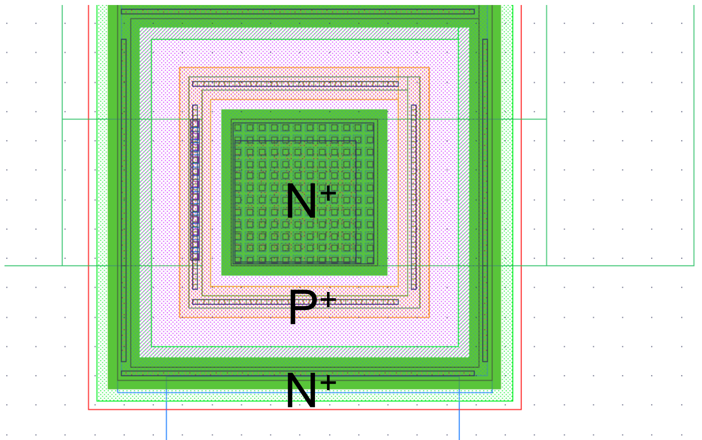
Vertical NPN Bipolar from the 0.18 μm Deep N-well Technology



- V_A = 22V
- BV_{CEO} = 6V
- BV_{CBO} = 17V







A_E : 5X5 μm^2

Conclusions

1. Deep n-well is effective in isolating substrate coupling for NMOSFET
2. Maximum of 35 dB isolation at 100 MHz obtained with deep n-well plus grounded nwell and p^+ guard ring, using deep n-well dose and implant energy of P1E13 @ 900 KeV
3. Deep n-well process with optimum dosage and energy will not impact the dc, ac, rf, and noise performance
4. Vertical NPN bipolar with beta of 14 can be obtained from the deep n-well technology